E Repeaters

E.1 Overview

The introduction of the Gen 2 data rate that doubles the Gen 1 data rate has led to increased channel loss which increases the need for repeaters. This includes the use of a repeater on some platforms in order to compensate for this channel loss and preserve the system routing requirement in terms of signal integrity. Likewise, there is a growing need for longer cables that require repeaters in the cable itself to support the extended lengths. As a result, new connectivity models emerge in USB 3.1 that include multiple repeaters between the host and device.

While the presence of repeaters effectively address the signal integrity needs of a system, they also introduce propagation delay that needs to be accounted for in both Gen 1 and Gen 2 data rates. In this Appendix, the link delay is defined for the pertinent system elements including the host, device, repeaters, and active cables. In addition, the details of a re-timer, a specific type of repeater architecture, are provided.

E.1.1 Term Definitions

In this document, the following definitions apply:

Repeater refers to any active component that acts on a signal in order to increase the physical lengths and/or interconnect loss over which the signal can be transmitted successfully. The category of repeaters includes both re-timers and re-drivers, which are defined below.

Re-timer refers to a component that contains a clock-data recovery (CDR) circuit that "retimes" the signal. The re-timer latches the signal into a synchronous memory element before re-transmitting it. It is used to extend the physical length of the system without accumulating high frequency jitter by creating separate clock domains on either side of the re-timer. Furthermore, a re-timer can be implemented based on one of the following architectures.

- SRIS (Separate Reference clock Independent SSC) re-timer refers to a re-timer implementation that has it's transmit clock derived from a local reference clock and is independent of the recovered clock at its receiver.
- Bit-level re-timer refers to a re-timer implementation that has it's transmit clock derived from the recovered clock at its receiver, except during part of link training.

A single-lane re-timer refers to a re-timer implementation capable of both Gen 1x1 and Gen 2x1 operation.

A dual-lane re-timer refers to a re-timer implementation capable of both Gen 1x2 and Gen 2x2 operation.

Both SRIS re-timer and bit-level re-timer are implemented with protocol awareness (refer to Section E.2.2.2 for details). In this Appendix, unless otherwise specified, a re-timer refers to either a SRIS re-timer or a bit-level re-timer.

Re-driver refers to an analog component that operates on the signal without re-timing it. This may include equalization, amplification, and transmitter. ~~The re-driver does not include a CDR. Re-drivers are beyond the scope of this document~~The re-driver does not include a CDR, and as a result, it does not cancel completely the jitter from the input, but only to compensate partially for the channel loss through equalization and amplification. Note that a re-driver in Gen 1 operation may employ a limiting re-driver that does not

maintain the linearity of its input signal. However, a re-driver in Gen 2 operation is required to be a linear re-driver to preserve the linearity of its input signal. In this Appendix, a minimum set re-driver behavioral and electrical requirement are defined to provide a reference re-driver implementation guideline. In addition, a system-level re-driver integration and link performance analysis are recommended to ensure maximum re-driver interoperability.

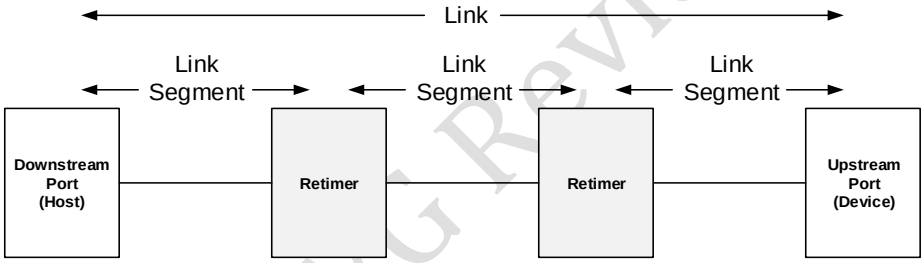
Captive re-timer or on-board re-driver refers to a re-timer or re-driver that is located on the same host or device system. The re-timer or re-driver is said to be associated with the host or device.

Link segment applies to re-timer only and it refers to a transmitter-channel-receiver combination between:

- A downstream port and a re-timer upstream port
- an upstream port and a re-timer
- two re-timers

This is shown in Figure E-1.

Figure E-1. Link Segment Definition



E.1.2 Scope of the Re-time Connectivity and Link Delay Budget

The scope of this Appendix covers SRIS re-timers and bit-level re-timers, which may be used on a printed circuit board in conjunction with a host or device, or as part of a cable assembly.

The USB usage model, which matches hosts, devices and cables at the time of usage, allows for the construction of systems that include re-timers on all three components. The requirements set forth in this Appendix comprehend the use of up to four re-timers in system configurations where a host and/or a device implementation may differ with respect to Pending_HP_Timer timeout value. Note that the Pending_HP_Timer timeout value varies based on different revisions of the specifications.

E.1.2.1 Re-timer Connectivity Models

This section defines the maximum number of re-timers allowed in two specific link connectivity models. Each contains an active cable with two re-timers. Those two connectivity models are the foundation to define the number of captive re-timers allowed and the link delay budget among host, device, active cable, and re-timers.

The two link connectivity models are defined based on host and device implementations with different Pending_HP_Timer timeout values.

- 3-µs host or device: implementations based on USB 3.1 Specification Revision 1.0 (July 26, 2013) and earlier revision that conform to the minimum Pending_HP_Timer timeout value of 3 µs. Note that 3-µs host or device applies only to x1 operation.

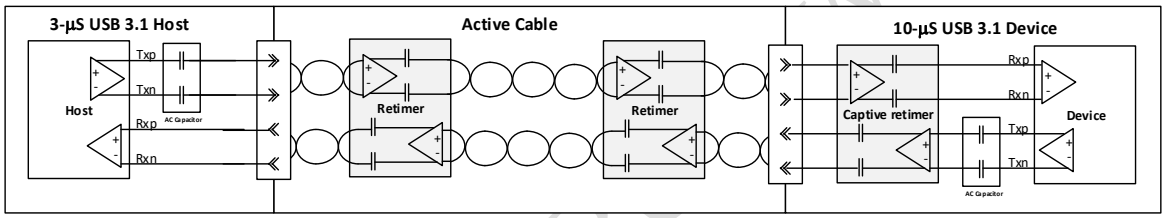
- 10-µs host or device: implementations based on USB 3.1 Specification Revision 1.0 (July 26, 2013) in conjunction with USB 3.1 Pending_HP_Timer ECN, and future Revisions incorporating this ECN, that conform to the minimum Pending_HP_Timer timeout value of 10 µs. Note that a 10-µs USB 3.1 host or device implementation also incorporates USB 3.1 PM_Timer ECN and USB 3.1 Ux_LFPS_Exit ECN. Note that 10-µs host or device may apply to either x1 or x2 operation.

E.1.2.1.1 3-Re-timer Connectivity

The 3-re-timer connectivity refers to connectivity of a 3-µs host or device that is connected with a 10 µs device or host. Under this configuration, a maximum of three re-timers may be supported, one with a 10-µs host or device, the other two may be in an active cable. Note that there is no re-timer in a 3 µs device or host.

An example link configuration is shown in Figure E-2, with a 3-µs host, and two re-timers in the active cable, interoperating with a 10-µs device including one re-timer on the device implementation. Note that it is assumed that a 3-µs host or device does not need retiming.

Figure E-2. Example Link Configuration of a 3-µs Host with a 10-µs Device

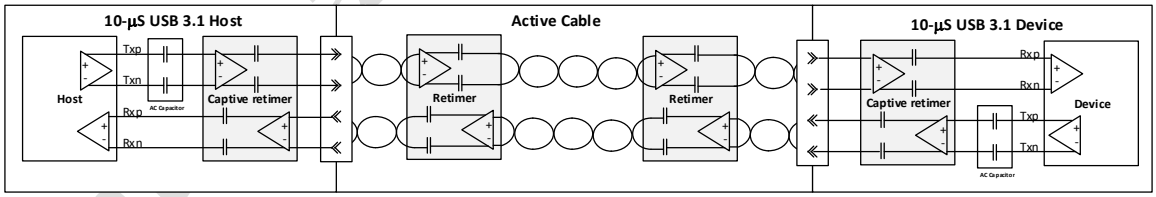


E.1.2.1.2 4-Re-timer Connectivity

The 4-re-timer connectivity refers to a 10-µs host or device connected to a 10-µs device or host. Under this configuration, a maximum of four re-timers may be supported.

An example link configuration is shown in Figure E-3, with a 10-µs host connected with a 10-µs ~~USB 3.1~~ device through an active cable.

Figure E-3. Example Link Configuration of a 10-µs Host with a 10-µs Device



E.1.2.2 Link Delay Budget Requirement

The link delay budget requirements is defined based on the 3-re-timer connectivity model in x1 operation. It is bounded by Pending_HP_Timer shown in Figure E-4.

- The total link delay budget is 2800 ns. This is defined assuming the following timings of a 3-µs host or device operating in ~~USB 3.1~~x1 mode.
    - The Pending_HP_Timer timeout value is 3 µs.
    - The combined Tx data path and Rx data path delays are 200 ns.

E.1.2.2.1 Gen 1x1 Link Delay Budget

The link delay budget of the 3-re-timer connectivity model in Gen 1x1 operation is divided with reference to the connectivity model defined in Section E.1.2.1.1.

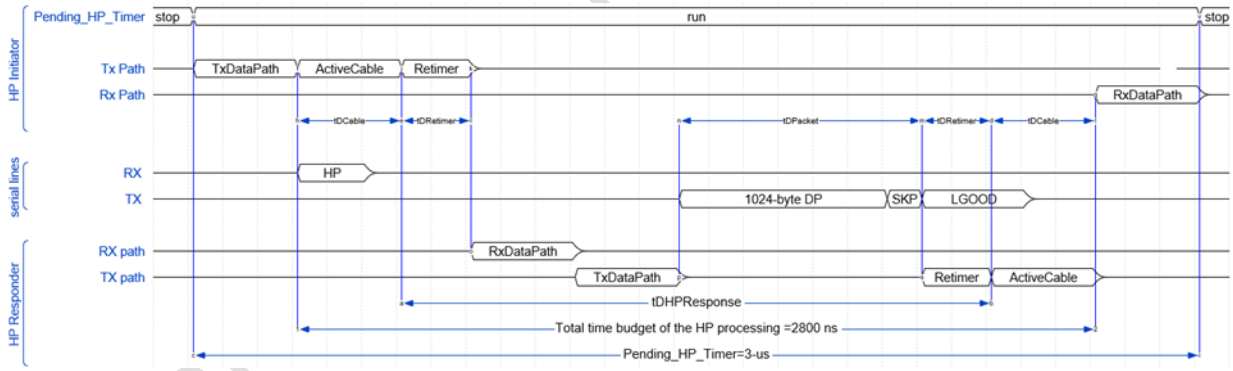
- tDCable: The propagation delay of the cable up to maximum 125 ns. This includes the propagation delay of the cable up to 5 m cable with a maximum of two re-timers.
- tDRe-timer: The maximum delay of a single re-timer up to 50 ns.
- tDHPResponse: The maximum delay of the HP response time not exceeding 2540 ns. Note that this includes the worst case delay (tDPacket = 2140 ns) when additional packets are scheduled ahead of the link command. Refer to Section 7.5.6.1 for definition of the HP response time.

E.1.2.2.2 Gen 2x1 Link Delay Budget

The link delay budget of the 3-re-timer connectivity model in Gen 2x1 operation is divided with reference to the connectivity model defined in Section E.1.2.1.2.

- tDCable: The propagation delay of the cable up to maximum 305 ns. This includes the propagation delay of the cable up to 5 m cable with a maximum of two re-timers.
- tDRe-timer: The maximum delay of a single re-timer up to 140 ns.
- tDHPResponse: The maximum delay of the HP response time not exceeding 1610 ns. Note that this includes the worst case delay (tDPacket = 910 ns) when additional packets are scheduled ahead of the link command. Refer to Section 7.5.6.1 for definition of HP response time.

Figure E-4. Link Delay Budget in 3-re-timer Connectivity Model



E.2 Re-timer Architectural Overview and Requirement

A re-timer's responsibility is to restore an attenuated incoming signal to the quality matching the transmitter requirement defined in Chapter 6 before re-transmission. To meet the transmit jitter requirement defined in Table 6-20, a SRIS re-timer relies on a local reference clock that is asynchronous to the recovered clock at its incoming data. This asynchronicity introduces phase and frequency offset between the incoming data and the outgoing data. For a bit-level re-timer, the clock used to transmit data is derived from a recovered clock on its incoming data. Only phase offset but no frequency offset is introduced.

A re-timer may be implemented to support x1 ~~operation~~ or x2 operation. This section summarizes the general requirements at PHY and Link Layers.

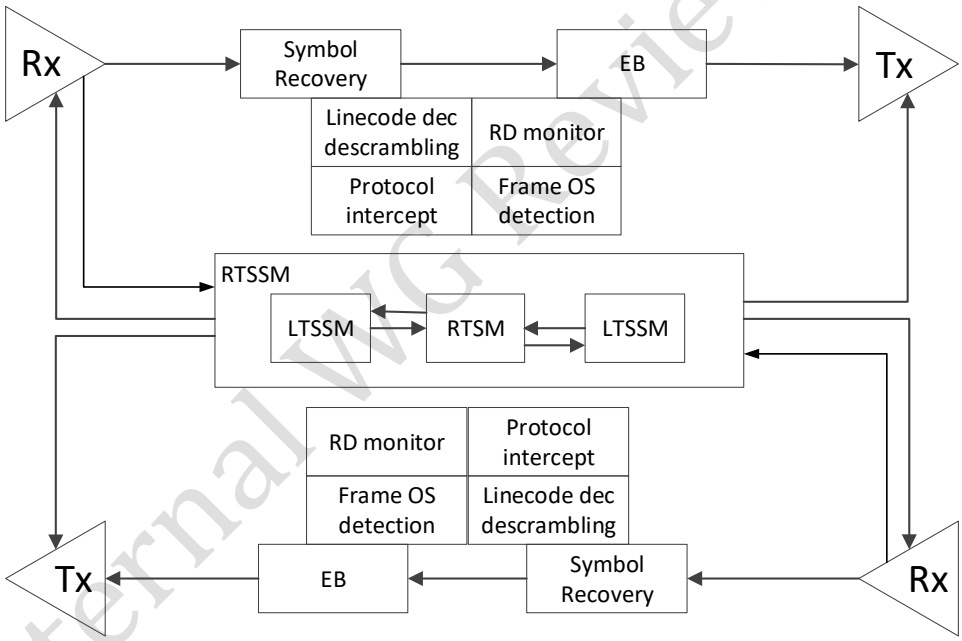
E.2.1 Architectural Overview

Shown in Figure E-5 are two high level re-timer architectural examples. In concept, each re-timer consists of a downstream port and an upstream port to perform clock data recovery at its receivers and data transmission at its transmitters. Each port may have its own LTSSM to manage the operation in various link states, and both LTSSMs are very similar to LTSSM defined in Chapter 7, but with differences unique to re-timer operation that are described in Section E.1. A re-timer state machine (RTSM) is employed to coordinate the operation between its upstream port and downstream port. In addition, RTSM is also responsible for, but is not limited to, serve the following management functions:

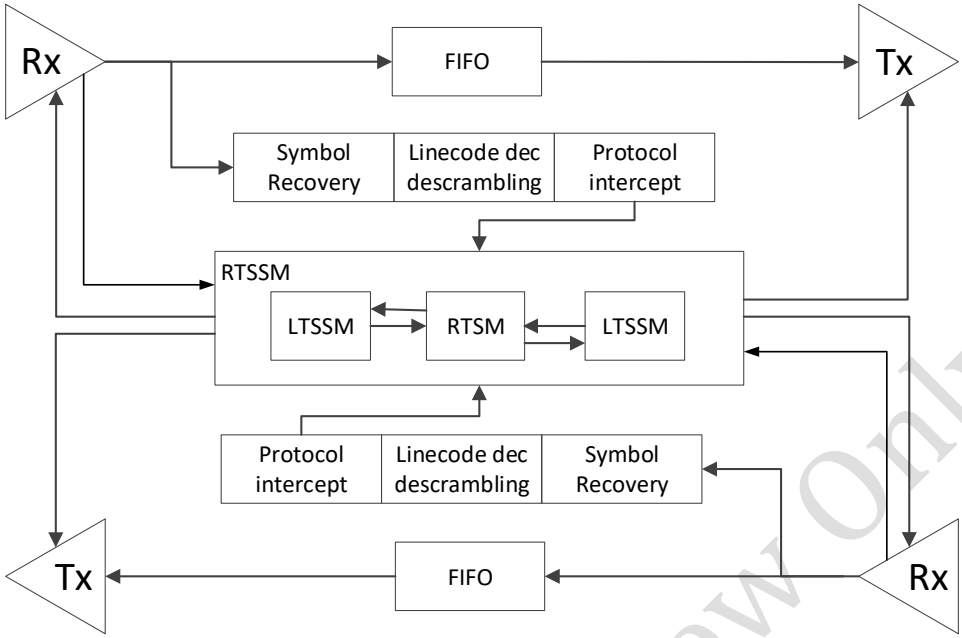
- Link state detection and re-timer power management.
- Data path management and clock offset compensation.
- Packet/link command detection.

A practical implementation of a re-timer may be architected with a single re-timer training and status state machine (RTSSM) to perform the link operation carried by LTSSM and RTSM.

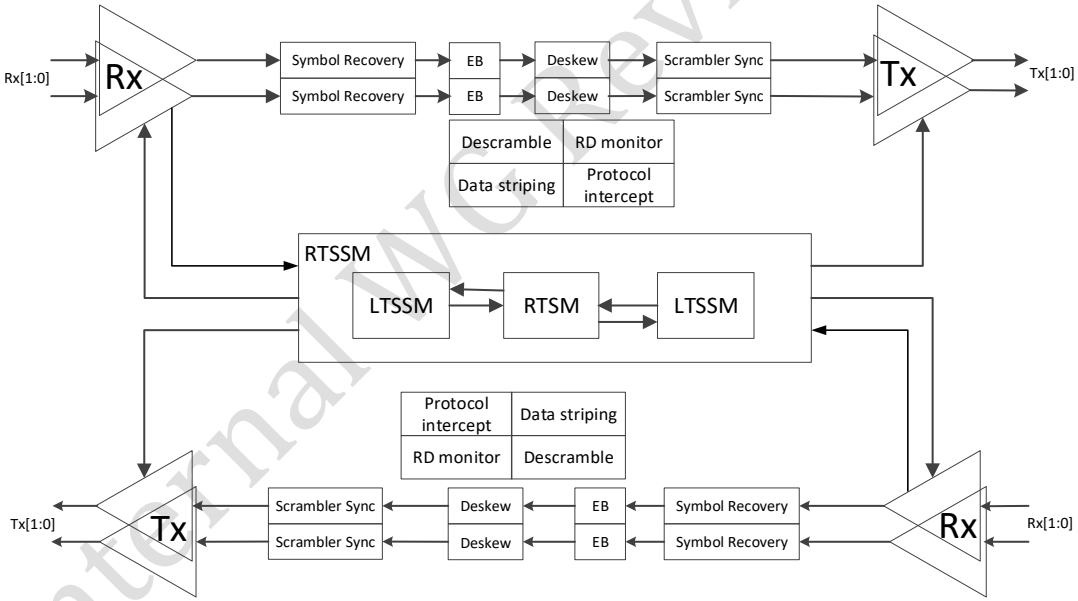
Figure E-5. Example Re-timer Architectures



(a) Example Block Diagram of a SRIS Re-timer Architecture



(b) Example Block Diagram of a Bit-Level Re-timer Architecture



(c) Example Block Diagram of a x2 Re-timer Architecture

E.2.2 General Requirements

A re-timer shall include the capability to successfully train and operate in both Gen 1 and Gen 2 modes. This includes implementation of all training and power states defined in Chapters 6 and 7.

The timing budgets, signal levels, and compliance specifications defined in Chapter 6 apply to re-timers. As with SuperSpeed and SuperSpeedPlus hosts and devices, SRIS re-timers shall implement the spread spectrum clocking (SSC) in compliance with the requirements contained in Section 6.5.3 and 6.5.4.

E.2.2.1 Physical Layer Requirements

A re-timer shall conform to the following requirement at the physical layer.

- It shall meet all the physical layer requirements defined in Chapter 6.
- For a bit level re-timer, it shall meet additional jitter transfer function requirement defined in Section E.5.

E.2.2.2 Link Layer Requirements

The purpose for re-timers to implement partial link layer function is to achieve protocol awareness such that the re-timer operation is in concert with the host and device. A re-timer shall implement the following capabilities.

- LFPS based Polling.LFPS, SCD1/SCD2, and LBPM tracking and decoding. A re-timer shall monitor Polling.LFPS and SCD1/SCD2 to determine ~~SeperSpeedPlus~~SuperSpeedPlus operation and decode LBPM to determine port configuration negotiated between the host and device. Refer to Section E.3.4 for details.
- TS2 ordered set decoding. A re-timer shall decode the link configuration field in TS2 ordered set to determine the link operation during Polling.Idle or Recovery.Idle. Refer to Sections E.3.4.5 and E.3.11 for details.
- Link command tracking. A re-timer shall track the link command and HPs to synchronize its link operation with the host and device. This includes but is not limited to determining the re-timer's upstream port to host and downstream port to device and tracking link power management. Refer to Section E.3.7 for details.
- Packet boundary tracking. A SRIS re-timer in SS operation shall track the packet boundary to perform the clock offset compensation. Refer to Section E.4.1 for details.

E.2.2.3 x2 Re-timer Requirements

In addition to meeting the general re-timer requirements defined in Sections E.2.2.1 and E.2.2.2, a re-timer in x2 operation shall also meet the following requirement.

- It shall establish the Configuration Lane when directed. Note that it is implementation specific for a captive re-timer or a re-timer in an active cable to determine the Configuration Lane.
- The re-timer shall perform the lane-to-lane deskew meeting ~~specifications~~requirements defined in Table 6-34. Specifically,
  - The re-timer shall complete the lane-to-lane deskew before switching from the local TS1 OS to received TS1 or TS2 OS. The re-timer may perform the lane-to-lane deskew based on either TS1 OS, TS2 OS, or SKP OS in Gen 1x2 operation, or SYNC OS in Gen 2x2 operation.
  - The re-timer shall preserve the OS boundary when switching from the local TS1 OS to received TS1 OS or TS2 OS to maintain transmitter lane-to-lane skew.
- The far-end receiver termination detection and the LFPS based operation shall be performed only on the Configuration Lane.
- The maximum re-timer delay (tDRe-timer) shall be 300 ns in Gen 1x2 operation, and 200 ns in Gen 2x2 operation.

E.3 Re-timer Training and Status State Machine (RTSSM)

The primary responsibility of a re-timer is to maintain connectivity between the host and device. This includes but is not limited to monitoring the state of connectivity between the host and device, participating the speed negotiation during initialization, link training with its link partners, tracking the link commands and HPs for link power management, and port orientation identification. A re-timer training, and status state machine (RTSSM) is defined to facilitate the successful operation of a re-timer. As shown in Figure E-6, RTSSM is similar to LTSSM defined in Chapter 7. The main differences are summarized in the following.

- eSS.Inactive is combined with Rx.Detect as the behaviors of a re-timer in those two states are the same. A re-timer, even upon detecting the presence of its far-end link partners, will not transition to Polling until Polling.LFPS is received.

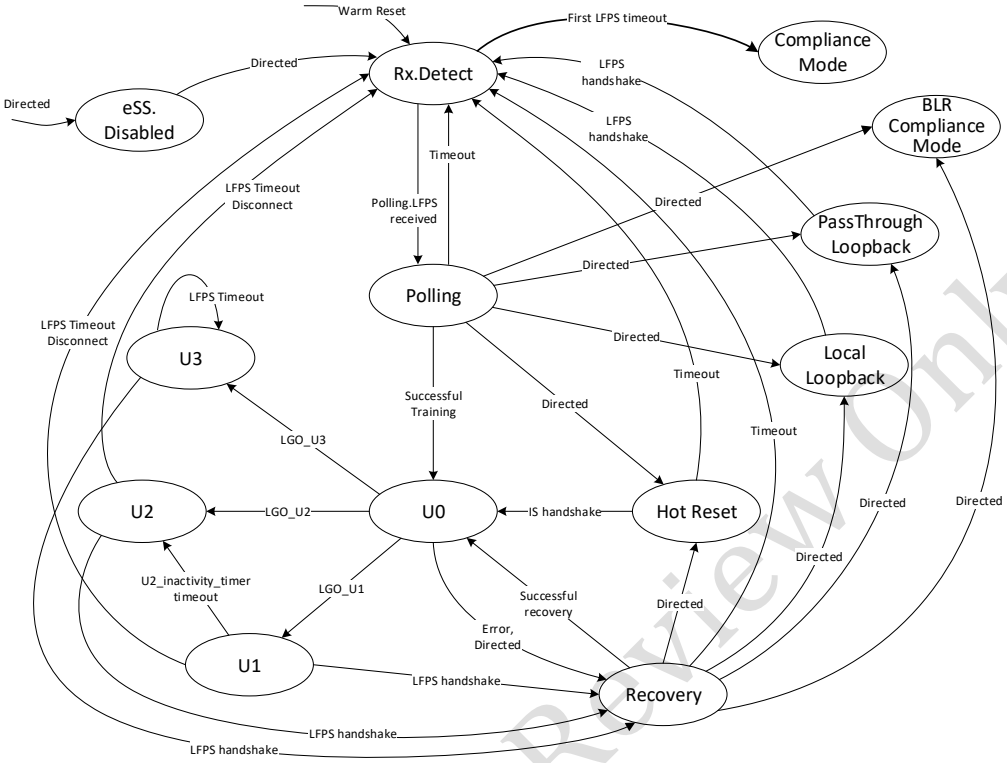
- eSS.Disabled is defined in LTSSM for a self-powered peripheral device where it may operate at USB 2.0 mode. The eSS operation is disabled and the link may enter the lowest power state. For re-timer operation, unless it is aware of the link configuration, it will not be able to take the advantage of this state. However, it is kept for implementations capable of managing the re-timer operation under proprietary mechanism, which is out of the scope of this specification.

- PassThrough Loopback is introduced for a re-timer. It is a special operation pertained to re-timers only when LTSSM is in Loopback. A re-timer in this state passes the inbound traffic directly as if it is in U0.

- Local Loopback is named to contrast PassThrough Loopback. The purpose and the operation of a re-timer in this state are the same as Loopback defined in LTSSM.

- BLR Compliance Mode is introduced to perform bit-level re-timer specific transmitter compliance test. The entry to this substate is based on the link configuration field of TS2 OS. Refer to Section E.3.6 for details.

Figure E-6. Re-timer Training and Status State Machine



In the following subsections, the details of RTSSM are described. The operations that are common to LTSSM will not be elaborated.

It is worth mentioning that the main purpose of RTSSM is to describe and define the re-timer operation under various LTSSM states. The external behavior of the RTSSM shall reflect that of the LTSSM. The implementation may vary regarding RTSSM optimization.

E.3.1 Warm Reset

Unlike devices that only need to detect Warm Reset, a re-timer has an added responsibility to detect and forward Warm Reset that complies with the electrical and timing specification defined in Section 6.9.3. The re-timer shall perform the following under different link states.

- In Rx.Detect, Polling, Recovery, U0, Hot Reset, Compliance Mode, or BLR Compliance Mode, if the LFPS signal is neither Polling.LFPS nor LBPM, the re-timer shall infer the reception of Warm Reset and forward the received LFPS signal within 200 µs.
- In U1 or U2, if the re-timer performs simultaneous Ux LFPS exit handshake, regardless of the Ux LFPS exit handshake status, the re-timer shall remain in Ux and continue the LFPS transmission at its downstream port if its upstream port continues to receive the LFPS signal. This is to ensure that the re-timer transmit continuous LFPS signal without interruption before resolving if the received LFPS signal at its upstream port is Ux LFPS exit handshake, or Warm Reset. The re-timer shall declare one of the following conditions.
    - It shall infer Warm Reset if the duration of the LFPS signal is more than 2 ms.
    - It shall declare the successful Ux LFPS exit handshake if the successful Ux LFPS exit handshakes are achieved at both ports and the duration of the received LFPS signal is less than 2 ms.

- It shall declare the failure of Ux LFPS exit handshake if it has not achieved the successful U1 or U2 LFPS exit handshake at either port within 2 ms.

- In U1, U2 or U3, if the re-timer forwards the LFPS signal, it shall forward the received LFPS signal regardless of the Ux LFPS exit handshake status. The re-timer shall declare one of the following conditions.
  - It shall infer Warm Reset if the duration of the LFPS signal is more than 2 ms when exit from U1 or U2, or 10 ms when exit from U3.
  - It shall declare the successful Ux LFPS exit handshake if the successful Ux LFPS exit handshakes are observed at both ports and the duration of the received LFPS signal is less than 2 ms when exit from U1 or U2, or 10 ms when exit from U3.
  - It shall declare the failure of Ux LFPS exit handshake if the successful U1 or U2 LFPS exit handshake is not observed at either port within 2 ms when exit from U1 or U2, or 10 ms when exit from U3.
- In U3, if the beginning part of Warm Reset is treated as U3 LFPS exit signal from the host, and the re-timer is not ready to exit from U3, the re-timer shall transition to U3S and monitor the duration of the LFPS signal. It shall infer Warm Reset if the received LFPS signal is more than 15 ms. The re-timer shall forward the LFPS signal and complete the Warm Reset transmission meeting the timing specification defined in Section 6.9.3.
- In PassThrough Loopback or Local Loopback, there is no need to distinguish between Warm Reset and the Loopback LFPS exit handshake. The re-timer transitions to Rx.Detect in either condition.

E.3.2 Rx.Detect

Rx.Detect is the default power-on state of the re-timer. The re-timer's responsibility is to detect the presence of its link partners by performing far-end receiver termination detection periodically and to mirror the presence status of its link partners. Rx.Detect also serves as an error state for the re-timer when an error situation is detected.

E.3.2.1 Rx.Detect Requirements

- The re-timer's receiver terminations at both ports shall present high impedance to ground of $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ defined in Table 6-22 upon power-on. Note that a re-timer may not have the knowledge to which port a host or a device is connected upon power-on.
- The re-timer shall preserve its original receiver termination if the transition to this state is due to an error event. Refer to transition conditions to eSS.Inactive in LTSSM.
- The re-timer shall initiate the far-end receiver termination detection at both ports upon entry to this state. It shall perform the far-end receiver termination detection at least every 8 ms. Note that this is to ensure the receiver termination from host DFP is propagated to a peripheral device before the peripheral device times out from Rx.Detect and transition to eSS.Disabled. Refer to Section 7.5.3 for behavior of a peripheral device in Rx.Detect.
- The re-timer, upon detecting far-end low-impedance receiver termination ($R_{RX\text{-}DC}$) defined in Table 6-22, shall enable its low-impedance receiver termination ($R_{RX\text{-}DC}$) at its respective port to mirror the presence of its link partner.

- The re-timer shall forward Polling.LFPS it may receive in this state and start monitoring the Polling.LFPS exit handshake if both of the following two conditions are met.
    - The low-impedance receiver terminations (R_{RX-DC}) are detected at both ports.
    - The LFPS operating conditions are established at both ports.
- The re-timer shall start the tPollingLFPSTimeout timer upon receiving Polling.LFPS.
- The re-timer shall enable the transition path to Compliance Mode by default upon power-on.
- The re-timer shall conclude the far-end receiver termination detection at its port where Polling.LFPS is received and continue to perform the far-end receiver termination detection at its other port if Polling.LFPS is not received. A re-timer shall perform the following under this condition.
    - Upon start of forwarding Polling.LFPS at one direction, it shall start a 24 ms timer to monitor the absence of the Polling.LFPS at its other direction.
    - If the 24 ms timer times out and no Polling.LFPS is received, it shall terminate the Polling.LFPS forwarding and perform far-end receiver termination detection.
        - If the far-end low-impedance receiver termination is removed, the re-timer shall propagate the receiver termination state by presenting high impedance to ground of $Z_{RX-HIGH-IMP-DC-POS}$ defined in Table 6-22, stop forwarding the Polling.LFPS signal and reset the tPollingLFPSTimeout timer. Note that this implies that a peripheral device may have transitioned to eSS.Disabled.
        - If the far-end low-impedance receiver termination is detected, the re-timer shall resume forwarding the Polling.LFPS signal and restart the 24 ms timer. Note that this may be due to a temporary receiver termination mismatch between re-timers and their link partners, or due to the next transition path to Compliance Mode, or an error case. Note also that the tPollingLFPSTimeout timer shall continue while performing the far-end receiver termination detection.
- The re-timer shall forward and decode Warm Reset it may receive. The re-timer shall ensure the duration of forwarded Warm Reset meets the timing requirement defined in Section 6.9.3. Refer to Section E.3.1 for details. Note that the re-timer may also assign the port receiving Warm Reset as USP, and the port transmitting Warm Reset as DSP.

E.3.2.2 Exit from Rx.Detect

- A re-timer shall transition to Polling if Polling.LFPS is received at both ports.
- The re-timer shall enter Compliance Mode upon the first timeout of the tPollingLFPSTimeout timer after power-on.

E.3.3 eSS.Disabled

eSS.Disabled is an optional state where no eSS activity is enabled. The re-timer is at its lowest possible power state. Note that there is no defined mechanism for entry to and exit from eSS.Disabled. It is the responsibility of the implementation to manage eSS.Disabled based on its capabilities.

E.3.3.1 eSS.Disabled Requirements

- The re-timer shall present high impedance to ground of $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ defined in Table 6-22 at both ports.
- The re-timer shall be in its lowest power state.

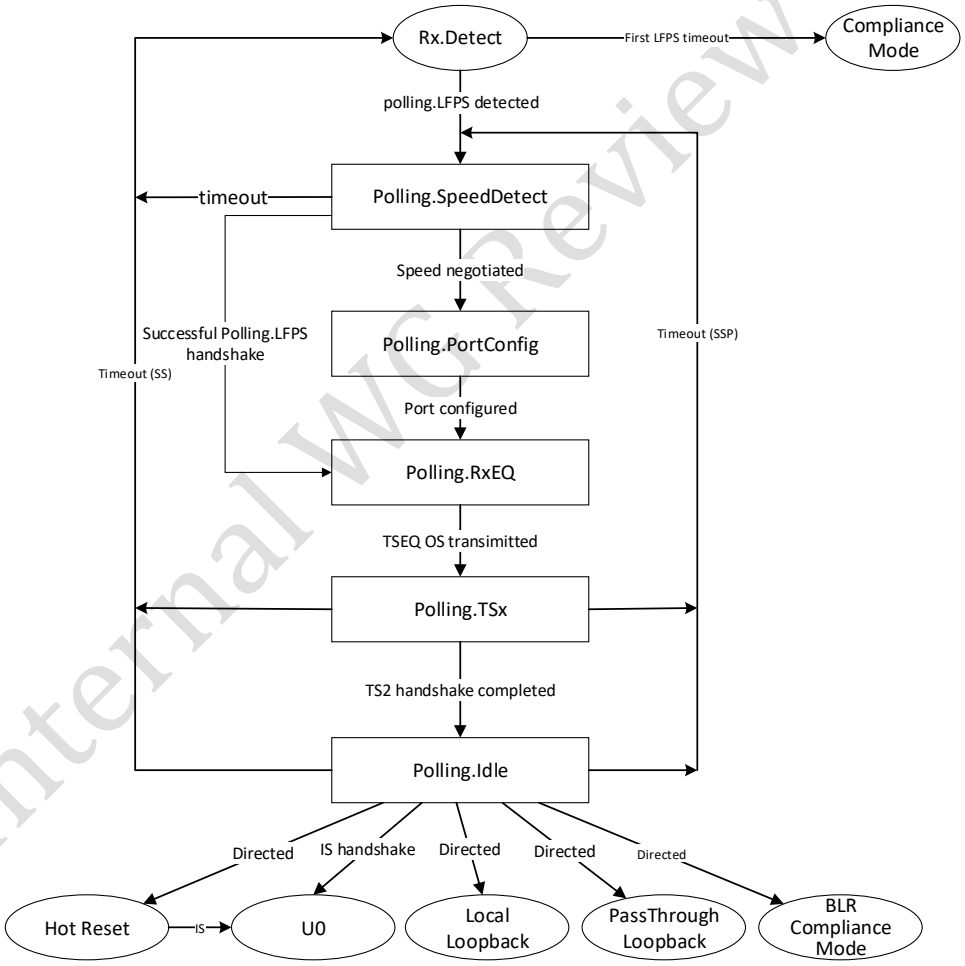
E.3.3.2 Exit from eSS.Disabled

- The re-timer shall transition to Rx.Detect upon direction.

E.3.4 Polling

Polling is a state for the re-timer to participate in speed negotiation, link training and to determine the state of operation upon exit from Polling. A simplified re-timer Polling substate machine is shown in Figure E-7. Note that the transition to Rx.Detect due to Warm Reset is not shown.

Figure E-7. Polling Substate Machine



E.3.4.1 Polling.SpeedDetect

Polling.SpeedDetect is a substate that covers the following substates in LTSSM.

- Polling.LFPS
- Polling.LFPSPlus

- Polling.PortMatch

The re-timer's responsibility in this substate includes:

- Forward the LFPS based signals include Polling.LFPS, SCD1/SCD2, and LBPM.
- Decode the LFPS signal including SCD1, SCD2, and LBPM to determine the negotiated data rate.

E.3.4.1.1 Polling.SpeedDetect Requirements

- The re-timer shall decode the following received LFPS signals and monitor the status and progression of LTSSM.
    - Polling.LFPS
    - SCD1/SCD2
    - LBPM
    - Warm Reset
- The re-timer shall forward the LFPS signals meeting the electrical and timing requirements defined in Section 6.9. The re-timer shall perform the following when forwarding the LFPS signals.
    - If the received signal is Polling.LFPS or SCD1/SCD2, the re-timer shall qualify between Polling.LFPS and SCD1/SCD2. The re-timer may buffer the maximum of one Polling.LFPS for implementation specific need.
    - If the received signal is Polling Warm Reset, it shall ensure that the forwarded Warm Reset meets the timing specification defined in Section 6.9. Note that if a re-timer does store and forward one Polling.LFPS, it is allowed to truncate the starting part of LFPS of Warm Reset, but the truncation shall be less than 20 µs.
- The re-timer shall participate the PHY capability negotiation between a hub DFP and a device UFP. It shall monitor and decode the received PHY Capability LBPM and perform the following.
    - A x1 only re-timer shall reset bits[7:4] of received PHY Capability LBPM.
    - A re-timer shall monitor [b3:b2] of the received PHY Capability LBPM. If the highest port capability defined in [b3:b2] is not "00" or "01", it shall update [b3:b2] to match its highest data rate before forwarding the PHY Capability LBPM.
    - If the re-timer's PHY capability is lower than the PHY capability specified in the received PHY Capability LBPM, it shall modify the received PHY Capability LBPM to match its highest PHY capability.
    - If the re-timer's PHY capability is equal to or higher than the PHY capability specified in the received PHY Capability LBPM, it shall forward the received PHY Capability LBPM as is.
    - The re-timer may store, update, and forward the received LBPM with maximum delay of one LBPM.
    - If the received LBPM does not match PHY Capability LBPM, i.e. bits[1:0] of the received LBPM is not "00", but "01", or "10", or "11", the re-timer shall forward the LBPM with the rest of the bit field reset to "00,0000". Note that this requirement does not apply when the re-timer is Polling.PortConfig.
- The re-timer shall continue the tPollingLFPSTimeout timer upon entry to this sub-state.

- The re-timer shall start the tPollingLBPMLFPSTimeout timer upon observing LBPM.
- The re-timer shall implement a tPollingSCDLFPSTimeout timer at both ports to monitor the absence of LFPS signal at both ports after the completion of SuperSpeed Polling.LFPS handshake at its receivers.
- The re-timer shall disable the tPollingSCDLFPSTimeout timer upon detecting successful SCD2 handshake.

E.3.4.1.2 Exit from Polling.SpeedDetect

- The re-timer shall transition to Polling.RxEQ for SS operation if the following two conditions are met.
  - Re-timer successfully observed on each port that at least four consecutive Polling.LFPS bursts are transmitted after receiving one.
  - Upon timeout of the tPollingSCDLFPSTimeout timer~~.~~ on either one of the ports.
- The re-timer shall transition to Polling.PortConfig if it has observed successful LBPM handshake for port match.
- The re-timer shall transition to Rx.Detect if one of the following conditions is met.
  - Warm Reset is detected.
  - The tPollingLBPMLFPSTimeout timer has expired.
  - The tPollingLFPSTimeout timer has expired and the conditions to transition to Polling.RxEQ or Polling.PortMatch are not met. Note that this condition also applies to the first tPollingLFPSTimeout timer timeout upon power-on.

E.3.4.2 Polling.PortConfig

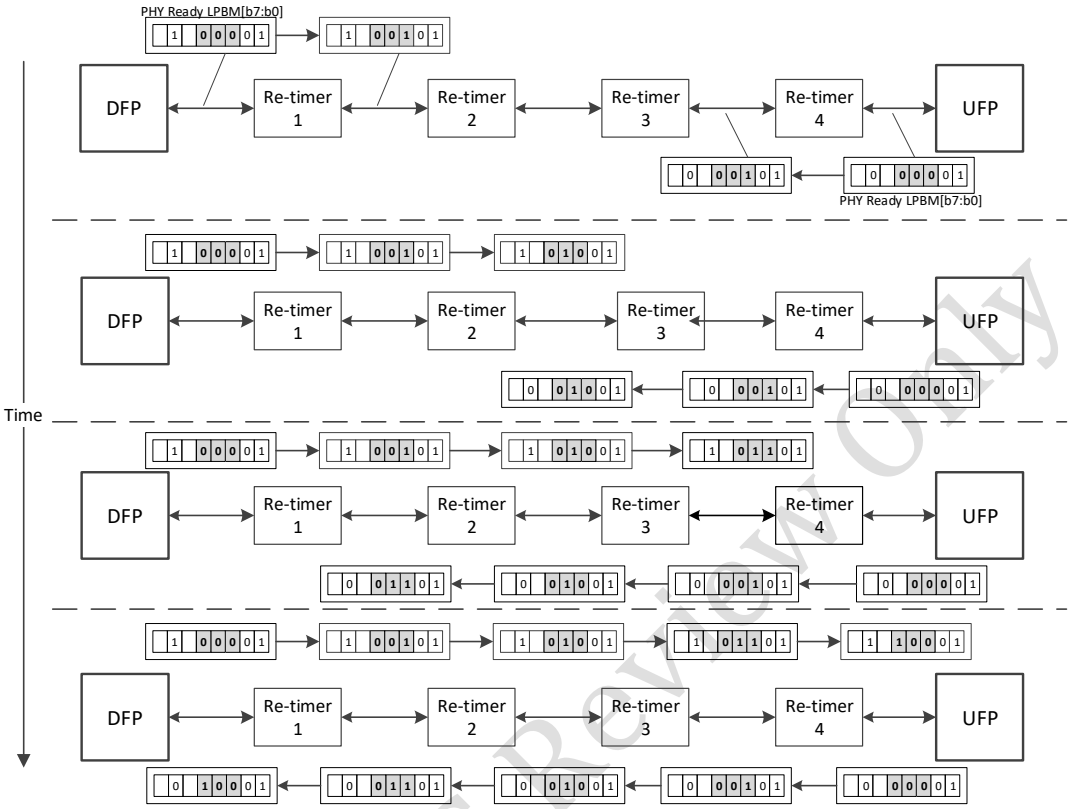
Polling.PortConfig is a substate for the re-timer to configure itself to the negotiated data. The operation of the re-timer is the same. It is also the substate for the re-timer to announce its presence if it is in x2 operation.

E.3.4.2.1 Mechanism for Re-timer Presence Announcement

The re-timer presence announcement applies to x2 operation only. The purpose of the re-timer presence announcement is for a port to determine the number of re-timers between the DFP and UFP such that a port ~~may~~ adaptively determine the number of SKP OS to be inserted in Gen 2x2 operation. The re-timer presence announcement also provides a mechanism in future revisions where DFP may want to address a re-timer for purpose of performing capability discovery and configuration.

Figure E-8 illustrates the re-timer presence announcement during Polling.PortConfig where the DFP and UFP are exchanging the PHY Ready LBPM with bit 6 of the PHY Ready LBPM from the DFP asserted.

Figure E-8. Illustration of Re-timer Presence Announcement



Refer to Table 7-13, in x2 operation, bits [4:2] of the PHY Ready LBPM is specified for re-timers to announce their presence. This is achieved by a re-timer incrementing bits [4:2] upon receiving the PHY Ready LBPM. When DFP and UFP transmit the PHY Ready LBPM, bits [4:2] are set to "000". When re-timer 1 received the PHY Ready LBPM from DFP, it will increment bits [4:2] by one, and passes it to re-timer 2. Re-timer 2, upon receiving the PHY Ready LBPM from re-timer 1, will perform the same by incrementing bits [4:2] by one, and again passes it to re-timer 3. This process continues until all re-timers complete the PHY Ready LBPM reception, bits [4:2] increment, and forwarding. Upon receiving the PHY Ready LBPM, UFP may decode bits [4:2] to determine how many re-timers that may be present between DFP and UFP. Note that the values of bits [4:2] of the PHY Ready LBPM also implies the re-timer relative proximity to DFP. For example, the value of bits [4:2] of the PHY Ready LBPM re-timer 2 forwarded is "010". This means there is one re-timer, or two link segments between DFP and re-timer 2. Note also that the same process happens from UFP to DFP. Once DFP received the PHY Ready LBPM, it may determine the number of re-timers between DFP and UFP. Furthermore, the unique value of bits [4:2] each re-timer asserted while forwarding the PHY Ready LBPM from DFP to UFP, also represents a unique address index such that DFP may use in future revisions to communicate with each re-timers.

E.3.4.2.2 Polling.PortConfig Requirements

- The re-timer shall not forward any PHY Ready LBPMs before it is ready for training at both ports. In x2 operations, the re-timer shall get both lanes ready for training. This include, for example, enabling the receiver termination at its non-Configuration Lane that may be disabled during the prior link substates.

- The re-timer shall monitor and forward the received LBPMs until a successful handshake is reached. Note that the forwarded LBPMs shall meet the electrical and timing requirements defined in Section 6.9.
- The re-timer shall start the tPollingLBPMLFPSTimeout timer upon entry to this substate.
- In x2 operation, the re-timer shall participate the re-timer presence announcement defined in Section E.3.4.2.1. A re-timer shall announce its presence by forwarding the received PHY Ready LBPM with bits [4:2] incremented by one. Note that the re-timer may determine the source of the PHY Ready LBPM based on bit 6. Refer to Table 7-13 for details.
- In x2 operation, after completing the re-timer presence announcement, the re-timer shall perform one of the following based on bit 7 of the PHY Ready LBPM from the DFP.
    - If it is asserted, it shall reset the tPollingLBPMLFPSTimeout timer, remain in this substate, forward the received LBPM message as is including the PHY Ready LBPM, and continue to monitor the PHY Ready LBPM handshake. Note that re-timer may observe LFPS electrical idle during the operation. The re-timer may store and forward one LBPM.
    - If it is de-asserted, it shall participate the PHY Ready LBPM handshake and prepare to exit to Polling.RxEQ.
- In x2 operation, the re-timer shall start a 60 µs LFPS EI timer to monitor the absence of LFPS after observing the successful PHY Ready LBPM handshake.

E.3.4.2.3 Exit from Polling.PortConfig

- In single-lane operation, the re-timer shall transition Polling.RxEQ if it has observed successful PHY Ready LBPM handshake.
- In x2 operation, the re-timer shall transition Polling.RxEQ if it has observed successful PHY Ready LBPM handshake with bit-7 of the PHY Ready LBPM from DFP de-asserted and the 60 µs LFPS EI timer has expired.
- The re-timer shall transition to Rx.Detect if one of the following conditions is met.
    - Warm Reset is detected.
    - The tPollingLBPMLFPSTimeout timer has expired.

E.3.4.3 Polling.RxEQ

Polling.RxEQ is a substate for eSS receiver equalization training. The training mechanism is the same as defined in LTSSM except the exit criteria.

E.3.4.3.1 Polling.RxEQ Requirements

- The lane polarity detection and correction for SS operation shall be enabled.
- The re-timer shall transmit the number of TSEQ ordered set (OS) defined in Section 6.4 while performing its receiver equalization training and clock data recovery.
- The re-timer shall be ready for TS1 OS detection upon completion of its receiver equalization training.
- A bit-level re-timer shall transmit TSEQ OS with its transmitter meeting the electrical and timing requirements defined in Chapter 6. Note that a bit-level re-timer shall have its SSC disabled while transmitting TSEQ OS.
- The re-timer shall forward the LFPS signal it has detected.

E.3.4.3.2 Exit from Polling.RxEQ

- The re-timer shall transition to Polling.TSx once it has transmitted the number of TSEQ OS defined in Section 6.4.
- The re-timer shall transition to Rx.Detect if Warm Reset is detected.

E.3.4.4 Polling.TSx

Polling.TSx is a substate where the re-timer tracks the TS1/TS2 OS to achieve end to end symbol/block alignment. This is also a substate for bit-level re-timers to perform sequential clock and OS switching.

E.3.4.4.1 Mechanism of the Sequential Clock Switching for Cascaded Bit-Level Re-timer

The bit-level re-timer architecture and its specific operation mechanism is defined to only support Gen 1x1 operation.

Sequential clock switching refers to a mechanism of clock switching in the ordered progression from the last re-timer to the leading re-timer, where multiple bit-level re-timers are cascaded between the host and device. This is illustrated in Figure E-9. In the simplex link from the host to device, RT4 is the last re-timer, and its preceding re-timer is RT3. RT1 is leading re-timer, and its following re-timer is RT2. Similarly in the opposite simplex link from the device to host, RT1 is the last re-timer, and its preceding re-timer is RT2. RT4 is the leading re-timer, and its following re-timer is RT3. The clock switching process is described in this section.

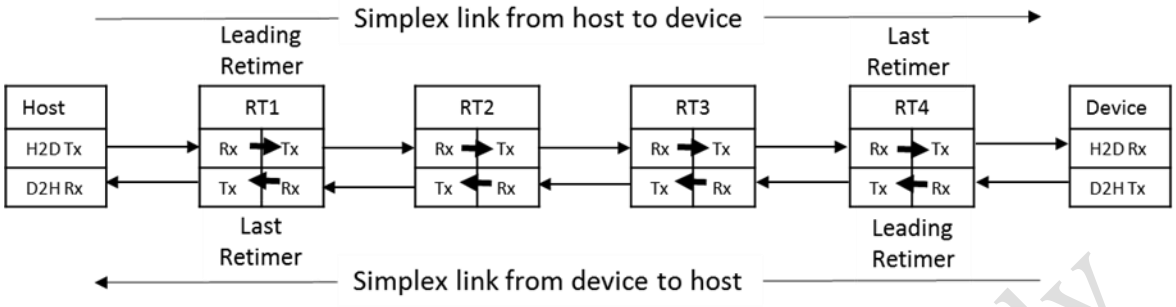
In the simplex link from host to device, the last bit-level re-timer RT4 will first perform its clock switching from its local transmit clock that has SSC disabled to the recovered clock from RT3 that also has SSC disabled. Because SSC are both disabled, RT4 only needs to achieve the receiver bit/symbol lock and perform the clock switching within 600-ppm, thus facilitating fast and robust clock switching. After RT4 completes its clock switching, RT3 will switch from its local clock to the recovered clock from RT2. Since RT4 is tracking RT3's clock, once RT3 completes its clock switching, RT4 is tracking RT2's clock through RT3. This process continues until RT1 completes its clock switching, and RT4 is now tracking RT1's clock through RT3 and RT2. Note that RT1 is switching from its local clock with SSC disabled to recovered clock from the host that has SSC enabled.

In the opposite simplex link from the device to host, the same clock switching process from RT1 to RT4 is performed simultaneously.

Once a bit-level re-timer completes clock switching at both simplex links, it will perform the OS switching to complete its clock and OS switching.

Note that this operation also applies to bit-level re-timers when in Recovery.TSx.

Figure E-9. Sequential Bit-Level Re-timer Clock Switching



To facilitate a successful sequential clock switching among bit-level re-timers two ordered sets, TS1A OS and TS1B OS, are defined based on TS1 OS. Note that the definition of TS1A OS and TS1B OS still serve the function to train the host and device but prevent them from declaring the successful exit handshake from Polling.Active before all bit-level re-timers complete the clock and OS switching. TS1A OS and TS1B OS definitions are shown in Table E-1 and Table E-2. Note that symbols 4-9 of the ordered sets are TS1A OS and TS1B OS identifiers. TS1A OS is defined to indicate that a bit-level re-timer is either in clock recovery state, or in a state that the received clock is recovered, and it is waiting for its following bit-level re-timer to complete the clock switching. TS1B OS is defined for a bit-level re-timer to indicate to its preceding bit-level re-timer that it has completed the clock switching. Note that receiving TS1 OS is also an indicator that the bit-level re-timer is either connected directly to the host or device or a SRIS re-timer, or its following bit-level re-timer has completed clock and OS switching.

- A bit-level re-timer shall declare successful receiver training if eight consecutive and identical TS1A OS or TS1B OS or TS1 OS are received.
- A bit-level re-timer shall declare successful TS1B OS reception if one TS1B OS is received.

Table E-1. Gen 1 TS1A Ordered Set (TS1A OS)

Symbol Number	Encoded Values	Description
0 – 3	K28.5	COM (Comma)
4 – 9	D18.1	TS1A identifier
10 – 15	D10.2	TS1 Identifier

Table E-2. Gen 1 TS1B Ordered Set (TS1B OS)

Symbol Number	Encoded Values	Description
0 – 3	K28.5	COM (Comma)
4 – 9	D10.6	TS1B identifier
10 – 15	D10.2	TS1 Identifier

A bit-level re-timer shall perform the clock and OS switching based on the following steps. Refer to Figure E-11 as an example process of RT1 and RT2 completing their clock switching in the simplex link from the device to the host.

- Upon entry to Polling.TSx, a bit-level re-timer shall transmit TS1A OS based on its local transmit clock at both ports with SSC disabled. It shall train its receiver at both ports based on TS1 OS, TS1A OS or TS1B OS while transmitting TS1A OS.

- Upon declaring successful receiver training, a bit-level re-timer shall perform one of the following.
    - If it has detected TS1 OS or TS1B OS at one simplex link, it shall perform the clock switching at its other simplex link and comply with the electrical and timing requirements defined in Chapter 6~~, specifically in terms of tCDR_SLEW_MAX for Gen 1 operation, and SSCdfdt for Gen 2 operation.~~. It shall continue the TS1A OS transmission at both ports. Note that a bit-level re-timer may receive TS1 OS and/or TS1B OS at both ports. Under this situation, a bit-level re-timer shall perform the clock switching at both simplex links.

      ~~Note that a bit-level re-timer may monitor the clock offset between the recovered clock and its local reference clock, and attempt to perform the clock switching when the clock offset is small. A bit-level re-timer shall expect that the frequency range of a host or device is either within +300ppm to –5300ppm, or within –1700ppm to –5300ppm if a RF-friendly SSC profile is employed. It is desired that a bit-level re-timer to monitor the recovered clock and determine its frequency range before setting the clock switching point.~~
    - If it has detected TS1A OS, it shall continue the TS1A OS transmission while waiting for incoming TS1 OS or TS1B OS.

- During the clock switching, a bit-level re-timer shall attempt to minimize the frequency jump when switching from its transmit clock based on the local reference clock to the transmit clock based on the recovered clock. This is to maximally ensure its following link partner to maintain its CDR lock during the clock switching. A bit-level re-timer shall comply with the short-term SSCdf/dt clock switching requirement specified in Table E-3.

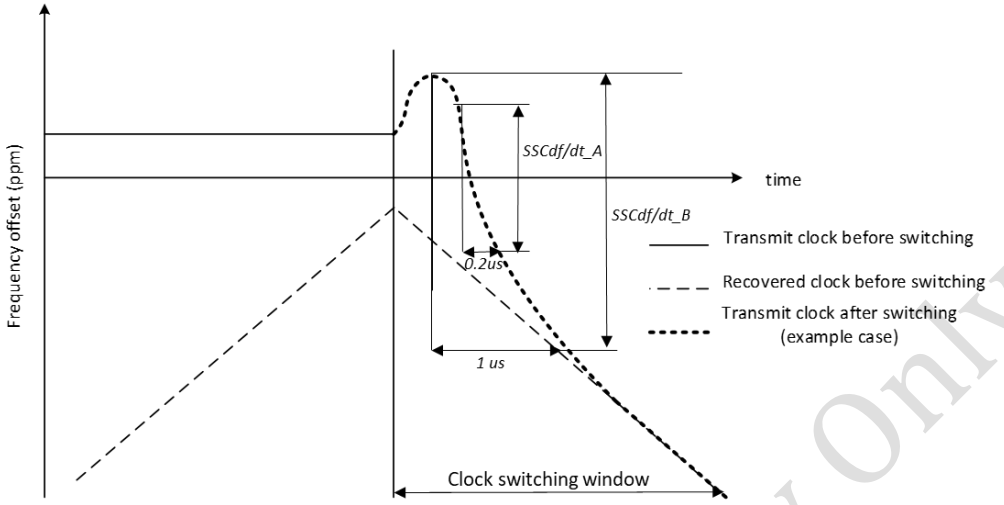
Table E-3. Bit-Level Re-timer Short-Term Clock Switching Requirement[1]

	Frequency offset (ppm)	Time interval (µs)	Comments
SSCdf/dt_A[2]	≤ 1400	0.2	Waveform under test is defined as window of switching point (+/–) * 0.5/$t_{SSC\_MOD\_RATE}$
SSCdf/dt_B[2]	≤ 2200	1.0	

Note 1: The requirements are outside the specification defined , thus interoperability may not be formally guaranteed but are strongly believed to be adequate.

Note 2: Refer to Figure E-10 for SSCdf/dt_A and SSCdf/dt_B definition.

Figure E-10. Definition of SSCdf/dt_A and SSCdf/dt_B



- Upon completing the clock switching in one simplex link, a bit-level re-timer shall transmit TS1B OS in its other simplex link to signal its preceding re-timer.
- Upon completing the clock switching at both simplex, a bit-level re-timer shall perform the ordered set switch. The symbol boundary shall be preserved when switching from the local TS1B OS to the received TS1 OS or TS1B OS.

Shown in Figure E-12 is an example of four bit-level re-timers performing the clock switching at both simplex.

Figure E-11. Sequential Bit-Level Re-timer Clock Switching Based on TS1A OS and TS1B OS

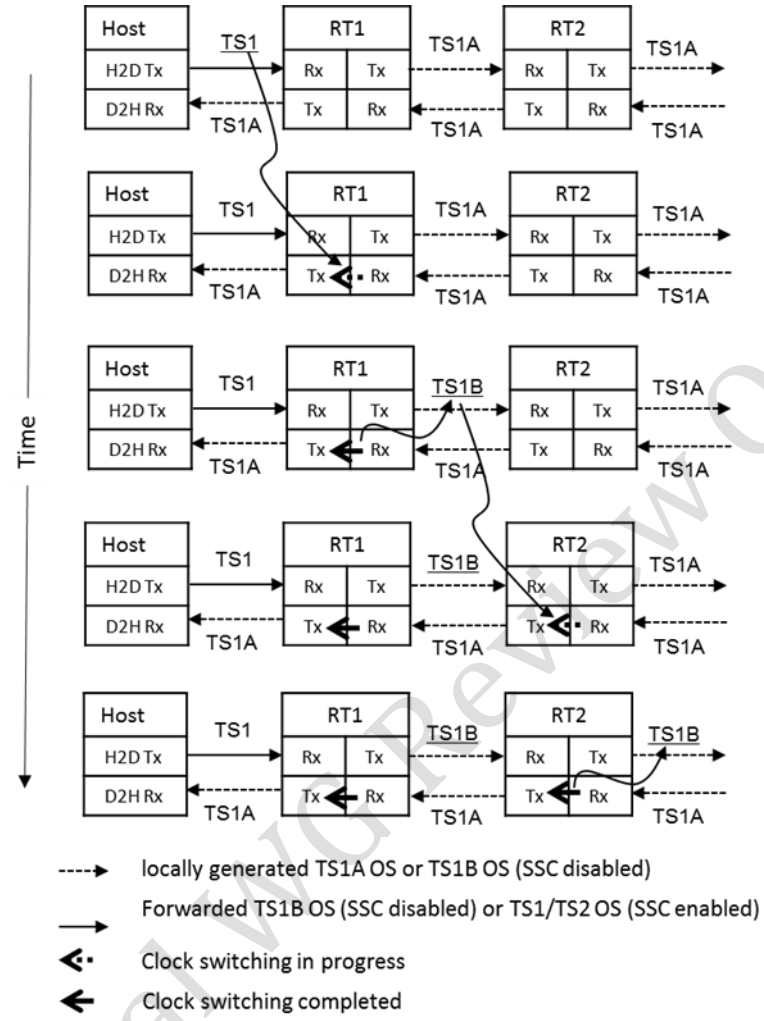
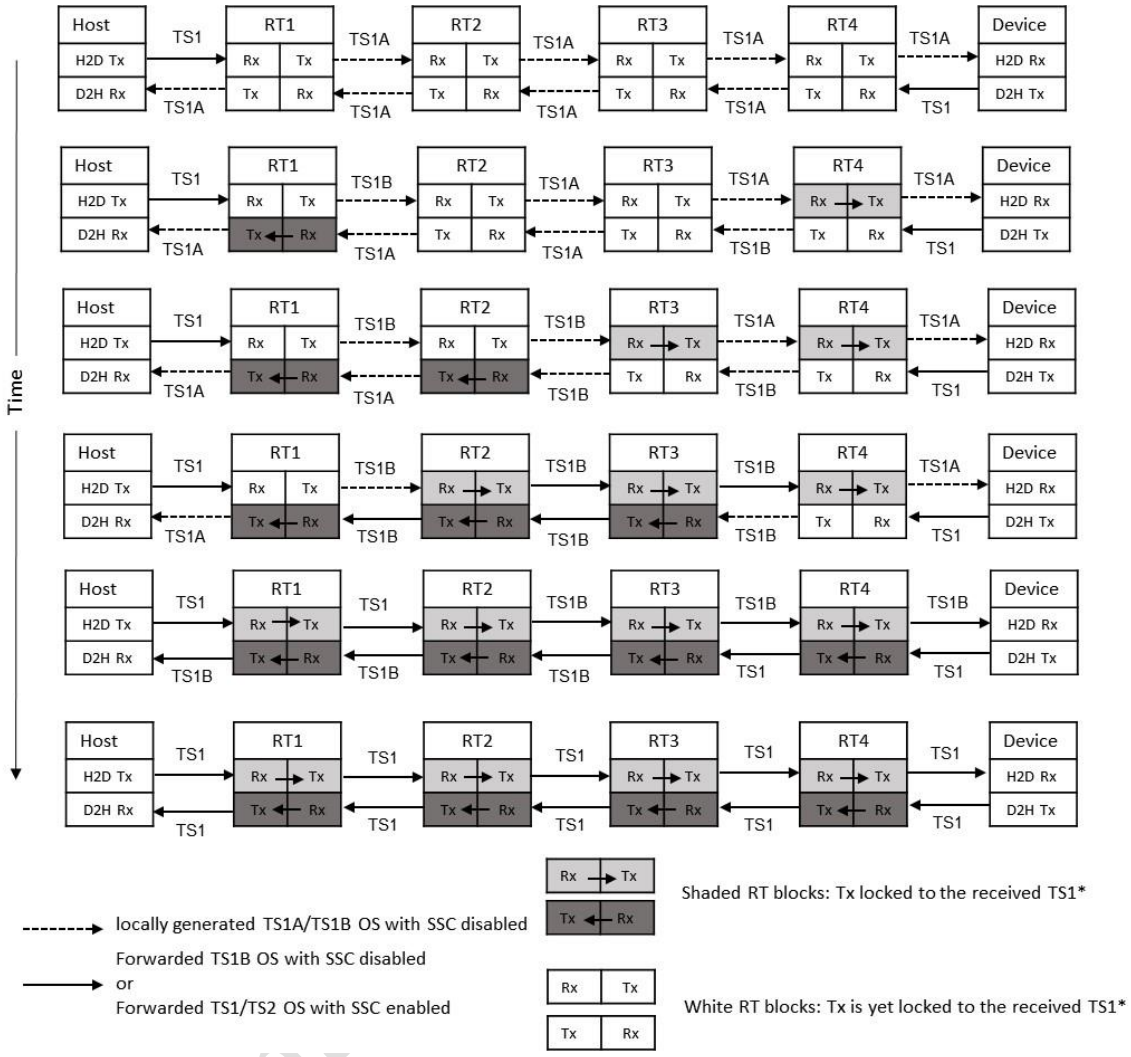


Figure E-12. Example of Four Bit-Level Re-timer Performing Sequential Clock Switching



E.3.4.4.2 Polling.TSx Requirements

- The lane polarity inversion detection and correction shall be completed before forwarding.
- The re-timer shall monitor the status and progression of LTSSM.
- Upon entry to this substate, a SRIS re-timer shall either transmit the local TS1 OS if received TS1 OS is not detected, or forward the received TS1 OS if it's already recovered.
- A SRIS re-timer shall preserve the OS boundary and in Gen 2 mode, maintain the scrambler synchronization when switching from the local TS1 OS to recovered TS1 OS or TS2 OS. A SRIS re-timer shall not forward any TS2 OS until both ports are ready to forward TS1/TS2 OS.
- A SRIS re-timer shall perform the clock offset compensation based on the following.
  - For SS operation, it shall perform the clock offset compensation as defined in Section E.4.1.

- For SSP operation, it shall perform the clock offset compensation as defined in Section 6.4.3.

- A bit-level re-timer shall perform its link training and complete its clock and OS switching based on Section E.3.4.4.1.
- The re-timer in SSP operation shall monitor and forward LBPMs upon detection. Note that this situation may happen when the host or device fail the training and timeout to Polling.PortMatch to re-negotiate the next link speed.
- The re-timer shall start the tPollingActiveTimeout timer upon entry to this substate. This timer shall be reset and disabled upon observing successful exit handshake from Polling.Active. Note that the re-timer shall also disable this timer and progress forward if it has observed TS2 OS from both ports but has not observed a successful TS1 OS exit handshake. This may be a corner case where a decoding error could happen within the re-timer.
- The re-timer shall start the tPollingConfigurationTimeout timer upon observing TS2 OS at both ports. Note that a host and device may not exit from Polling.Active simultaneously. For re-timers, observing TS2 OS at both ports is an indication that both the host and device have entered Polling.Configuration.

E.3.4.4.3 Exit from Polling.TSx

- The re-timer shall transition to Polling.Idle upon observing successful TS2 handshake.
- The re-timer in SSP operation shall disable its eSS transceivers and transition to Polling.SpeedDetect if either one of the following conditions is met.
  - Upon the expiration of the tPollingActiveTimeout timer and no successful TS1 OS handshakes have been observed.
  - Upon the expiration of the tPollingConfigurationTimeout timer and no successful TS2 OS handshakes have been observed.
  - LBPM is detected at both ports.
- The re-timer in SS operation shall disable its SS transceivers and transition to Rx.Detect if either one of the following two conditions is met.
  - Upon the expiration of the tPollingActiveTimeout timer and no successful TS1 OS handshake has been observed.
  - Upon the expiration of the tPollingConfigurationTimeout timer and no successful TS2 OS handshake has been observed.
- The re-timer shall transition to Rx.Detect if Warm Reset is detected.

E.3.4.5 Polling.Idle

Polling.Idle is a substate where the re-timer decodes TS2 OS and determines its next operation state.

E.3.4.5.1 Polling.Idle Requirements

- The re-timer shall decode the link configuration field in TS2 OS and configure itself to the corresponding operation state.
- The re-timer in SSP operation shall monitor and forward LBPMs upon detection.
- The re-timer shall start the tPollingIdleTimeout timer to monitor the progression of LTSSM.

E.3.4.5.2 Exit from Polling.Idle

- The re-timer shall transition to U0 if either one of the following conditions is met.
  - Successful idle symbol handshake is observed.
  - A link command is observed.
- The re-timer shall transition to PassThrough Loopback if the Loopback bit (bit 2) in the link configuration field is asserted and the Compliance bit (bit 5) in the link configuration field is de-asserted.
- The re-timer shall transition to BLR Compliance Mode if the Loopback bit (bit 2) in the link configuration field and the Compliance bit (bit 5) in the link configuration field are both asserted.
- The re-timer shall transition to Local Loopback as the loopback slave if the re-timer loopback bit (bit 4 in the link configuration field) is asserted. Note that it is illegal to have both bit4 and bit 2 asserted. If both bits are asserted, the re-timer shall give priority to PassThrough Loopback.
- The re-timer shall transition to Hot Reset if the Reset bit is asserted.
- The re-timer in SSP operation shall disable its eSS transceivers and transition to Polling.SpeedDetect if either one of the following two conditions is met.
  - Upon the expiration of the tPollingIdleTimeout timer and no successful idle symbol handshake has been observed.
  - LBPMs is detected at both of its ports.
- The re-timer in SS operation shall disable its SS transceivers and transition to Rx.Detect upon the expiration of the tPollingIdleTimeout timer and no successful idle symbol handshake has been observed.
- The re-timer shall transition to Rx.Detect if Warm Reset is detected.

E.3.5 Compliance Mode

Compliance Mode is to test re-timer's transmitter characteristics based on a local reference clock.

E.3.5.1 Compliance Mode Requirements

- Upon entry to the substate, the re-timer shall transmit CP0 on its transmitter. An x2 capable re-timer shall meet the additional scrambler seed requirement on each lane as defined in Section 6.13.5.
- An x2 re-timer shall monitor the LFPS signal at its Configuration Lane.
  - If the received signal is Ping.LFPS, it shall advance the compliance pattern accordingly. An x2 capable re-timer shall advance the compliance pattern on both lanes.
  - If the received signal is WarmReset, it shall conclude the compliance test
- The re-timer shall monitor the LFPS signal at both ports. Note that the re-timer may receive Ping.LFPS at the port in the compliance test, or WarmReset at either port if the compliance test is concluded.
- The re-timer shall configure the port not receiving Polling.LFPS in Rx.Detect for the transmitter compliance test~~,~~ and keep the transmitter at its port receiving Polling.LFPS in electrical idle.

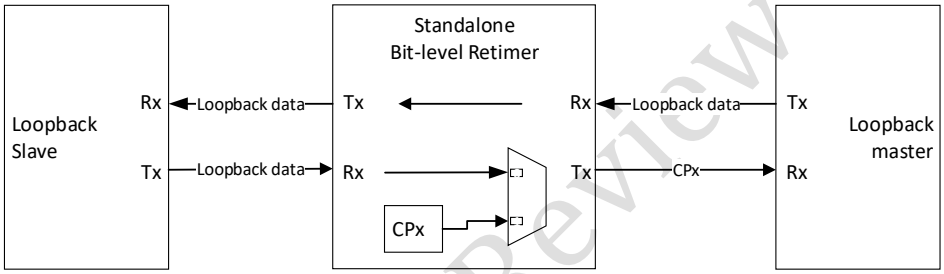
E.3.5.2 Exit from Compliance Mode

- The re-timer shall transition to Rx.Detect if WarmReset is detected or if directed.

E.3.6 BLR Compliance Mode

BLR Compliance Mode is a bit-level re-timer specific test mode for transmitter compliance test. It applies to Gen 1x1 operation only. Shown in Figure E-13 is a test setup for a standalone bit-level re-timer Compliance Mode. Note that the loopback master may be the compliance test handler capable of sending the bit-level re-timer into transmitter compliance test, directing the bit-level re-timer to advance compliance patterns, and analyzing compliance patterns. The loopback slave can either be a compliant host or device, or another compliance test handler. Also note that this configuration applies to transmitter compliance test of a re-timer in the captive environment. For transmitter compliance test of the re-timers in an active cable, it is implementation specific to configure the re-timers, with one under test in BLR Compliance Mode, and the other in PassThrough Loopback.

Figure E-13. Standalone Bit-Level Re-timer Compliance Test Setup



E.3.6.1 BLR Compliance Mode Requirements

- A bit-level re-timer shall monitor the LFPS signal at both ports.
- It shall set its data path from the loopback master to the loopback slave in PassThrough Loopback.
- It shall set its data path from the loopback slave to the loopback master in transmitter compliance test by transmitting the locally generated compliance pattern based on the recovered clock from the loopback slave.
- It shall advance the compliance pattern if four consecutive SKP OS are detected at forwarding data path. It shall advance sequentially from CP0 to CP8, and back to CP0.

E.3.6.2 Exit from BLR Compliance Mode

- The re-timer shall transition to Rx.Detect if WarmReset is detected or if directed.

E.3.7 U0

U0 is the normal operational state where packets are forwarded by the re-timer in both directions.

E.3.7.1 U0 Requirements

- The re-timer shall monitor and decode the link command to participate in re-timer and link power management.

- The re-timer shall determine its port orientation towards a host downstream port or device upstream port.
- The re-timer shall decode U2 Inactivity timeout LMP from host, when acknowledged by device with ACK.
- A SRIS re-timer shall perform the clock offset compensation as defined in Section E.4.
- The re-timer shall not initiate entry to Recovery due to bit errors at its inbound traffic.
- The re-timer shall start a 1 ms timer (tU0RecoveryTimeout) to monitor the absence of link command at each port. This timer will be reset and restarted every time a link command is received. Note that a re-timer may lose receiver lock before the timer expires. Under this condition, a re-timer may transmit any scrambled idle symbols based its local scrambler. A bit-level re-timer may transmit idle symbols or TS1A OS with its local reference clock.

E.3.7.2 Exit from U0

- The re-timer shall transition to U1 upon successful completion of LGO_U1 entry sequence. Refer to Section 7.2.4.2 for details.
- The re-timer shall transition to U2 upon successful completion of LGO_U2 entry sequence. Refer to Section 7.2.4.2 for details.
- The re-timer shall transition to U3 upon successful completion of LGO_U3 entry sequence. Refer to Section 7.2.4.2 for details.
- The re-timer shall transition to Recovery if either one of the following conditions is met.
    - Upon observing TS1 OS, TS2 OS, TS1A OS, or TS1B OS.
    - Upon timeout of the tU0RecoveryTimeout timer.
- The re-timer shall transition to Rx.Detect if Warm Reset is detected. Refer to Section E.3.1 for Warm Reset detection.

E.3.8 U1

U1 is a low power state where no packets are observed and the re-timer is in a standby state.

E.3.8.1 U1 Requirements

- The re-timer shall distinguish the received LFPS signal to determine if it is Ping.LFPS or U1 LFPS exit signal.
- The re-timer shall either forward or regenerate Ping.LFPS meeting the timing requirement defined in Table 6-30. Note that if a re-timer forwards Ping.LFPS, it shall be prepared that the received Ping.LFPS meet only the minimum Ping.LFPS timing requirement defined in Table 6-30. Any distortion introduced by the re-timer may lead to non-compliant Ping.LFPS.
- A captive re-timer shall perform the U1 LFPS exit handshake meeting the timing specification defined in Section 6.9.2. This is measured at the connector side.
- The re-timers in active cable shall initiate simultaneous U1 LFPS exit handshake at both sides of its connectors and meet the timing specification defined in Section 6.9.2. This is defined by re-timers performing the following operation.
    - As LP2 defined in Section 6.9.2 responding to the U1 LFPS exit handshake.

  - As LP1 defined in Section 6.9.2 initiating the U1 LFPS exit handshake within 500 ns at the other side of the connector upon detecting U1 LFPS exit signal.

- A re-timer may receive Polling.LFPS from a host while in U1. This is a corner case where a host may declare device disconnect earlier than a re-timer. Before a re-timer declares device disconnect, a host may transition from U1 to Rx.Detect declaring a new event of device connect, and subsequently transition to Polling transmitting Polling.LFPS signal. A re-timer shall perform one of the following.
  - If a re-timer forwards LFPS signal in U1 and determines that it is Polling.LFPS, it shall stop forwarding the LFPS signal, and transition to Rx.Detect.
  - If a re-timer performing simultaneous U1 LFPS exit treats the LFPS burst of the first Polling.LFPS signal as U1 LFPS exit signal from LP1, it may initiate simultaneous U1 LFPS exit towards device as LP1, while acknowledging to host with U1 LFPS exit handshake as LP2. It shall be expected that its UFP LTSSM may be in Recovery, and its DFP LTSSM still in U1. If it has determined the received LFPS signal is Polling.LFPS, it shall transition to Rx.Detect.
- The re-timer shall distinguish between U1 LFPS exit handshake and Warm Reset based on specification defined in Section E.3.1.
- The re-timer shall enable an U2 inactivity timer upon entry to this state if the U2 inactivity timer has a non-zero timeout value between 0x01H and 0xFEH. It shall set its timeout value to be at least 500 µs more than the value defined in the U2 inactivity timeout LMP. Note this is to make sure that re-timer remains in U1 until the device has entered U2 and no Ping.LFPS is to be transmitted. Refer to Section 10.6.1 for PM timer accuracy requirement.
- The re-timer shall enable a 300 ms timer (tU1PingTimeout). This timer will be reset and restarted when a Ping.LFPS is received.
- In x2 operation, the transmitter DC common mode voltage of the non-Configuration Lane shall be also within specification ($V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$) defined in Table 6-19 on each both lanes. The receiver's low-impedance receiver termination ($R_{RX\text{-}DC}$) defined in Table 6-22 shall also be maintained on the non-Configuration Lane.

E.3.8.2 Exit from U1

- The re-timer shall transition to Recovery upon successful completion of a LFPS handshake meeting the U1 LFPS exit handshake signaling in Section 6.9.2 and additional conditions defined in Section E.3.1.
- The re-timer shall transition to U2 upon the timeout of the U2 inactivity timer.
- The re-timer shall transition to Rx.Detect if one of the following three conditions is met.
  - Upon the 300 ms timer (tU1PingTimeout) expiration and removal of the receiver termination at its own corresponding port mirroring the far-end receiver termination.
  - Upon detecting Warm Reset. Refer to Section E.3.1 for Warm Reset detection.
  - Upon the 2 ms LFPS handshake timer timeout (tNoLFPSResponseTimeout) and a successful LFPS handshake meeting the U1 LFPS exit handshake signaling in Section 6.9.2 is not achieved.

- The re-timer shall transition to Rx.Detect if Polling.LFPS signal is detected.

E.3.9 U2

U2 is a link state where more power saving is allowed for the re-timer as compared to U1, but with an increased exit latency. The operation of the re-timer is the same as is defined in LTSSM with a few exceptions that are described in the following subsections.

E.3.9.1 U2 Requirements

- A captive re-timer shall perform the U2 LFPS exit handshake meeting the timing specification defined in Section 6.9.2. This is measured at the connector side.
- The re-timers in active cable shall initiate simultaneous U2 LFPS exit handshake at both sides of its connectors and meet the timing specification defined in Section 6.9.2. This is defined by re-timers performing the following operation.
  - As LP2 defined in Section 6.9.2 responding to the U2 LFPS exit handshake.
  - As LP1 defined in Section 6.9.2 initiating the U2 LFPS exit handshake within 2 ms at the other side of the connector upon detecting U2 LFPS exit signal.
- The re-timer shall distinguish between U2 LFPS exit handshake and Warm Reset based on specification defined in Section E.3.1.
- The re-timer shall be prepared to detect Polling.LFPS signal. This is a corner case where a device may be reconnected within a period so short that the re-timer is not able to declare a disconnect event.

E.3.9.2 Exit from U2

- The re-timer shall transition to Recovery upon successful completion of a LFPS handshake meeting the U2 LFPS exit signaling defined in Section 6.9.2 and additional conditions defined in Section E.3.1.
- The re-timer shall transition to Rx.Detect if one of the following three conditions is met.
  - Upon detection of a far-end high-impedance receiver termination ($Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$) defined in Table 6-22 and removal of the receiver termination at its own corresponding port mirroring the far-end receiver termination.
  - Upon detecting Warm Reset. Refer to Section E.3.1 for Warm Reset detection.
  - Upon the 2 ms LFPS handshake timer timeout (tNoLFPSResponseTimeout) and a successful LFPS handshake meeting the U2 LFPS exit handshake signaling in Section 6.9.2 is not achieved.
- The re-timer shall transition to Rx.Detect if Polling.LFPS signal is detected.

E.3.10 U3

U3 is a link state where a device is put into a suspend state. Significant link and re-timer power can be saved. The re-timer operation is the same as is defined in LTSSM except that U3 LFPS exit is propagated.

E.3.10.1 U3 Requirements

- The re-timer shall perform propagated U3 LFPS exit, rather than simultaneous U1/U2 LFPS exit. This is primarily due to the fact that a port may not be ready to respond in time, and attempt U3 LFPS exit when it is ready. The re-timer shall perform the following to facilitate the propagated U3 LFPS exit.

- The re-timer shall implement a specific U3 standby (U3S) state such that upon observing the failure of the U3 LFPS exit handshake, it remains in U3S and is ready for another U3 LFPS exit handshake event. The re-timer shall implement the following while in U3S.
    - It shall maintain its operational state similar to U1.
    - It shall implement a one-second timer to monitor the absence of U3 LFPS exit event. The re-timer shall transition from U3S to U3 upon the one-second timer expiration and no U3 LFPS exit signal is observed.
- Upon detecting the U3 LFPS exit signal, the re-timer shall perform one of the following.
    - If it is capable of exiting from U3 and completing the subsequent link training, it shall propagate the received U3 LFPS exit signal from LP1 within 100 µs and forward the U3 LFPS exit signal from LP2 within 1 µs.
    - If it is not ready to exit from U3, it shall not forward the received U3 LFPS exit signal. The re-timer shall transition itself to U3S.
- The re-timer shall distinguish between U3 LFPS exit handshake and Warm Reset based on specification defined in Section E.3.1.
- The re-timer shall establish its eSS operating condition within 2 ms upon detecting and forwarding the U3 LFPS exit signal.
- Upon observing the successful completion of U3 LFPS exit handshake, if the re-timer has not established its eSS operating condition, it shall continue the LFPS transmission until it is ready for eSS operation.

  Note: the situation may exist that the re-timer's eSS operating condition may not be established upon successful U3 LFPS exit handshake. To make sure that the maximum gap of electrical idle between the LFPS transmission and the eSS transmission does not exceed the specification defined in Section 6.9.2, the re-timer shall continue the LFPS transmission until it is ready to transmit eSS signal.
- The re-timer shall be prepared to detect Polling.LFPS signal. This is a corner case where a device may be reconnected within a period so short that the re-timer is not able to declare a disconnect event.

E.3.10.2 Exit from U3

- The re-timer shall transition to Recovery if the following two conditions are both met.
    - Upon observing the successful completion of the U3 LFPS exit handshake meeting the U3 wakeup signaling defined in Section 6.9.2 and additional conditions defined in Section E.3.1.
    - The re-timer is ready for eSS operation.
- The re-timer shall remain in U3S upon failure to achieve a successful U3 LFPS exit handshake meeting the U3 wakeup signaling in Section 6.9.2.
- The re-timer shall transition to Rx.Detect if one of the following conditions is met.
    - Upon detection of a far-end high-impedance receiver termination ($Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$) defined in Table 6-22 and removal of the receiver termination at its own corresponding port mirroring the far-end receiver termination.
    - Upon detecting Warm Reset. Refer to Section E.3.1 for Warm Reset detection.
- The re-timer shall transition to Rx.Detect if Polling.LFPS signal is detected.

E.3.11 Recovery

The re-timer operations in Recovery are largely the same as its operations in Polling.TSx, and Polling.Idle. Recovery contains two substates, Recovery.TSx and Recovery.Idle as shown in Figure E-14.

E.3.11.1 Exit from Recovery.TSx

- The re-timer shall transition to Recovery.Idle upon observing successful TS2 handshake.
- The re-timer shall transition to Rx.Detect if either one of the following two conditions is met.
    - Upon the expiration of the tRecoveryActiveTimeout timer and no successful TS1 OS handshake has been observed.
    - Upon the expiration of the tRecoveryConfigurationTimeout timer and no successful TS2 OS handshake has been observed.
- The re-timer shall transition to Rx.Detect if Warm Reset is detected. Refer to Section E.3.1 for Warm Reset detection.

E.3.11.2 Recovery.TSx

Recovery.TSx is a substate for re-timers to participate link training with host and device. It combines Recovery.Active and Recovery.Configuration LTSSM substates.

E.3.11.2.1 Recovery.TSx Requirements

- If entry to Recovery is due to detecting TS1 OS, TS1A OS, or TS1B OS, and bit-lock/symbol lock are still preserved in both directions, a bit-level re-timer shall forward the received OS and monitor the progression of LTSSM. A SRIS re-timer shall transmit local TS1 OS instead of the received TS1A OS or TS1B OS until TS1 OS is received. Note that entry to Recovery under this condition may be due to the need for host to reset the device based on Hot Reset, or other operation modes, or due to bit errors that result in link layer initiating entry to Recovery. The bit-lock and symbol lock are preserved and no link training to acquire bit/symbol lock is required.
- If entry to Recovery is due to the timeout of the tU0RecoveryTimeout timer, or loss of bit-lock and symbol lock, the re-timer shall perform link training as defined in Section E.3.4.4.
- The re-timer shall participate the link training and monitor the status and progression of LTSSM.
- A SRIS re-timer shall preserve the OS boundary when performing OS switch from the local TS1 OS to recovered TS1 OS or TS2 OS. A SRIS re-timer shall not forward any TS2 OS until both received clocks are recovered.
- A SRIS re-timer shall perform the clock offset compensation based on the following.
    - For SS operation, it shall perform the clock offset compensation as defined in Section E.4.1.
    - For SSP operation, it shall perform the clock offset compensation as defined in Section 6.4.3.
- Upon entry to this substate, a bit-level re-timer shall perform its link training and complete the clock and OS switching per Section E.3.4.4.1. Additionally, a bit-level re-timer shall perform the clock and OS switching meeting the following timing requirements.

- If switching from the received TS1 OS, it shall complete the clock switching within 140 µs. Note that a bit-level re-timer may monitor the clock offset between the recovered clock and its local reference clock, and attempt to perform the clock switching when the clock offset is small. A bit-level re-timer shall expect that the frequency range of a host or device is either within +300ppm to −5300ppm, or within −1700ppm to −5300ppm if a RF-friendly SSC profile is employed. It is desired that a bit-level re-timer to monitor the recovered clock and determine its frequency range before setting the clock switching point.
- If switching from the received TS1A OS or TS1B OS, it shall complete the clock switching within 10 µs. Note that TS1A/TS1B OS do not contain SSC.
- Upon completing the clock switching at both simplex links, a bit-level re-timer shall complete the OS switching within two OS interval.

- The re-timer shall start the tRecoveryActiveTimeout timer upon entry to this substate. The ~~re-~~ tRecoveryActiveTimeout timer shall be reset and disabled upon observing successful exit handshake.
- The re-timer shall start the tRecoveryConfigurationTimeout timer upon observing TS2 OS at both ports. Note that a host and device may not exit from Recovery.Active simultaneously. For re-timers, observing TS2 OS at both ports is an indication that both the host and device have entered Recovery.configuration.

E.3.11.3 Recovery.Idle

Recovery.Idle is a substate where re-timers decode TS2 OS and decide the next operation state.

E.3.11.3.1 Recovery.Idle Requirements

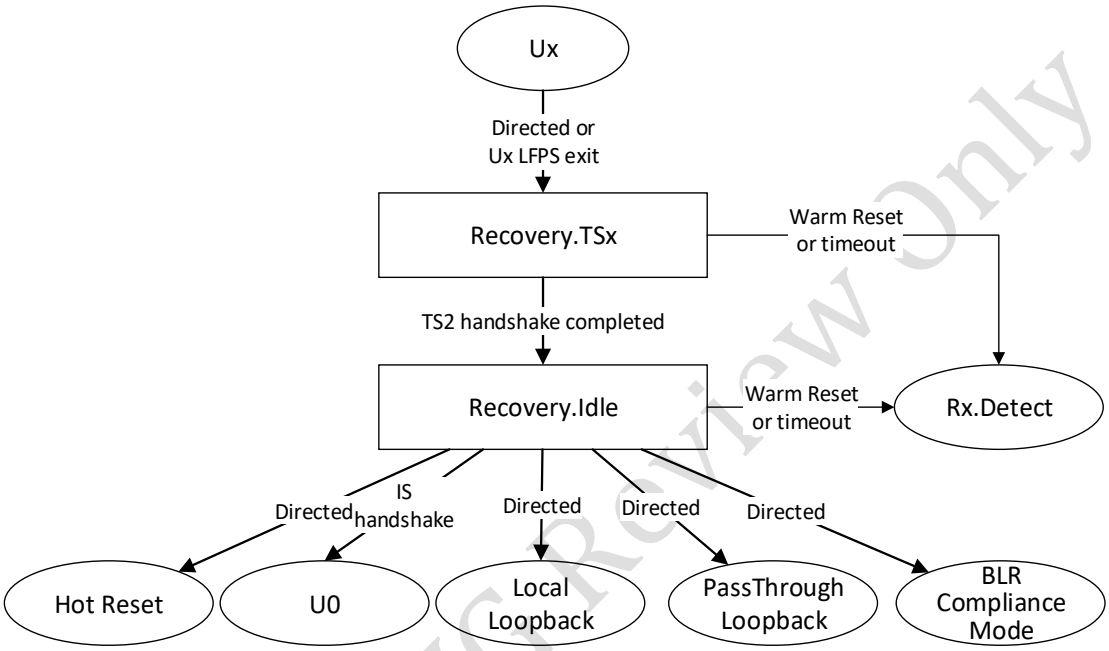
- The re-timer shall decode the link configuration field in TS2 OS and configure itself to the corresponding operation state.
- The re-timer shall start the tRecoveryIdleTimeout timer to monitor the progression of LTSSM.

E.3.11.3.2 Exit from Recovery.Idle

- The re-timer shall transition to U0 if either one of the following conditions is met.
  - Successful idle symbol handshake is observed.
  - A link command is observed.
- The re-timer shall transition to PassThrough Loopback if the Loopback bit (bit 2) in the link configuration field is asserted and the Compliance bit (bit 5) in the link configuration field is de-asserted.
- The re-timer shall transition to BLR Compliance Mode if the Loopback bit (bit 2) in the link configuration field and the Compliance bit (bit 5) in the link configuration field are both asserted.
- The re-timer shall transition to Local Loopback as the loopback slave if the re-timer loopback bit (bit 4 in the link configuration field) is asserted. Note that it is illegal to have both bit 4 and bit 2 asserted. If both bits are asserted, the re-timer shall give priority to PassThrough Loopback.
- The re-timer shall transition to Hot Reset if the Reset bit is asserted.

- The re-timer shall transition to Rx.Detect upon the expiration of the tRecoveryIdleTimeout timer if no successful idle symbol handshake has been observed.
- The re-timer shall transition to Rx.Detect if Warm Reset is detected. Refer to Section E.3.1 for Warm Reset detection.

Figure E-14. Recovery Substate Machine



E.3.12 PassThrough Loopback

PassThrough Loopback is a re-timer specific state defined by the Loopback bit (Bit 2) in the link configuration field of TS2 OS. In this state the re-timer operation shall be the same as if it is in U0, except that no error correction is allowed. The re-timer does not need to implement the two substates.

E.3.12.1 PassThrough Loopback Requirements

- The re-timer shall monitor the LTSSM progression.
- The re-timer shall not perform any error correction while looping through the traffic. Additionally, in Gen 1 operation, it shall perform one of the following.
  - Forward all data as is including bit errors.
  - Replace an error symbol with K28.4. Note that the re-timer shall preserve the running disparity at its transmitter but is not required to use the same disparity as decoded by the remove receiver.
- A SRIS re-timer shall perform the clock offset compensation as necessary.
- The re-timer shall implement and start the tLoopbackExitTimeout timer upon detecting Loopback LFPS exit signal.
- In x2 operations, the re-timer shall pass the received data on each lane independently. The transmitter lane to lane skew does not need to be maintained.

E.3.12.2 Exit from PassThrough Loopback

- The re-timer shall transition to Rx.Detect if any one of the following conditions is met.
  - Upon detecting successful Loopback LFPS exit handshake.
  - Upon timeout of the tLoopbackExitTimeout timer.
  - Upon detecting Warm Reset.

E.3.13 Local Loopback

Local Loopback is the same as the Loopback state defined in LTSSM. The re-timer always operates as a loopback slave.

E.3.13.1 Local Loopback Requirements

- The re-timer shall configure the two ports in the following.
  - It shall configure its port receiving TS2 OS with the Local Loopback bit (bit-4) within the link configuration field asserted.
  - It shall configure its other port in Rx.Detect.
- The re-timer shall implement the two substates defined in LTSSM.
- The re-timer operation shall meet the requirements defined in LTSSM.
- In x2 operations, the loopback operation is performed on a per lane basis. The transmitter lane to lane skew does not need to be maintained.

E.3.13.2 Exit from Local Loopback.Active

- The re-timer shall transition to Rx.Detect upon detecting Warm Reset at its port in Rx.Detect. Note that the re-timer will not declare Warm Reset at its port in Local Loopback.Active since the beginning of the Warm Reset will be treated as the start of the Loopback LFPS exit signal.
- The re-timer shall transition to Local Loopback.Exit upon detection of Loopback LFPS exit signal.

E.3.13.3 Exit from Local Loopback.Exit

- The re-timer shall transition to Rx.Detect if one of the following conditions is met.
  - Upon detecting Warm Reset.
  - Upon completing the Loopback LFPS exit handshake meeting Loopback LFPS exit signaling defined in Section 6.9.2.

E.3.14 Hot Reset

Hot Reset is a state where no actions need to be taken by the re-timer. The re-timer's responsibility is to monitor the progression of Hot Reset until its completion. The re-timer does not need to implement two substates in Hot Reset.

E.3.14.1 Hot Reset Requirements

- The re-timer shall track and monitor the progression of LTSSM.
- The re-timer in SS operation shall not delete any inbound TS2 OS with the Reset bit de-asserted in order to perform clock offset compensation. Note that the TS2 OS with the Reset bit de-asserted is used for Hot Reset.Active exit handshake.
- The re-timer shall start the tHotResetActiveTimeout timer upon entry to the state.

- The re-timer shall disable and reset the tHotResetActiveTimeout timer and start the tHotResetExitTimeout timer upon detecting successful TS2 OS based Hot Reset.Active handshake.

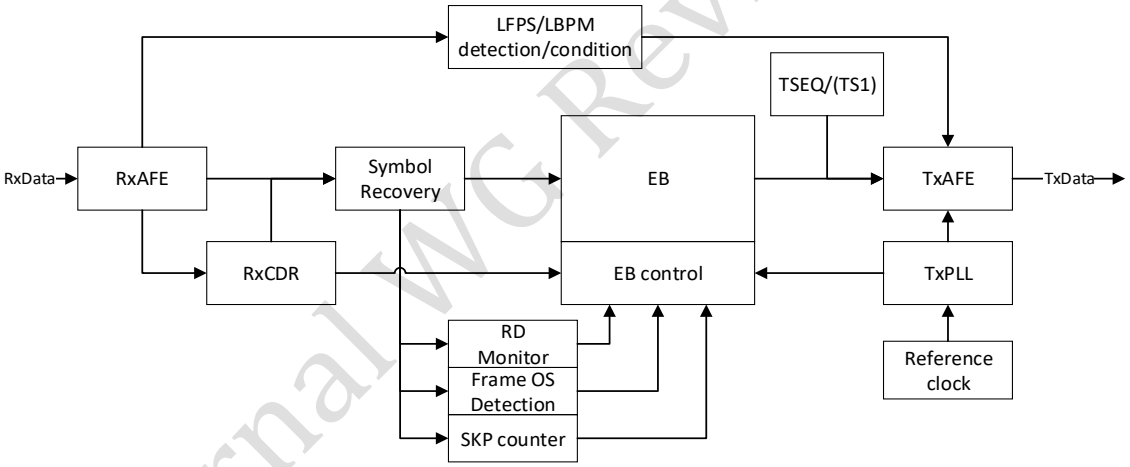
E.3.14.2 Exit from Hot Reset

- The re-timer shall transition to U0 upon observing successful Hot Reset.Exit handshake or any link command.
- The re-timer shall transition to Rx.Detect if one of the following conditions is met.
  - Upon timeout of the tHotResetActiveTimeout timer and no successful Hot Reset.Active handshake is observed.
  - Upon timeout of the tHotResetExitTimeout timer and no successful Hot Reset.Exit handshake is observed.
  - Upon detecting Warm Reset.

E.4 SRIS Re-timer Clock Offset Compensation

A SRIS re-timer is expected to implement a reference clock to facilitate its data transmission. Shown in Figure E-15 is an example block diagram of a SRIS re-timer implementation based on separate reference clock.

Figure E-15. Example Block Diagram of a Re-timer Operating in Gen 2 Mode



E.4.1 Gen 1x1 Operation

In Gen 1x1 operation, SKP OS defined for the clock offset compensation only considers the need by a host or device. There is no additional SKP OS budgeted for SRIS re-timers when in U0, Polling.TSx, Recovery, Hot Reset and PassThrough Loopback. A SRIS re-timer shall perform its clock offset compensation in those states based on implementation specific mechanisms, which are out of the scope of this appendix.

E.4.2 Gen 1x2 Operation

Re-timers shall perform its clock offset compensation as defined in Section 6.4.3.1.

- The maximum re-timer delay tDretimer shall not exceed 300 ns.

E.4.3 Gen 2 Operation

Re-timers shall perform its clock offset compensation as defined in Section 6.4.3.2.

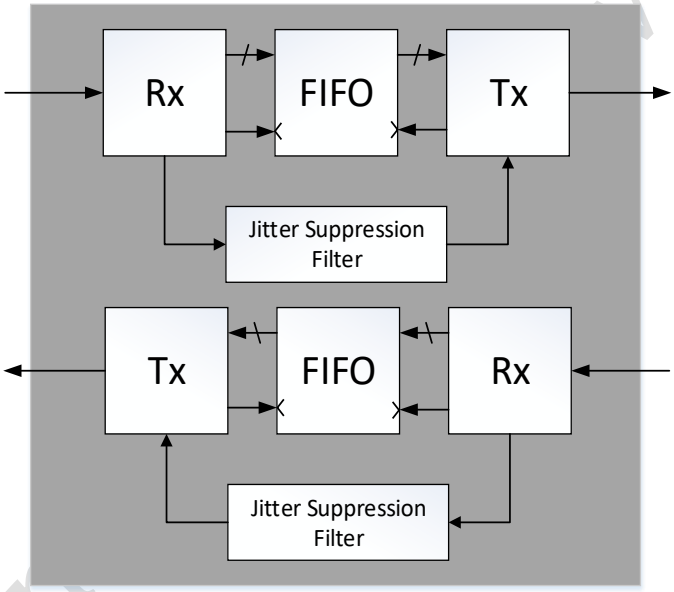
- The maximum re-timer delay tDretimer in Gen 2x2 operation shall not exceed 200 ns.

E.5 Bit-Level Re-timer Jitter Transfer Function

This section describes the normative jitter transfer function (JTF) requirements for bit-level re-timers. Bit-level re-timers which use the recovered clock from the input data stream as the input clock for the transmitter can pass on low frequency jitter, which can in turn result in accumulation of excessive low frequency jitter in systems with cascaded bit-level re-timers. The JTF requirements defined in this section ensure that a host or device receiver does is not subjected to input jitter that exceeds the amounts specified in the jitter tolerance requirements contained in Section 6.8.5.

In specifying the bit-level re-timer JTF requirements, the conceptual clocking architecture shown in Figure E-16 is assumed. Note that the actual clocking architecture for a given product is an implementation choice.

Figure E-16. Block Diagram for Example Bit-Level Re-timer Clocking Architecture



The jitter transfer function for a re-timer with this clocking architecture is

(E.1) $$H_{JTF\_TX}(s) = H_{JTF\_RX}(s) \cdot H_{JSF}(s)$$

where $H_{JTF\_RX}(s)$ is the jitter transfer function for the re-timer receiver clock recovery

$H_{JSF}(s)$ is the jitter transfer function for the jitter suppression filter.

The transfer function for a second order CDR typical of high-speed signaling systems is expressed as:

(E.2) $$H_{JTF\_RX}(s) = \frac{2\zeta_{Rx}\omega_{nRx}s + \omega_{nRx}^2}{s^2 + 2\zeta_{Rx}\omega_{nRx}s + \omega_{nRx}^2}$$

The transfer function for the jitter suppression filter may be either first order or second order, depending upon implementation. The reference JTF curves in Figure E-18 assume a second order filter with transfer function expressed as:

$$H_{JSF}(s) = \frac{2\zeta_{JSF}\omega_{nJSF}s + \omega_{nJSF}^2}{s^2 + 2\zeta_{JSF}\omega_{nJSF}s + \omega_{nJSF}^2} \quad \text{(E.3)}$$

where ω_{nRx} is the natural frequency of the re-timer CDR

ζ_{Rx} is the damping factor of the re-timer CDR

ω_{nJSF} is the natural frequency of the low pass jitter suppression filter (JSF)

ζ_{JSF} is the damping factor of the low pass jitter suppression filter (JSF)

The relationship of the 3 dB frequencies of the CDR and JSF to their natural frequencies and damping factors are

$$\omega_{3dBRx} = \omega_{nRx}\left(1 + 2\zeta_{Rx}^2 + \left[\left(1 + 2\zeta_{Rx}^2\right)^2 + 1\right]^{\frac{1}{2}}\right)^{\frac{1}{2}} \quad \text{(E.4)}$$

$$\omega_{3dBJSF} = \omega_{nJSF}\left(1 + 2\zeta_{JSF}^2 + \left[\left(1 + 2\zeta_{JSF}^2\right)^2 + 1\right]^{\frac{1}{2}}\right)^{\frac{1}{2}} \quad \text{(E.5)}$$

The jitter transfer function for this system is illustrated in Figure E-17. Bit-level re-timers shall meet the normative jitter gain requirements defined in Table E-4. In addition, the re-timer shall meet all normative timing and electrical requirements defined in Chapter 6. A set of reference curves for SuperSpeed Gen 1x1 re-timers are shown in Figure E-18.

Figure E-17. Jitter Transfer Illustration

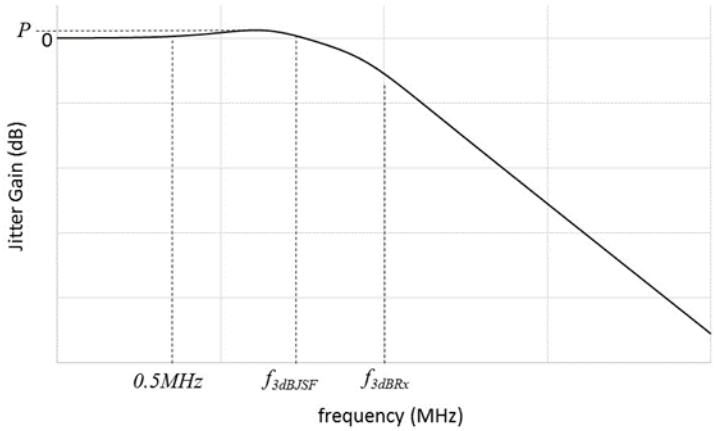
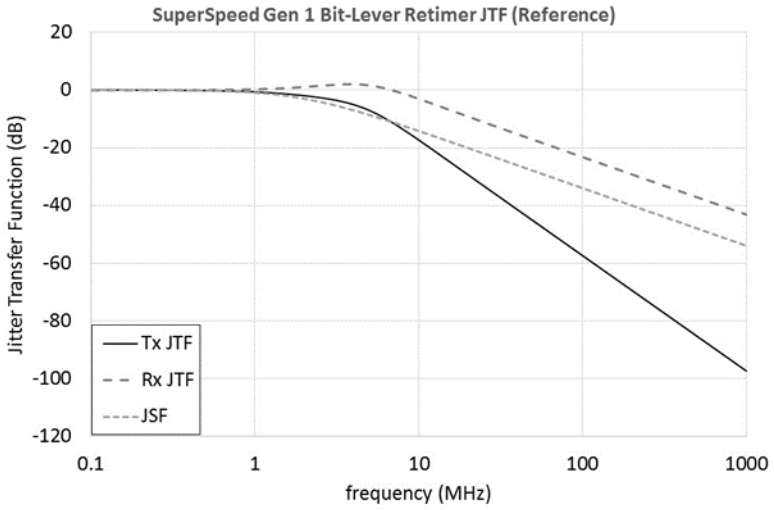


Table E-4. Bit-Level Re-timer Jitter Transfer Function Requirements

Term	Gen 1x1	Notes
Jitter Gain for f<500kHz	0.~~1dB~~15dB (max)	Normative requirement.
Jitter Gain for f>500kHz	0.0dB (max)	Normative requirement.
JSF 3dB frequency	2MHz (max)	Overall JTF is expected to meet a −20 dB/decade slope above the JSF 3 dB frequency.

Figure E-18. Jitter Transfer Reference Curves



E.6 Re-driver Architectural Overview and Requirement

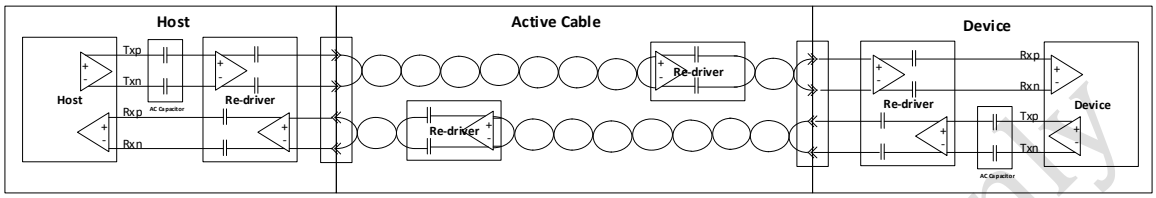
As a re-timer is protocol aware and complies to the transmit and receive electrical specifications defined in Chapter 6, it ensures the interoperation with the host and device. As for a re-driver, it is protocol agnostic, and its transmit compliance to the specification depends not only on the re-driver's own performance, but also the quality of its input signals. This is especially true in Gen 2 operation, where linearity of the signal is critical to the success of clock and data recovery at the receiver. Furthermore, as a re-driver compensates for the input signal due to the channel loss, it may also inevitably inject various non-correctable noises to the output. These un-wanted noises may include random noise, noise due to signal distortion when passing through a re-driver, and additional power supply noise, etc. They are not accounted for by the receiver and must be constrained to ensure maximum interoperability. In this section, the behavioral and electrical requirement of a linear re-driver (LRD) are recommended for Gen 2 operation. The linearity of the LRD at Gen 1 operation may not be required. Additional re-driver place and route guideline and a system level validation methodology are also provided.

E.6.1 Re-driver Link Topology

It is assumed that a link in Gen 2 operation can accommodate for the maximum number of three re-drivers, one on-board with a hub DFP, and one on board with a device UFP, and one in an active cable. It is out of the scope of this specification if more than three re-drivers are employed. Shown in Figure E-19 is an example link topology with three re-drivers. Note

that the placement of the re-driver in the active cable is only an illustration with a unidirectional re-driver placed at the far-end. The actual construction of a re-driver based active cable is implementation specific. Furthermore, an active cable shall be equal or better in its loss characteristics of more than -6dB as an equivalent passive cable. Refer to the USB Type-C Specification for details.

Figure E-19. Example Link Topology with Three Re-drivers



E.6.2 Re-driver Power Management

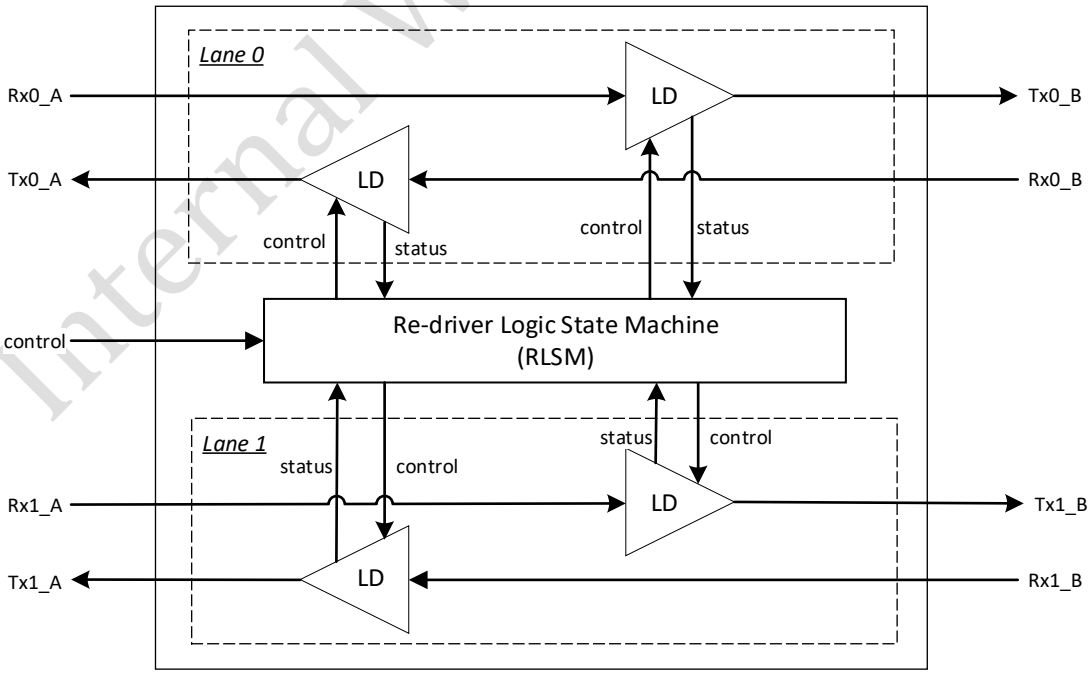
A re-driver is not protocol aware and will not manage its power state explicitly matching the low power link states of U1, U2 or U3. System level simplification is required to ensure the interoperability with the re-driver.

- It is highly recommended that both U1 and U2 be disabled if an on-board re-driver is deployed.

E.6.3 Re-driver Behavioral Requirement

Shown in Figure E-20 is a conceptual block diagram of a Gen 2x2 re-driver. It consists of two lanes with each lane having two line drivers (LD). The operation of each LD is controlled by a re-driver logic state machine (RLSM). In this section, the details of RLSM and the LD functional requirements are described.

Figure E-20. Re-driver Conception Block Diagram

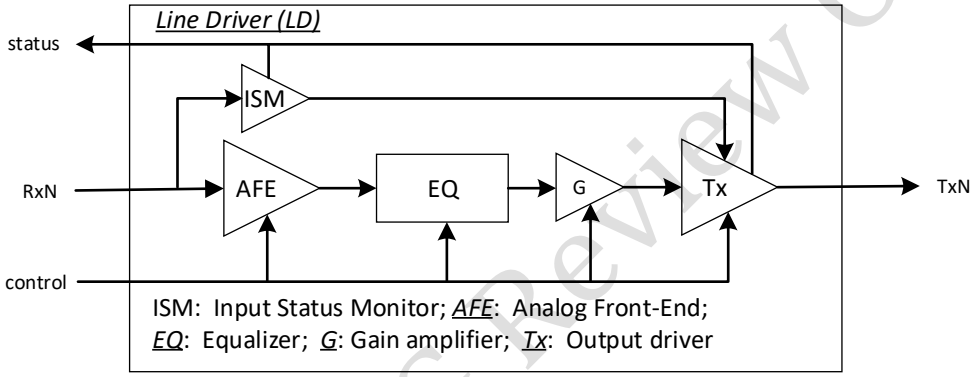


E.6.3.1 LD Functional Requirements

Shown in Figure E-21 is a conceptual LD block diagram. An LD consists of all the analog components in its signal path to restore the input signal to its original condition. This signal path includes, but is not limited to, an analog front-end for input signal conditioning, an equalizer and a flat gain amplifier to compensate for the channel loss, and an output driver with its source impedance meeting $R_{TX\text{-}DIFF\text{-}DC}$ defined in Table 6-18. The configuration of these components is typically done before the LD operation. Note that the LD performance also varies depending on the amount of the channel loss it is capable of compensating.

An LD includes Input Status Monitor (ISM) to monitor the input status, in order to manage the operation of its signal path and provide the input status to RLSM for link state monitoring and coordination of each LD. The input status includes the incoming LFPS signal or SS signal, the detection of LFPS electrical idle, and the transition from SS to LFPS EI.

Figure E-21. Conception Line Driver Block Diagram

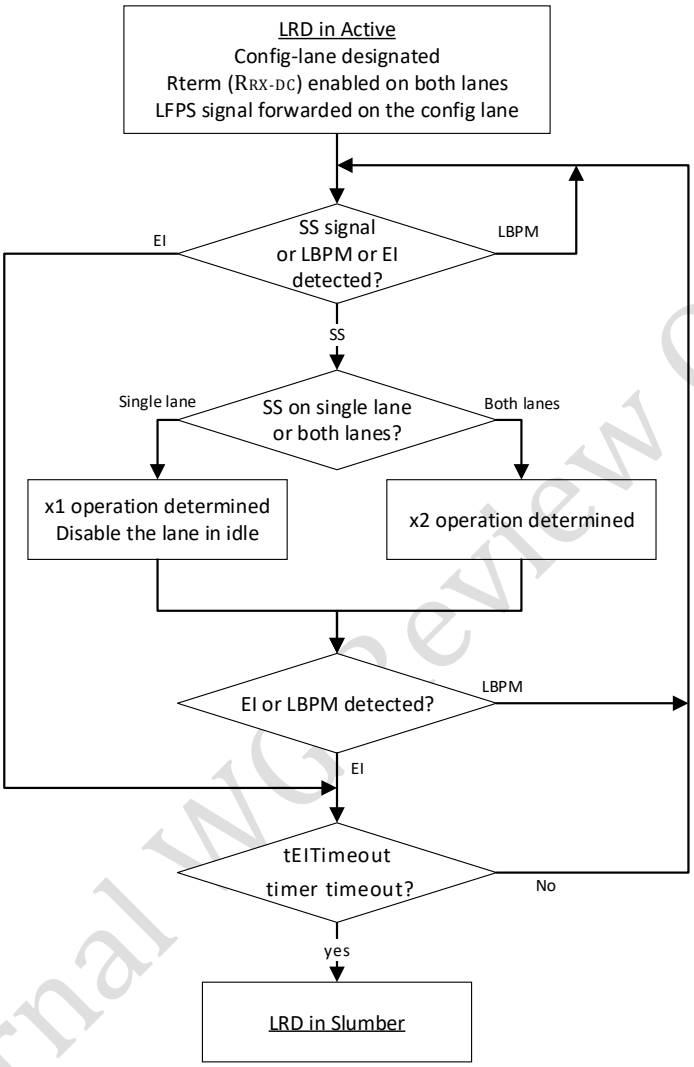


Shown in Figure E-23 is the state diagram of RLSM to coordinate and synchronize the operations on all lanes in different sublinks. RLSM is defined based on the following assumptions and capabilities.

- When the transition condition "directed" is used, it implies the direction from a system.
- It is capable of differentiating among LFPS, LBPM and the SS signal. It is preferred but not required to perform LFPS and LBPM decoding. Note that the ability to perform LFPS and LBPM decoding ensures the re-driver to configure its operation according to the speed negotiation between DFP and UFP.
- It may employ the same LD configuration for both Gen 2 and Gen 1 operations, or different configurations if desired based on LBPM decoding. The mechanism for re-driver configuration, or advanced equalization adaptation are implementation specific, and they are out of the scope of this specification.
- It shall be designated by the system which lane is the config lane.
- The transition of the link configuration between x1 or x2 modes is highly desired to be based on LBPM decoding. It may be implicitly inferred through monitoring the progression on the input LFPS/LBPM or SS signals. Shown in Figure E-22 is a reference flow diagram of re-driver performing the link configuration without LBPM decoding.

Note that the RLSM behavioral requirement described in this section is intended for future implementations to achieve maximum interoperability.

Figure E-22. Re-driver in Active Tracking Line Configuration and Operation



E.6.3.2 Disabled

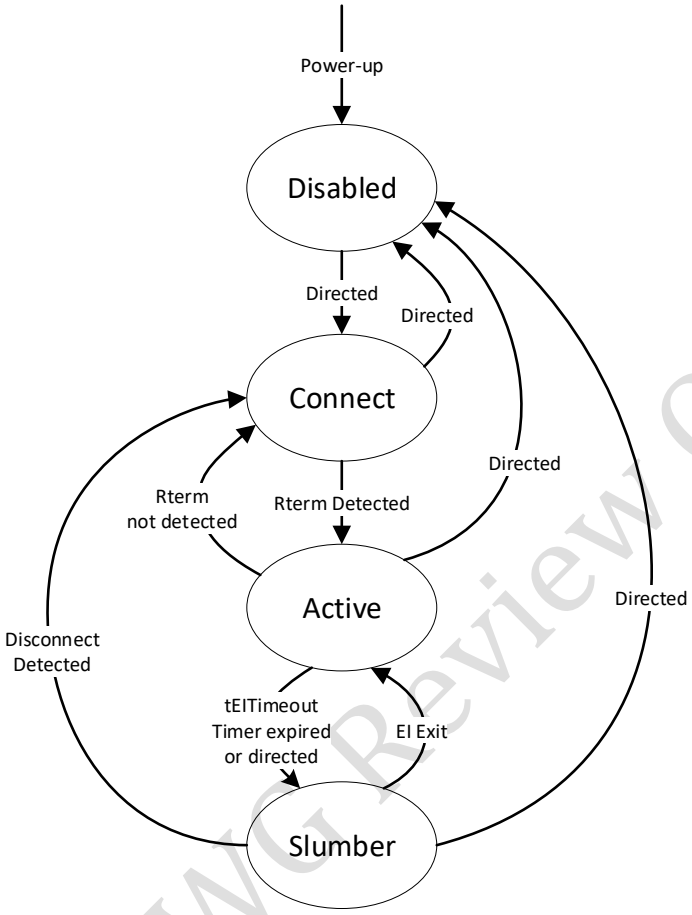
Disabled is an optional power-on initial state. The re-driver shall meet the following requirement.

- It shall be in its lowest power state and wait for direction to enter operation.
- It shall present its high impedance to ground of $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ defined in Table 6-22 at its receiver.

The re-driver shall perform the state transition based on the following.

- The next state is Connect if directed.

Figure E-23. Re-driver Logic State Machine (RLSM)



E.6.3.3 Connect

Connect is a state where the re-driver performs far-end receiver termination. It maps the LTSSM Rx.detect's sub-states of Rx.Detect.Active, Rx.Detect.Quiet. Connect may also be a power-on intial state, if it is placed in a system that is ready to start the USB operation upon power-on. The re-driver shall perform the following in Connect.

- It shall perform the periodic far-end receiver termination detection on the Configuration Lane and at both DFP and UFP at least every 8 ms as defined in Section E.3.2.1. Note that it is highly desired that the re-driver consumes no more than 200 µs to perform the far-end receiver termination detection. This is to ensure minimum interruption to potential incoming LFPS signal.
- It shall disable the transmitters. Note an LD may have its LFPS receiver enabled to improve the responsiveness of the LRD in this state. If a Polling.LFPS signal is detected, it implies its link partner has already transitioned to Polling. An LRD may not need to wait until the next cycle of far-end receiver termination detection.

The re-driver shall perform the state transition based on the following.

- The next state is Active if either of the following conditions is met.

- The far-end low-impedance receiver termination (R_{RX-DC}) defined in Table 6-22 is detected at both ports of the config lane.
- The Polling.LFPS signal is received at either port if the LFPS receiver in the LD is enabled.
- When directed by RLSM. Note that the opposite sublink may have received Polling.LFPS implying the presence of R_{RX-DC}.

- The next state is Disabled if directed.

E.6.3.4 Active

Active is a state where the re-driver is either forwarding the LFPS signal or SS signal. It maps the LTSSM states of Polling, U0, Recovery, Loopback, Hot Reset, Compliance Mode, and Rx.Detect sub-state of Rx.Detect.Reset. The re-driver shall meet the following requirement.

- It shall enable its low-impedance receiver termination (R_{RX-DC}) at config lane. It may enable its low-impedance receiver termination (R_{RX-DC}) at non-config lane in x1 operation.
- It shall forward the received LFPS on the config lane, and SS signal on both lanes if it is x2 operation.
- It shall monitor the input status and manage the LD and LRD operation during various LTSSM link state in Active.
- It shall implement a 24 ms tEITimeout timer to monitor the duration of EI. This timer shall be started when LFPS EI or the transition from SS signal to LFPS EI is detected. It shall be reset and disabled if an input signal is detected. Note that this timer is intended to ensure that the link enters U3 or eSS.Inactive, and to overcome any EI during Polling to remain in Active.
- It shall remain in this state if EI is declared and the tEITimeout timer has not expired.
- It shall monitor the duration of the LFPS signal. If it is Warm Reset, it shall perform the following at then of Warm Reset
  - It shall perform the far-end receiver termination detection at its DFP.
  - It shall block any Polling.LFPS signal it may receive at its DFP while performing the far-end receiver termination detection at its DFP.

The re-driver shall perform the state transition based on the following.

- The next state is Disabled if Directed.
- The next state is Slumber if directed or when the tEITimeout timer has expired and the input remains in EI.
- The next state is Connect if the far-end low-impedance receiver termination (R_{RX-DC}) defined in Table 6-22 is not detected.

E.6.3.5 Slumber

Slumber is a state where the input is in EI and the re-driver is in a low power state. It maps the USB link states of U3, and eSS.Inactive. The re-driver shall meet the following requirement.

- It shall maintain its low-impedance receiver termination (R_{RX-DC}).
- It shall perform the far-end receiver termination detection upon entry to the state and in at least every 100 ms tSLRxdetDelay interval afterwards, regardless its orientation towards a hub DPF or device UFP.

The re-driver shall perform the state transition based on the following.

- The next state is Disabled if Directed.
- The next state is Connect if the far-end receiver termination (R_{RX-DC}) is not detected.
- The next state is Active if an input LFPS signal is detected.

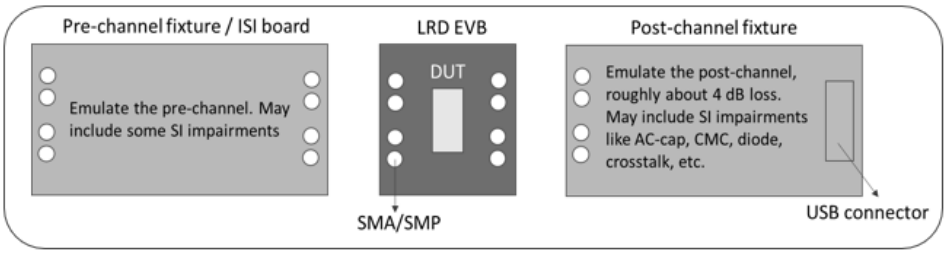
E.6.4 LRD Electrical Requirements

LRD electrical requirements govern the performance of an LRD as a stand-alone component and its performance in emulated system environments. This section specifies those requirements.

E.6.4.1 Test Fixtures

Fixtures shown in Figure E-24 are needed to evaluate LRD electrical performance include the LRD Electrical Evaluation Board (EVB), Pre- and Post-channel Fixtures, and the standard USB 3.2 test fixtures.

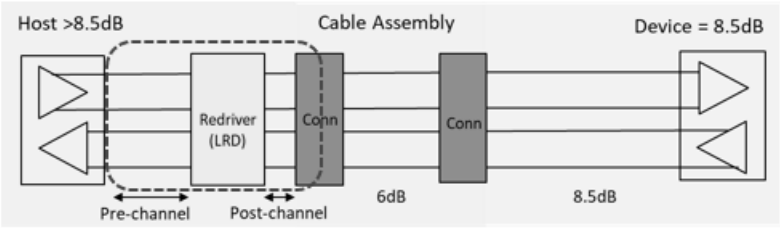
Figure E-24. Illustration of LRD Test Fixtures



An LRD EVB is a small PCB mounted with an LRD as the DUT. The EVB includes SMA or SMP connectors to connect with measurement instruments or the pre- and post-channel fixtures to evaluate LRD performance. The insertion loss of the trace between the LRD and SMA/SMP in the EVB shall be controlled within 1.5 +/– 0.5 dB. There shall be a calibration structure in the EVB to remove the fixture effect in the LRD S-parameter or transfer function measurements. This calibration structure may also be used to measure the baseline jitter (without the LRD), which will be discussed in Section E.6.4.3. All the high-speed differential pairs shall be routed out to SMA's/SMP's to allow crosstalk measurements.

The pre-channel fixture emulates the interconnect of a USB 3.2 host or device between the transmitter/receiver and the LRD, while the post-channel fixture mimics the interconnect between the LRD and a USB connector, as illustrated in Figure E-25. A USB 3.2 host or device is emulated when the pre- and post-channel fixtures are connected via the LRD EVB.

Figure E-25. Illustration of a Typical USB 3.2 Topology with LRD



The pre- and post-channel fixtures include signal integrity impairments (loss and reflection) typically seen in a USB 3.2 host or device. The pre- and post-channel fixtures may include multiple ports to cover a range of insertion losses that an LRD is expected to support. The pre- and post-channel fixtures are standardized by USB-IF. Refer to the USB-IF whitepaper "LRD Test Fixtures" for details (to be developed).

The standard USB 3.2 test fixtures include the existing USB 3.2 transmitter and receiver test fixtures defined by USB-IF. Refer to USB 3.1 Electrical Test Fixture Topologies & Tools (https://usb.org/sites/default/files/documents/usb3p1_fixture_topologies_11-8-2017_0.pdf) for descriptions.

The electrical requirements listed in sections E.6.4.2 to E.6.4.6 are informative. The normative compliance requirement is a full channel compliance eye test discussed in E.6.4.7. Furthermore, any system that uses re-driver should go through existing USB compliance test to ensure proper system level compliance.

Although the electrical requirements are informative, re-driver vendors are strongly encouraged to provide these data in their product datasheet. This is because these electrical data are critical in system implementation, tuning, and debug, if needed.

E.6.4.2 Linearity Requirements

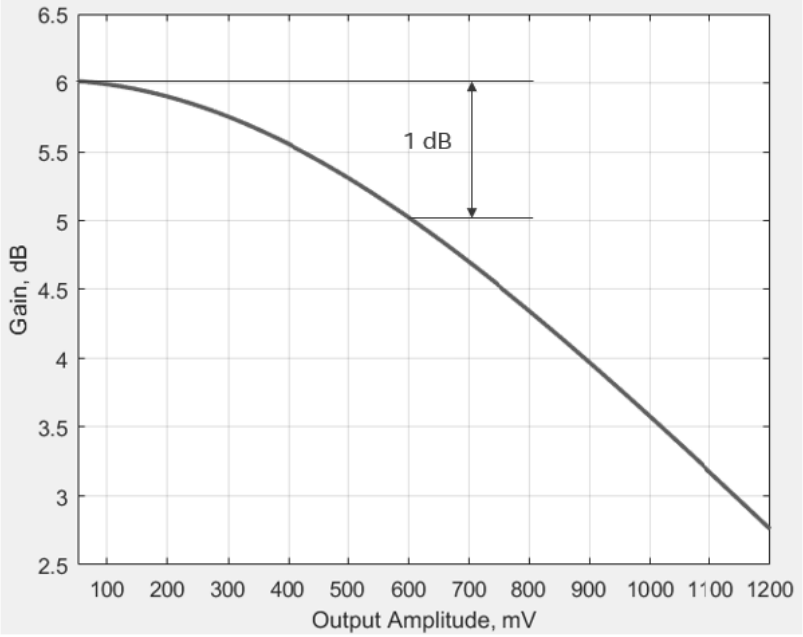
Linearity is a key performance indicator for an LRD. Excessive nonlinearity from an LRD may interfere with link training and degrade eye margins.

Both low frequency or DC linearity and high frequency or AC linearity are specified. Those linearity tests use the LRD EVB to measure the relationship between LRD input and output signal amplitudes, with the following steps and processes:

- For DC linearity measurement, set a signal generator / BERT to a 20 MHz clock pattern, or 20-MHz sine wave.
- For AC linearity test, a 5-GHz sine wave shall be used.
- The calibration structure, a through connection (see Figure E-27) without the LRD, is used to calibrate the input signal amplitude. The signal generator / BERT is connected to the scope via the through and signal amplitude seen from the scope is the input amplitude. The signal generator/ BERT is tuned such that the amplitudes measured by the scope are about from 50 mV to 1200 mV.
- The signal generator/BERT can now be connected to the scope with the LRD in between and the output amplitudes can be measured by the scope. DC blocking capacitors shall be used if they are not included in the EVB.

- The Gain is calculated as the ratio of the output amplitude to input amplitude, measured in dB: Gain = 20*log10(output amplitude / input amplitude). The Gain is plotted against the output amplitude, as illustrated in Figure E-26. The output 1-dB compression amplitude Vout_1dB, is used to measure linearity.

Figure E-26. Illustration of 1-dB Compression Point



- The 1-dB compression amplitude depends on LRD EQ gains or settings. The DC and AC linearity tests shall be performed for the optimal LRD EQ settings identified in the compliance eye tests to be discussed in Section E.6.4.7.

The pass/fail criterion for the 1-dB compression amplitude Vout_1dB is ≥ 700 mV.

E.6.4.3 Intrinsic Jitter Requirements

An LRD as an active component will introduce some jitter. Hence a jitter requirement is defined to control the intrinsic jitter from an LRD.

To obtain LRD intrinsic jitter, two measurements shall be done, as illustrated in Figure E-27. The baseline testing is to calibrate jitter using the calibration structure or the through in the EVB without the DUT LRD. The following key points shall be noted in the baseline testing:

- Jitter measurements shall be done with the LRD EQ setting identified from the compliance eye testing to be discussed in Section E.6.4.7.

- A clock or single-tone signal of 5 GHz, the Nyquist frequency of USB 3.2 Gen 2, shall be used for jitter measurements.

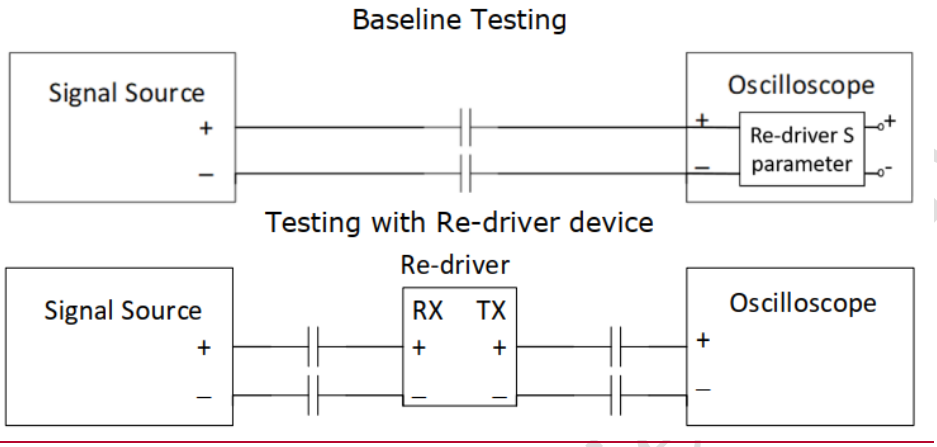
- The signal source should be adjusted such that the output amplitude of the LRD be about 100 mV below the AC 1-dB compression point to avoid LRD operating in non-liner region for the specific LRD EQ setting.

- The LRD S-parameter or transfer function for the specific LRD EQ setting, with fixture effect de-embedded, shall be embedded in the oscilloscope. This will ensure

the baseline testing and LRD measurement be done with about the same dynamic range to ensure accuracy.

- DC blocking capacitors shall be used if they are not part of the EVB.

Figure E-27. Intrinsic Jitter Test Setups



To test with an LRD, set the LRD to the specific EQ and the rest of the steps are the same as in the baseline measurement, except that no LRD s-parameter be embedded into the oscilloscope.

Utilizing the USB jitter processing software (in the oscilloscope), the baseline and LRD measurement jitters are reported in their respective components. The jitter difference at the target BER (10-12) is defined as the LRD intrinsic jitter:

$$DJ_{Intrinsic} = DJ_{LRD\ measurement} - DJ_{Baseline}$$

$$DCD_{Intrinsic} = DCD_{LRD\ measurement} - DCD_{Baseline}$$

$$RJ_{Intrinsic} = (RJ^2_{LRD\ measurement} - RJ^2_{Baseline})0.5$$

$$TJ_{Intrinsic}\ at\ 1e\text{-}12\ BER = DJ_{Intrinsic} + DCD_{Intrinsic} + 14.07 * RJ_{Intrinsic}$$

The pass/fail criteria for the intrinsic jitter is $TJ_{Intrinsic} \leq 0.04UI$ (4ps) at 1e-12 BER. Note there is no separate requirements on DJ, DCD, or RJ. It is recommended, however, to minimize DJ and DCD so that the total jitter in multiple re-driver implementation can be better managed.

E.6.4.4 Additive Noise Requirement (σ_n)

σ_n is the standard deviation of the uncorrelated additive noise added to the output signal of an LRD. Due to the expected small magnitude of the LRD additive noise, its determination also needs two measurements: One baseline measurement to establish the measurement noise floor, and an LRD measurement to capture the total noise. The difference of the two measurements is the LRD additive noise.

In order to achieve an accurate measurement, the measurement is done with a low frequency signal of a 10 MHz clock pattern. A relatively low signal amplitude of 300 mV peak-to-peak shall be used. The additive noise test shall be done with the LRD EQ setting identified from the compliance eye testing to be discussed in Section E.6.4.7.

For the baseline measurement, the LRD S-parameter or transfer function for the specific LRD EQ setting, with fixture effect de-embedded, shall be embedded in the oscilloscope. This will ensure the baseline testing and LRD measurement be done with about the same dynamic range to ensure accuracy. DC blocking capacitors shall be used if they are not part of the EVB.

For the LRD measurement, set the LRD to the specific EQ and the rest of the steps are the same as in the baseline measurement, except that no LRD s-parameter be embedded into the oscilloscope.

The low and high signal levels can be obtained from the captured waveform. The averaged standard deviation for the low and high signal levels is reported as the noise.

$$\sigma_n = (\sigma^2 \text{LRD measurement} - \sigma^2 \text{Baseline})^{0.5}$$

σ_n shall be less or equal to 2 mV-rms.

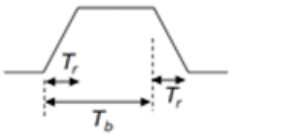
E.6.4.5 Integrated Return Loss Requirement

The integrated return loss is specified to manage the reflection from the LRD package and die termination. The differential return loss may be measured with a VNA using the LRD EVB, as part of the LRD transfer function characterization. The LRD EQ setting identified from the compliance eye testing shall be used and the fixture effect shall be de-embedded. The integrated return loss is calculated as:

$$IRL = db\left(\sqrt{\frac{\int_0^{fmax} |V_{in}(f)|^2 |RL(f)|^2 df}{\int_0^{fmax} |V_{in}(f)|^2 df}}\right)$$

where *fmax* = 10 GHz, *df* <= 10MHz, *RL(f)* is the measured differential return loss, referencing to an 85-ohm impedance, and *Vin(f)* is the input pulse frequency spectrum:

Figure E-28. Input Pulse Frequency Spectrum



$$|V_{in}(f)| = \left|\frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b}\right|$$

T_b = Unit Interval = 100 ps
T_r = 0 to 100% rise time = $0.4T_b$

The integrated return loss, IRL, shall be less or equal to –17 dB.

E.6.4.6 Integrated Crosstalk Requirement

The integrated crosstalk controls the crosstalk noise from the LRD among signal pairs. Crosstalk may be measured with a VNA using the LRD EVB. The integrated near-end and far-end crosstalk are calculated using the equations below:

$$INEXT = db\left(\sqrt{\frac{\int_0^{fmax} |V_{in}(f)|^2 |NEXT(f)|^2 df}{\int_0^{fmax} |V_{in}(f)|^2 df}}\right)$$

$$IFEXT = db\left(\sqrt{\frac{\int_0^{fmax} |V_{in}(f)|^2 |FEXT(f)|^2 df}{\int_0^{fmax} |V_{in}(f)|^2 df}}\right)$$

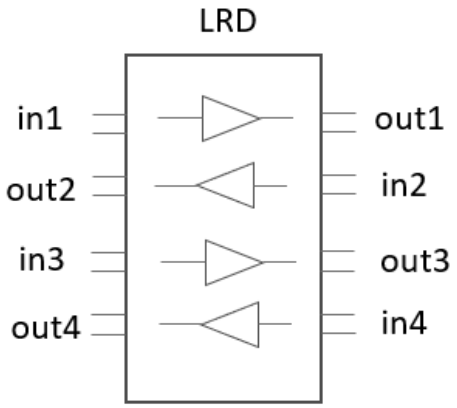
where *NEXT(f)* and *FEXT(f)* are measured near-end and far-end crosstalk, respectively. The definitions of *fmax*, *df*, and *Vin(f)* are the same as the integrated return loss formula above.

The integrated near-end crosstalk INEXT shall be measured between pairs in1-out2 and in2-out1, as illustrated in Figure E-29. If the LRD supports two USB lanes, INEXT between the following pairs shall also be measured: in3-out2, in3-out4, in2-out3, and in4-out3. For an LRD with two USB lanes, IFEXT between pairs in1-out3 and in2-out4 shall be measured.

INEXT and IFEXT have a strong dependency on LRD gains, which amplify the crosstalk. The optimal LRD EQ setting used for the compliance eye testing shall be used for INEXT and IFEXT measurements. The fixture effect shall be de-embedded out.

The integrated near-end and far-end crosstalk between any two signal pairs shall be less or equal to –35 dB. If the LRD includes other high-speed signals, for example, DisplayPort, it is recommended to control the crosstalk within this spec.

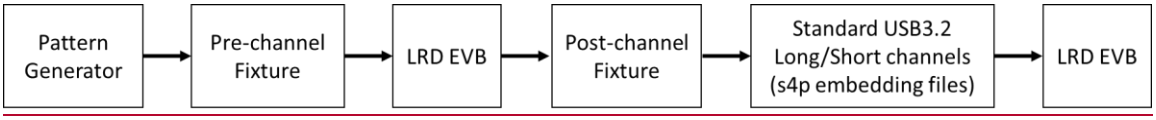
Figure E-29. Integrated Near-End Crosstalk Measurement Points



E.6.4.7 Compliance Eye Requirement

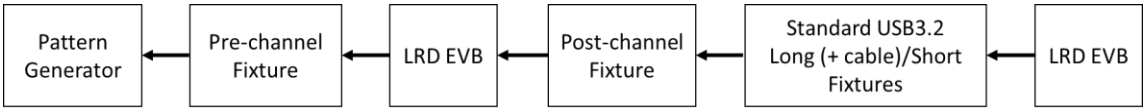
The LRD compliance eye requirement and test setups follow the relevant USB 3.2 base specification and the compliance test specification (https://www.usb.org/document-library/electrical-compliance-test-specification-superspeed-usb-10-gbps-rev-10). Figure E-30 shows the Tx test path; it emulates the USB 3.2 transmitted Eye Test at 10 GT/s (TD 1.4), except that the transmitter is replaced with a pattern generator.

Figure E-30. Compliance Eye Test – Tx Path



The Rx path, illustrated in Figure E-31, shall also be tested. The standard USB 3.2 long/short fixtures are identical to what used in the USB 3.2 Rx JTOL test; they are physical fixtures, not embedding s4p files. Refer to "Electrical Compliance Test Specification Enhanced SuperSpeed Universal Serial Bus" for details.

Figure E-31. Compliance Eye Test – Rx Path



The compliance eye test shall follow the setups and requirements below. Refer to USB 3.2 compliance test spec for all other setups.

- The pattern generator is configured with the following outputs:
  - 800 mV differential peak-to-peak swing
  - 1 ps rms random jitter
  - 0.17 UI sinusoidal jitter at 100 MHz
  - 2.2 dB pre-shoot and –3.1 de-emphasis
- The test shall be done for each of the pre- and post-channel fixture ports with a prescribed insertion loss range for the short and long fixtures. LRD EQ settings may e swept for optimal result.
- The same LRD settings shall be used for both the long and short channels/fixtures during test.
- Tx and Rx-path tests may use different LRD settings.
- The eye height and eye width pass/fail criteria are 70 mV and 48 ps (both at 10-6 BER), respectively, the same as defined in the USB 3.2 spec.

E.6.4.8 Implementation Guidelines

One of the key considerations in using an LRD is the LRD equalization range. The USB 3.2 specification has an informative insertion budget of 8.5 dB for the host/device and 23 dB for the end-to-end channel. We should make sure that the LRD equalized insertion loss of the host/device and channel be a few dB, recommend 3dB better than the spec budget. Such a margin is needed to compensate for the LRD impairments such as nonlinearity, intrinsic jitter, additive noise and crosstalk amplification.

In the example shown in Figure E-32, the unequalized (thick solid line) host insertion loss is about –10dB, just about 1.5 dB exceeding the budget. After applying LRD EQ, the equalized host insertion loss can be much less than the spec budget of 8.5 dB. So, in this example, the LRD EQ gain range is more than adequate. Actually, some of the high gain EQ will cause over equalization as the host further deviates from a low-pass filter nature of a passive channel.

Figure E-32. Illustration of Host Insertion Loss

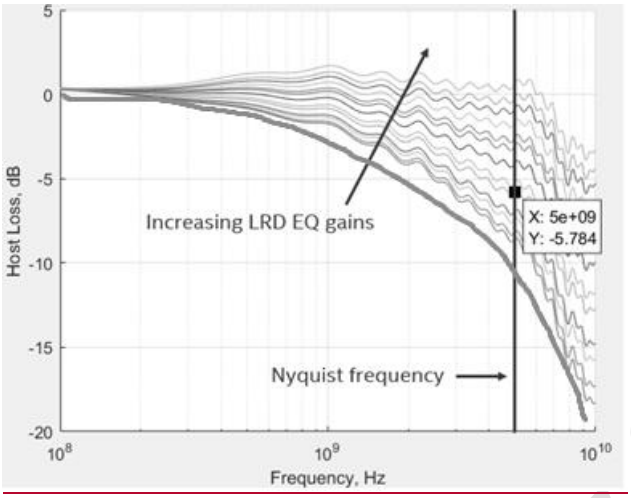
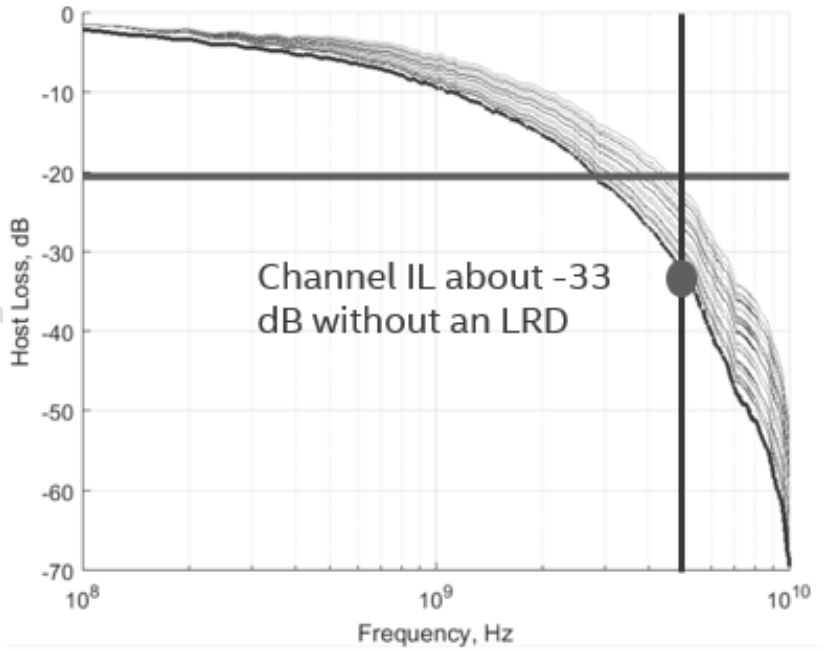


Figure E-33 shows an example of a long channel insertion loss. The channel insertion loss without an LRD is about –33dB, far exceeding the spec budget of 23 dB. If we target to have an equalized channel insertion loss of 20 dB (3 dB less than the spec budget), even the highest LRD gain will not be able to achieve it. So, in this example, the LRD might not have enough EQ gain range to support this channel.

Insertion loss is certainly not the only parameter that impacts signal integrity. Channel crosstalk and reflection can seriously degrade link margin and efforts should be made by system integrators to minimize crosstalk and reflection.

Figure E-33. Illustration of Channel Insertion Loss



There may be an optimal LRD placement. Placing an LRD very close to a transmitter should be avoided. In this case, the signal amplitude entering the LRD is very high and the output signal will be seriously compressed by the LRD such that the signal does not have enough strength to reach the receiver. It is up to system integrators to optimize the LRD location based their specific implementations.

E.6.4.9 Electrical Over Stress Requirements

To ensure the electrical compatibility with an on-board host or device, the re-driver shall comply to the following transmitter and receiver requirements.

- It shall meet the instantaneous voltages (DC+AC) $V_{TX\text{-}DC+AC\ CONN}$ as defined in Table 6-18. Note that the measurement of $V_{TX\text{-}DC+AC\ CONN}$ is at the far side of the AC coupling capacitors. Refer to TBD LRD Compliance Program for $V_{TX\text{-}DC+AC\ CONN}$ test configuration.

- It shall meet the instantaneous DC common mode voltage coupled to the far-end Tx $V_{RX\text{-}CM\text{-}DC\ CONN}$ as defined in Table 6-23. Note that $V_{RX\text{-}CM\text{-}DC\ CONN}$ requirement for re-driver is normative and is measured at the side of the AC cap associated with the far-end Tx. Refer to TBD LRD Compliance Program for $V_{RX\text{-}CM\text{-}DC\ CONN}$ test configuration.

~~E.6~~E.7 Compliance

~~E.6.1~~E.7.1 Host and Device Product Compliance

Host and device products with re-timers shall meet the transmitter compliance requirements defined in Section 6.7.3 and the receiver jitter tolerance requirements defined in Section 6.8.5 of the base specification. During all host or device product compliance testing the re-timer shall be in the normal operation state (U0).

~~E.6.2~~E.7.2 Component-Level Re-timer Compliance

Re-timer products may also undergo component level compliance testing. The transmitter and receiver compliance requirements specified in Sections 6.7.3 and 6.8.5 apply to component level compliance testing. When undergoing component level compliance testing for the transmitter, the re-timer shall generate appropriate compliance patterns. When undergoing component level compliance testing for the receiver, the re-timer shall be placed into loopback mode.

E.7.3 Component-Level LRD Conformance

The Re-driver for on-board applications may also undergo component level compliance test. The transmitter and receiver compliance requirements and the test environment are specified in Section E.6.4.