

## USB ENGINEERING CHANGE NOTICE – May 21 '12

**Title: HSIC ECN**

**Applies to: High Speed Inter Chip Specification, Rev 1.0**

### Summary of ECN:

- Modifications to the HSIC electrical parameters concerning Total Capacitive load, Slew Rate (Rise and fall) of Strobe and Data, Receiver Data Setup value, bus keepers and Strobe Frequency are specified.
- An optional keeper mechanism is specified to improve interoperability when the power up sequence between a host and a device cannot be guaranteed. An alternative usage is also defined for implementations that cannot guarantee the timing required for enabling and disabling the keepers.
- Clarifications to the HSIC protocol specification concerning CONNECT signaling are described.
- Includes supplemental information on the receiver implementation for data signaling. An adaptive receiver recommendation is made to ensure backwards compatibility with any existing legacy HSIC devices.

### Reasons for ECN:

- The changes to the electrical parameters are intended to simplify implementations and improve electrical inter-operability or to fix an erratum in the original specification.
- The optional keeper mechanism specified improves interoperability when the power up sequence between a host and a device cannot be guaranteed. An alternative usage is also defined for implementations that cannot guarantee the timing required by the specification for enabling and disabling the keepers.
- The changes to CONNECT signaling are intended to clarify the intent of the specification.
- An adaptive receiver recommendation for data signaling is made to ensure backwards compatibility with any existing legacy HSIC devices.

### Impact on existing peripherals and systems:

- The electrical and protocol timing changes are intended to clarify and simplify implementations, are backwards compatible and will not impact existing implementations.
- The proposed spec changes will help simplify future implementations of HSIC PHYs
- The adaptive receiver recommendation should have zero impact. This is a clarification which will ensure interoperation with existing USB HS signaling and HS hubs. There are no known existing HSIC receivers that are designed to filter HSIC packets that transmit data using inverted encoding. The reason for this is that the UTMI specification defines an identical encoding, and that has been used by all known HSIC receiver implementations.

### Hardware Implications:

- The electrical and protocol timing changes are intended to clarify and simplify implementations, are backwards compatible and will not impact existing implementations.

## U S B E n g i n e e r i n g C h a n g e N o t i c e

- The specified spec changes will help simplify future implementations of HSIC PHYs

### **Software Implications:**

- None

### **Compliance Testing Implications:**

- Not Applicable

## Specification Changes:

### 1. Total Capacitive Load:

Current Spec:

Page 16, Section 4 of the spec lists a table that specifies:

- Total Capacitive Load (CL) range as 3 pf to 14 pf.
- $T_i$ ,  $T_L$  and  $T_S$  as normative values.

Proposed Change:

Modify the table in Page 16, Section 4 of the spec as below:

- Replace the row specifying the Total Capacitive Load (CL) range with a row specifying the Input Buffer Load (BL) range as 1 pf to 5 pf
- Circuit Board Trace Length (TL) range as 2 cm to 10 cm
- Specify "Note 4" in the Comments Column for the rows corresponding to  $T_i$ ,  $T_L$  and  $T_S$
- At the bottom of Table add Note 4) Informative values only.

Reason: Current specified values do not accurately reflect actual systems. For actual systems the connection is a transmission line and the distributed capacitance must not be included as a lumped load. A realistic input buffer load range is 1-5 pf. The minimum trace length specified will allow slew rates to be tuned for a minimum load of 3pf (1 pf load + 2pf trace). Appropriate design of the trace with respect to  $T_i$ ,  $T_L$  and  $T_S$  values is assumed to be an implementation-specific exercise. As a result these values are now marked as informative.

### 2. Slew Rate (Rise and Fall) Strobe and Data

Current Spec:

Page 16, Section 4 of the spec lists a table that specifies:

- Slew Rate ( $T_{SLEW}$ ) range as  $0.6 \cdot V_{DD}$  to 1.2 V/ns

Proposed Change:

Modify the table in Page 16, Section 4 of the spec as below:

- Specify the Slew Rate( $T_{SLEW}$ ) range as 0.7 V/ns to 2 V/ns depending on the operating process-voltage-temperature condition.
- Specify "Note 6" in the Comments Column for the row corresponding to  $T_{SLEW}$
- At the bottom of Table add Note 6) Slew measured at the transmitter with a capacitive test load of 3pf.

Reason: Current specified values are too slow and do not allow any margin for crosstalk and impedance mismatch.

### 3. HSIC receiver – Setup Time

Current Spec:

Page 16, Section 4 of the spec lists a table that specifies:

- Receiver Data Setup (TS) value at 300 ps

Proposed Change:

Modify the table in Page 16, Section 4 of the spec as below:

- Receiver Data Setup (TS) value at 365 ps
- Add a row that specifies the transmitter uncertainty (TT) at 365 ps

Reason: At the transmitter side several design restrictions can be avoided if the current 300ps value is increased. This proposal calls for dividing the setup budget (1.042 ns) in the following manner: 35% for the receiver, 35% for the transmitter and 30% for the board. ( $0.35 \cdot 1.042\text{ns} = 365\text{ps}$ )

### 4. Strobe Frequency

## U S B E n g i n e e r i n g C h a n g e N o t i c e

Current Spec:

Page 16, Section 4 of the spec lists a table that specifies:

- STROBE Frequency ( $F_{\text{STROBE}}$ ) range as 239.988 MHz to 240.012 MHz.

Proposed Change:

Modify the table in Page 16, Section 4 of the spec as below:

- STROBE Frequency ( $F_{\text{STROBE}}$ ) range as 239.88 MHz to 240.12 MHz.

Reason: Current specified values are incorrectly calculated as per the 500ppm note.

### 5. Bus Keepers Electrical Parameters

Current Spec:

Page 16, Section 4 of the spec lists a table that specifies:

- I/O Weak Keepers ( $I_L$ ) range as 20 to 70uA

Proposed Change:

Modify the table in Page 16, Section 4 of the spec as below:

- Remove the I/O Weak Keepers ( $I_L$ ) row
- Add a row specifying the pullup/pulldown bus keeper resistor ( $R_K$ ) with a range as 20K $\Omega$  to 50K $\Omega$
- Add a row specifying alternate pullup resistor ( $R_{\text{PU-ALT}}$ ) with a range as 2K $\Omega$  to 5K $\Omega$
- Add a row specifying device alternate pulldown keeper resistor ( $R_{\text{PD-ALT}}$ ) with a range as 20K $\Omega$  to 50K $\Omega$
- In the I/O Input Impedance ( $Z_i$ ) row, increase the minimum value to 240 K $\Omega$
- Specify "Note 5" in the Comments Column for the row corresponding to  $R_K$ ,  $R_{\text{PU-ALT}}$  and  $R_{\text{PD-ALT}}$ .
- At the bottom of Table add Note 5) The bus keeper values implemented depend on power up sequence assumptions. Please see Section 3.5 for details.

Reason: It is not clear how the current specified current is measured. If this parameter is to be defined as a current there should be a V/I characteristics chart so the designer knows that bus keeper behavior is the expected in all conditions. Proposed solution converts existing specified current range based on ohms law.

### 6. Bus Keepers Usage

Current Spec:

Page 16, Section 3.1.1 of the spec states – "USB host, hub and peripherals must be constructed in such a way to ensure that the STROBE and DATA signals do not float to an undetermined value, or a false connect may be detected. An example implementation to prevent this floating condition from occurring is to incorporate a clamping diode on both STROBE and DATA."

Proposed Change:

Modify Section 3.1.1 of the spec as below:

"USB host, hub and peripherals must be constructed in such a way to ensure that the STROBE and DATA signals do not float to an undetermined value, or a false connect may be detected. Please refer to Section 3.5 for details on requirements for bus keepers during the IDLE state and the discovery sequence."

Modify Section 3.5 of the spec as below:

"

3.5 Bus Keepers in IDLE bus state and Discovery Sequence

## U S B E n g i n e e r i n g C h a n g e N o t i c e

Bus Keepers will be asserted by the downstream facing Host or Hub interface on the STROBE and DATA lines to maintain the bus IDLE state. These bus keepers must be disabled 1 Strobe-period after any non-IDLE bus state is detected, and must be enabled 1 Strobe-period after IDLE is detected. An implementation that cannot meet this requirement must keep the IDLE bus keepers always enabled. This alternative approach incurs the penalty of additional power consumed by the bus keepers.

In a deterministic discovery sequence in which the host is always powered-up before the device, the host must implement either the pullup/pulldown keeper resistor ( $R_K$ ) or the alternate pullup resistor ( $R_{PU-ALT}$ ) as defined in this ECN. In this case if the device implements the alternate pulldown bus keeper resistor ( $R_{PD-ALT}$ ) it must be disabled.

If a deterministic discovery sequence cannot be guaranteed the host must implement the alternate pullup resistor ( $R_{PU-ALT}$ ) and the device must implement the alternate pulldown bus keeper resistor ( $R_{PD-ALT}$ ) as defined in this ECN. Also in this case, the device must turn-on  $R_{PD-ALT}$  on both strobe and data when powered up and enabled and must disable  $R_{PD-ALT}$  within 1 strobe period after the start of connect signaling.”

### 7. Connect Signaling

Proposed Change: Replace text in Section 3.3 with “CONNECT (STROBE line low, DATA line high) for a minimum 2 strobe periods”. This change clarifies that the peripheral must send the connect signaling for a minimum of 2 strobe periods. The host must detect the connect signaling if seen for a minimum of 1 Strobe-period.

Reason: Overall intention of the spec is that the CONNECT detection would typically be implemented as a debounced edge detection (not a timed event), and since 1 STROBE period is adequate for the detection on the receiver side (whether it is edge detected or a timed event), the driver side was defined to be 2 STROBE periods to ensure that a minimum of 1 STROBE period was available to the receiver under all conditions. The proposed change will help clarify the intent of the spec.

### 8. Data Signaling

The following text additions are proposed to the High Speed Inter Chip Specification, section 3.4 Data Signaling: (the existing text in section 3.4 remains, the text below is added as supplemental information after the existing text)

As noted in Figure 3 the first and last bit of DATA are sampled at the rising edge of STROBE which implies that only an odd number of bits can be transmitted. Implementations must ensure that a padding bit be inserted so that an odd number of bits are always transmitted.

The HSIC receiver should be designed to be adaptive, meaning that the HSIC receiver does not filter packets based on a USB “J” or USB “K” encoding, but instead uses the decoded NRZI (DENZRI) and unstuffed data (the raw data). Please see the example below showing SYNC packet encoding and inverted encoding, and how the raw data is identical.

Additionally, the HSIC transmitter should be designed to transmit packets as defined in the USB specification with the following encoding association. A logic ‘1’ state on the HSIC interface is equivalent to a high-speed (HS) USB ‘J’. A logic ‘0’ state on the HSIC interface is equivalent to a high-speed (HS) USB ‘K’.

When the HSIC interface is included as part of a hub and is connected to a high-speed hub repeater path, the repeater path data will be transmitted with the encoding that is on the repeater path.

