

# **Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification**

**Revision 1.2**

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# 1 Preface

## 1.1 Scope of this Revision

This supplement defines eUSB2 PHY layer requirement and signaling attributes. Protocol behavior which is not explicitly called out in this document shall remain the same as defined in USB Revision 2.0 specification.

## 1.2 Revision History

Revision Number	Date	Description
1.0	1 August, 2014	Initial release
1.1	03 November 2018	Updated Release containing all ECNs
1.2	15 November 2021	<p>V1.1 ECN incorporation and editorial update. Additional non-editorial changes include the following</p> <ol style="list-style-type: none"> <li>1. Revoked eUSB2v1.1ECR_MinimizingDribble_e2U</li> <li>2. Document wide replacement of L1Sleep with SleepM and Suspend with SuspendM.</li> <li>3. Main updates in Chapter 3 include <ol style="list-style-type: none"> <li>a. Table 3-1 updated notes and reformatted table to distinguish eD+ and eD- states.</li> <li>b. Table 3-2: corrected the range of <math>V_{RX\_DIF}</math></li> <li>c. Figure 3-7: Clarified FS/LS EOP detection requirement at eUSBr</li> <li>d. Figure 3-9(b): Clarified bus state mapping of a HS device connected to a FS host after device chirp</li> <li>e. Section 3.3.4.2.2 <ol style="list-style-type: none"> <li>i. Added clarification for eUSPh and eDSPp to enable HS termination upon observing eSE0 to avoid potential SE EOReset corruption</li> <li>ii. Consolidated requirement for HS USB 2.0 Bus Reset</li> <li>iii. Changed the name of <math>T_{PR\_RESET\_FROM\_HS\_TO\_FS}</math> timer to <math>T_{PR\_RESET\_FROM\_HS}</math> timer and summarized its operational requirements</li> </ol> </li> <li>f. Section 3.3.1 added clarification of transmitting SYNC pattern and notes about crossover glitches. Also added bullet about driving or maintaining with <math>R_{PD}</math> after <math>T_{eSE0\_DR\_LSFS}</math>.</li> <li>g. Section 3.3.3 added requirement to map SE0 detected during cross-over of USB 2 signal to eUSB2.</li> <li>h. Section 3.3.4.1.2: added a requirement for peripheral repeater to transmit FS EOReset with reduced <math>T_{STROBE}</math> duration. <math>T_{STROBE}</math> definition is updated accordingly.</li> <li>i. Section 3.3.5: Added to summarize L1 and L2 Suspend entry operation</li> <li>j. Section 3.3.5.1.2 added requirement about not re-transmitting CM.Lx.</li> <li>k. Section 3.3.6.2.2: added clarification for eUSPh and eDSPp to enable HS termination upon observing eSE0 to avoid potential SE EOReset corruption</li> <li>l. Section 3.3.7: added optional normative feature of auto-resume (new to v1.2)</li> <li>m. Sections 3.3.7.1.2: Introduced and formalized the TSE0_FILTER SE0 filter timer definition to replace the non-activity timer</li> <li>n. Section 3.3.7.1.2: added Table 3-3 for USB 2.0 to eUSB2 bus state mapping after EOWake without Resume</li> <li>o. Clarified CM Recovery and retry requirements</li> <li>p. Sections 3.3.9.2/3.3.11: added for XeSE1/eSE1 transmit and detection recommendation</li> </ol> </li> <li>4. Main updates Chapter 4 include <ol style="list-style-type: none"> <li>a. Figure 4-7: added missing transition conditions of the state machine</li> <li>b. Section 4.3.3.1 added note to t4 and t5 in timing of Figure 4-8 with respect to UTMI+ xcvrselect, opmode, and termselect.</li> <li>c. Figure 4-9 updated to J driven on linestate after t5.</li> <li>d. Section 4.3.4: added L0 for completeness</li> </ol> </li> </ol>

		<ul style="list-style-type: none"> <li>e. Section 4.3.5: editorial with section re-organization</li> </ul>
		<ul style="list-style-type: none"> <li>5. Main updates of Chapter 5 include                             <ul style="list-style-type: none"> <li>a. Updated state machine and formalize the operation requirements and transition conditions in each sub-states</li> <li>b. Figure 5-10: adding missing transitions in the Lx sub-state machine</li> <li>c. timer</li> <li>d. Section 5.5: removed inconsistencies and added additional clarifications</li> <li>e. Section 5.4.1.1.2 Added text for eUSPr.</li> </ul> </li> <li>6. Chapter 6: clarified back to back CM transmission rule and RAP format</li> <li>7. Various other editorial corrections (links, references, etc.)</li> </ul>

## 2 Introduction

### 2.1 Acronyms and Terms

This section lists and defines terms and abbreviations used throughout this specification.

**Table 2-1: Acronyms**

Acronyms	Terms
Attach	This specification makes a distinction between the words “attach” and “connect”. A downstream device is attached to an upstream port when there is a physical cable between the two
Analog Ping	An analog pulse of a differential signal with variable pulse width used by an upstream eUSB2 port in high-speed operation to indicate its presence
bus state	The electrical state of D+/D- of the USB 2.0 bus or eD+/eD- of the eUSB2 bus
Connect	A downstream device is connected to an upstream port when it is attached to the upstream port, and when the downstream device has pulled either the D+ or D- data line high through a 1.5 kΩ resistor, to enter low-speed, full-speed or high-speed signaling.
D+	USB 2.0 data+ pin
D-	USB 2.0 data- pin
DRD	Dual role device capable of host function and device function
DFP	Downstream-facing port
Digital Ping	A single-ended digital pulse of various pulse width used in the eUSB2 operation as a ping or an acknowledgement
Downstream	The direction of data flow from the host or away from the host. A downstream port is the port on a hub/repeater toward the Device direction that generates downstream data traffic from the hub. Downstream ports receive upstream data traffic
eD+	eUSB2 data+ pin
eD-	eUSB2 data- pin
eDSPn	Downstream eUSB2 port in native mode
eDSPp	Downstream eUSB2 port of the peripheral repeater
eDSPr	Downstream eUSB2 port facing host repeater
EOR	End of reset(EOReset) or end of Resume(EOResume)
EOS	Electrical Over Stress
EOW	End of Wake(EOWake)
eSE0	Single-ended logic '0' at both eD+ and eD-

Acronyms	Terms
eSE1	Single-ended logic '1' at both eD+ and eD-
eUSBr	An eUSB2 port in repeater mode before or after it is configured to eDSPr or eUSPr
eUSPh	Upstream eUSB2 port of the host repeater
eUSPn	Upstream eUSB2 port in native mode
eUSPr	Upstream eUSB2 port facing peripheral repeater
FS	Full-Speed
HS	High-Speed
L1	LPM-L1
L2	Suspend
LineState	USB 2.0 bus state defined by UTMI+
LPM	Link Power Management
LS	Low-Speed
Lx	Link power management states, includes both L1 and L2.
POR	Power On Reset
RAP	Register Access Protocol
Redriver	Analog repeater
Retimer	Retiming repeater
Repeater	General term of a bridge. In this specification, it refers to a non-linear eUSB2-USB2 redriver.
SCM	Start of Control Message
SDP	Standard downstream port
SoC	System-on-chip
Upstream	The direction of data flow towards the host. An upstream port is the port on a device toward the Host direction that generates upstream data traffic from the hub/repeater. Upstream ports receive downstream data traffic.
UUSP	Upstream USB 2.0 port of the peripheral repeater
UDSP	Downstream USB 2.0 port of the host repeater
UFP	Upstream-facing port.
USB OTG	USB On-the-go
USB session	The lifetime of a USB port in connected state
UTMI/UTMI+	The interface between the protocol layer and the eUSB2 PHY. Refer to the UTMI/UTMI+ specification.
Walk-up port	Ports which have physical connectivity through the connector
XeSE1	Extended eSE1

## 2.2 Terminology

“Shall” is normative and used to indicate mandatory requirements which are to be followed strictly in order to conform to this standard.

“Should” is normative and used to indicate a recommended option or possibility.

“May” is normative and used to indicate permitted behavior.

“Can” is informative and used to indicate behavior which is possible or may be seen.

The use of “must” and “will” is deprecated for requirements and shall only be used for statements of fact.

## 2.3 Motivation

The success of USB 2.0 technology has enjoyed wide adoption in almost every computing device, with tremendous ecosystem support not only in terms of device choice to support various platform features, but also in terms of technology development with well-established hardware IP portfolios and standardized software infrastructure. It is foreseeable that the great asset of USB 2.0 technology will continue to benefit the ecosystem for years to come.

As power efficiency becomes increasingly critical in today's computing devices, there is a need for IO technology to be optimized for both active and idle power. USB 2.0 technology, originally optimized for external device interconnect, is primed to be enhanced for inter-chip interconnect such that the link power can be further optimized.

Meantime, silicon technology continues to scale. Device dimensions are getting smaller and therefore more devices can be packed onto a single integrated chip. However, the device reliability challenge arising from the densely packed transistors has become more profound. The manufacturing cost for an advanced process technology to support 3.3V IO signaling has grown exponentially. A low voltage USB 2.0 solution is therefore required to address the gap.

In summary, eUSB2 is introduced to address the following:

1. IO Power Efficiency
  - Improve both the link active and idle power efficiency.
2. Process scalability
  - Provide a low voltage USB 2.0 PHY solution to eliminate 3.3V IO signaling requirement, which allows the process technology to continue to scale for many generations to come.
3. Implementation simplicity
  - The PHY analog content is reduced. Digital mechanisms are employed for PHY functionality, for example, device disconnect detect.
4. Support both USB 2.0 inter-chip and out-of-the-box devices
  - Though eUSB2 and USB 2.0 are not electrically compatible, a mechanism is defined for eUSB2 to support standard USB 2.0 devices.

Table 2-2 tabulates the key attributes of eUSB2 technology in comparison to other USB interfaces.

**Table 2-2: Comparison of Various USB Interfaces**

	<b>USB2</b>	<b>IC-USB</b>	<b>HSIC</b>	<b>ULPI</b>	<b>eUSB2</b>
Interface Pin (SoC view)	2-pin	2-pin	2-pin	12-pin	2-pin
Supported data rate	low-speed, full-speed and high-speed	low-speed and full-speed	high-speed	low-speed, full-speed and high-speed	low-speed, full-speed and high-speed
Connectivity	Inter-chip and out-of-the-box	Inter-chip	Inter-chip	Inter-chip	Inter-chip and out-of-the-box USB 2.0 connectivity through repeater
Signaling Voltage Requirement	Max 3.3V	Multiple voltage	1.2V	Vendor specific. Typically	Max 1.2V

	<b>USB2</b>	<b>IC-USB</b>	<b>HSIC</b>	<b>ULPI</b>	<b>eUSB2</b>
		classes, from 1V to 3.3V		1.8V and 3.3V	
Recommended trace length support	Long	short	short	short	Medium to long

## 2.4 eUSB2 PHY Feature

eUSB2 is fully compliant to the USB 2.0 layer architecture with the following features and characteristics.

- Supports high-speed, full-speed, and low-speed operation.
  - High-Speed:
    - Low voltage differential signaling
  - Low-Speed/Full-Speed:
    - Single-ended digital low-voltage signaling.
- Supports selected single speed configuration in native mode.
- Supports USB 2.0 operation based on repeater architecture.
- Supports link power management LPM-L1 (L1) and Suspend (L2).
- eUSB2 implementation is based on UTMI/UTMI+ Parallel Mode. FS/LS Serial Mode is out of scope for eUSB2. Note that implementations based on UTMI/UTMI+ may vary. In the rest of the specification, UTMI/UTMI+ is quoted as a reference to describe the interface between the protocol layer and the eUSB2 PHY.
- Supports register access protocol (RAP) for eUSB2 device or repeater configurations.
- Fully compliant to USB 2.0 base spec at the protocol layer.
- No change to USB 2.0 software programming model.
- Not compatible with the physical layer defined by USB 2.0.
- Not compatible with standard USB 2.0 connectors defined by USB 2.0 and its derivatives.

Shown in Figure 2-1 is a description of eUSB2 scope. An implementation that supports UTMI/UTMI+ as the standard interface between the protocol layer and the physical layer is used as an example.

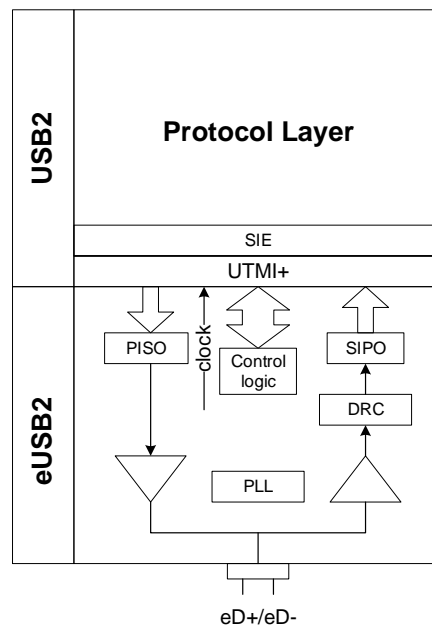


Figure 2-1: eUSB2 Under USB 2.0 Layer Architecture

## 2.5 eUSB2 Modes of Operation

eUSB2 supports two modes of operation: native mode and repeater mode.

Native mode refers to a host port and a device port both implementing an eUSB2 PHY and communicating based on eUSB2 signaling. Native mode eUSB2 is used for inter-chip interconnect. Single speed configuration is allowed in native mode.

Repeater mode refers to an eUSB2 port communicating with a USB 2.0 port through a repeater that translates between eUSB2 signaling and USB 2.0 signaling. Repeater mode may also be used between two eUSB2 ports communicating with each other through two repeaters, such a case typically involves applications with USB 2.0 receptacles at both sides of the ports.

Example usages of eUSB2 in native mode and repeater mode are shown in Figure 2-2 and Figure 2-3. Note that Figure 2-3, both the SOC's and repeaters may be dual role capable. Later sections in the specification describe the configuration and operation of this.

An eUSB2 implementation on an SoC may support both native mode and repeater mode operation with slight differences in accommodation for repeater operation. This gives the system designer the flexibility to determine the mode of operation of the eUSB2 port on an SoC.

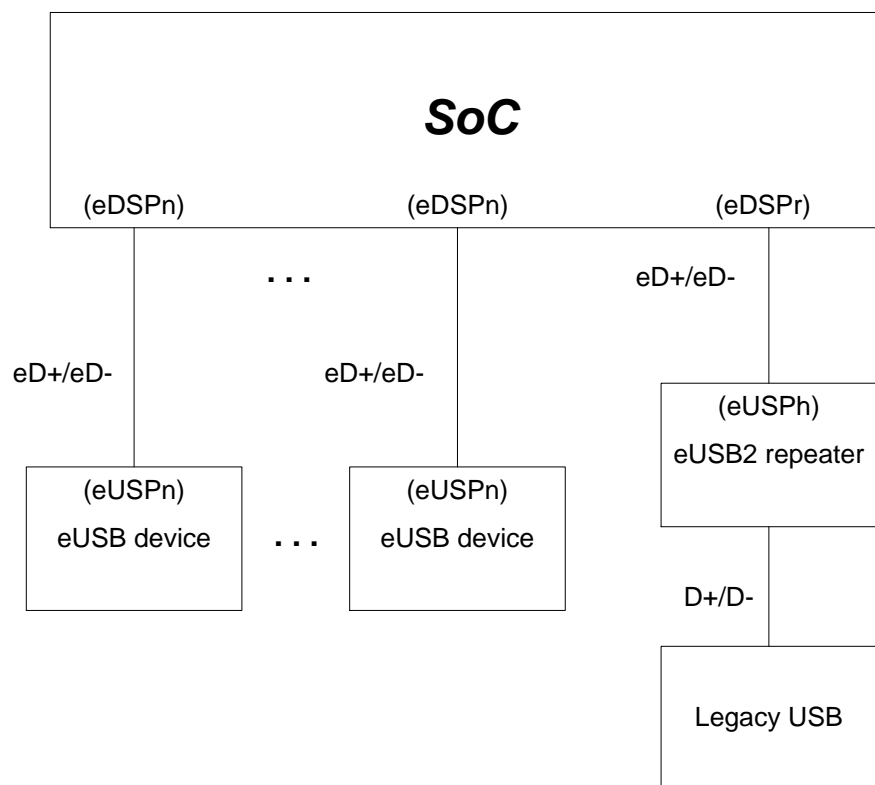


Figure 2-2: Typical eUSB2 Use Cases



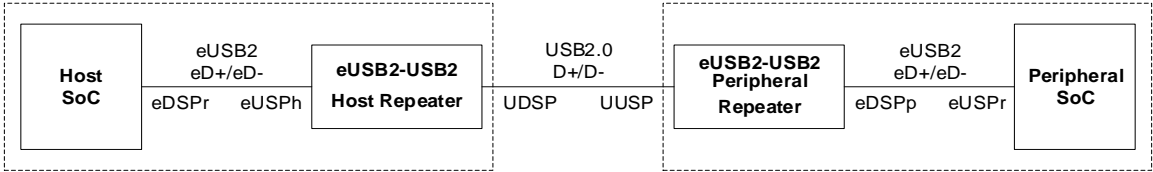


Figure 2-3: Example eUSB2 With Host and Device Side Repeaters

Table 2-3 describes the number of hubs that are supported relative to the number of eUSB2 repeaters present between the host and peripheral where all the hubs are operating at HS or all are operating at FS. It does not attempt to define mixed use cases, where one or more hubs connected at the host operate at HS and one or more at the peripheral operate at FS. Per USB 2.0, a HS-capable hub must operate at FS when its upstream-facing port is connected behind a host or hub that is operating at FS or that is not HS-capable. A legacy USB 1.x host or hub is not HS-capable and necessarily operates at FS.

Table 2-3: Number of Hubs Supported with Host and/or Peripheral Repeater

Number of eUSB2 Repeaters	Number of Hubs Operating at HS	Number of Hubs Operating at FS	Notes
1	4	2	Number of hubs operating at FS is reduced due to $T_{e\_to\_U\_DJ1}$ and $TRJR1$ .
2	3	1	Number of hubs operating at HS is reduced due to SOP truncation and EOP dribble
0	5	5	non-eUSB2 system for reference

2.6 Related Documents

eUSB2 only defines the physical layer. The protocol layer is defined in the USB 2.0 base specification.

The following is a list of related documents.

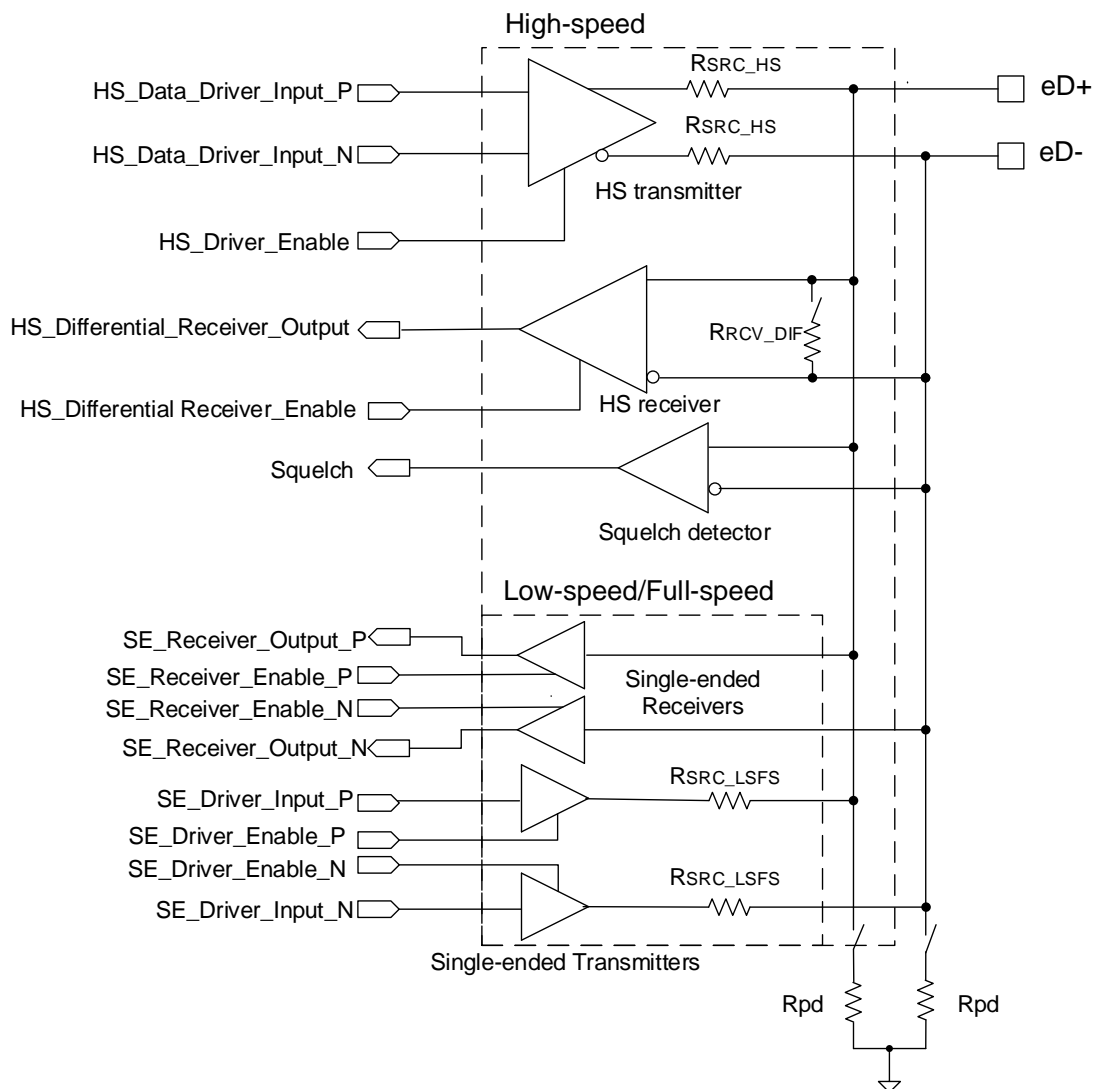
USB 2.0	Universal Serial Bus Revision 2.0 Specification including ECNs and errata.
[USB2 OTG]	On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification.
[USB Type-C]	Universal Serial Bus Type-C Cable and Connector Specification Revision 1.3
[UTMI+ v1.0]	USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Specification.

### 3 eUSB2 PHY Architecture and Operation

This chapter describes the eUSB2 PHY architecture and its operation. Although the focus is on native mode, most of native mode operation also applies to repeater mode.

#### 3.1 PHY Architecture

A conceptual block diagram of the eUSB2 PHY is shown in Figure 3-1. It supports three data rates defined by USB 2.0. A differential transceiver and a low power squelch detector are needed for data transfer at high-speed. Two pairs of single-ended CMOS buffers are employed to carry out low-speed/full-speed data transfer, control signaling during initialization and link power state transitions.



**Figure 3-1: eUSB2 Physical Layer Transceiver Block Diagram**

An eUSB2 implementation shall contain the following building elements.

- A port shall implement two pull-downs,  $R_{PD}$ , intended to hold the eUSB2 bus to ground during power-up or when the link is idle. Note: Under a general scenario,

upon power-up, these pull-downs shall be enabled. It is implementation specific to allow disabling for testing or debug.

- A low-speed/full-speed eUSB2 port is fully digital. A low-speed/full-speed transceiver shall meet the following requirements.
  - The port shall implement a pair of low-speed/full-speed single-ended transmitters.
  - The port shall implement a source-series termination at each transmitter.
  - The port shall implement a pair of low-speed/full-speed single-ended receivers and they shall be enabled always with the exception that they may be optionally disabled during a HS USB 2.0 packet is being transfer.
- A high-speed transceiver shall meet the following requirements.
  - The port shall implement an analog transceiver for low swing differential signaling.
  - The port shall employ embedded clocking compliant to USB 2.0.
  - The port shall implement a squelch detector.
  - The port shall implement a source-series termination at its transmitter.
  - If enabled, the port shall implement a differential receiver termination with the center tap capacitance to ground. Note that not employing ground termination of the differential receiver termination avoids overloading the SE (Single-ended) transmitter in HS operation when a control message may be issued during HS idle. Refer to Section 3.3.8 for control message definition.
  - The receiver termination shall always be enabled in repeater mode
  - The default receiver termination shall be disabled in native mode. A downstream port may alter the termination scheme during Port Configuration. Refer to Section 4.2.2 for the details.

## 3.2 Bus State and Signaling

### 3.2.1 Low-Speed/Full-Speed Bus State and Signaling

The FS/LS eUSB2 operations are based on single-ended signaling. A FS packet consists of Data J, Data K, and EOP. A Data J or Data K is represented as logic '0' or logic '1' at eD-, while logic '0' is maintained at eD+ through  $R_{PD}$ . An EOP is presented in two different formats, one in repeater mode when the repeater is forwarding a USB 2.0 packet from D+/D- to eD+/eD-, and the other in repeater mode when the repeater is forwarding an eUSB2 packet from eD+/eD- to D+/D-, or in native mode between eDSPn and eUSPn. A LS packet consists of the same Data J, Data K, and EOP as FS, except on opposite bus lines with Data on eD+ and EOP on eD-. In addition, the L0 idle and L1/L2 idle state of the eUSB2 bus in either native mode or repeater mode is presented as eSE0.

Table 3-1 summarizes the FS/LS bus states, and packet representations.

**Table 3-1: eUSB2 Low-Speed/Full-Speed Bus State Representations**

Bus State	Signaling Levels		
	At the Transmitter	At the Receiver	
Logic '1'	$> V_{OH(min)}$	$> V_{IH(min)}$	
Logic '0'	$< V_{OL(max)}$	$< V_{IL(max)}$	
Single-ended 0 (eSE0)	Logic '0' at eD-; Logic '0' at eD+		
Single-ended 1 (eSE1) <sup>1</sup>	Logic '1' at eD-; Logic '1' at eD+		
FS/LS Packet and Bus State Representation			
		eD+	eD-

Data J	FS		Logic '0' <sup>5</sup>	Logic '0' <sup>2</sup>
	LS		Logic '0' <sup>2</sup>	Logic '0' <sup>5</sup>
Data K	FS		Logic '0' <sup>5</sup>	Logic '1'
	LS		Logic '1'	Logic '0' <sup>5</sup>
SE0 <sup>3</sup>	FS		Logic '1'	Logic '0'
	LS		Logic '0'	Logic '1'
End-of-Packet (EOP)  Native mode <sup>4</sup> or eDSPr/eUSPr to repeater	FS	1 <sup>st</sup> UI	Logic '1'	Logic '0' <sup>4</sup>
		2 <sup>nd</sup> UI	Logic '0'	
		3 <sup>rd</sup> UI	Logic '1'	
	LS	1 <sup>st</sup> UI	Logic '0' <sup>4</sup>	Logic '1'
		2 <sup>nd</sup> UI		Logic '0'
		3 <sup>rd</sup> UI		Logic '1'
End-of-Packet (EOP)  Repeater to eDSPr/eUSPr <sup>6</sup> :	FS	1 <sup>st</sup> UI	Logic '1'	Logic '0' <sup>6</sup>
		2 <sup>nd</sup> UI	Logic '0'	
		3 <sup>rd</sup> UI		
	LS	1 <sup>st</sup> UI	Logic '0' <sup>6</sup>	Logic '1'
		2 <sup>nd</sup> UI		Logic '0'
		3 <sup>rd</sup> UI		
L0/L1/L2 Idle		FS/LS	eSE0	
Reset/Resume/Remote Wake		Refer to Section 3.3 for details.		
Connect/Disconnect		Refer to Chapters 4 and 5 for details.		

**Note 1:** Singled-ended eSE1 is used in eUSB2 to distinguish various control signals from an FS/LS eUSB2 packet. Refer to the remaining sections of this chapter for details.

**Note 2:** Refer to Section 3.3.1 for implementation specific exceptions relative to driving vs. maintaining Logic '0'.

**Note 3:** USB 2.0 Bus Reset from FS/LS in native or peripheral repeater modes or FS/LS disconnect in host repeater mode. Also see Section 3.3.4 and Chapters 4 and 5.

**Note 4:** Refer to Section 4.2.3.1 for digital ping transmission during EOP.

**Note 5:** Refer to Section 3.3.3 for glitch filtering during crossover.

**Note 6:** Refer to Section 3.3.3 for EOP variation.

### 3.2.2 Low-Speed/Full-Speed Idle State Transition

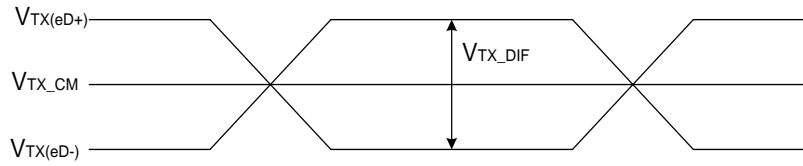
Low-Speed/Full-Speed idle state (eSE0) is maintained by the pull-down resistors ( $R_{PD}$ ) implemented at a downstream port. To ensure a swift transition to idle state (eSE0) or logic '0', the port shall drive the bus to eSE0 or logic '0' for  $T_{eSE0\_DR\_LSFS}$  when transitioning from a non-eSE0 before disabling its transmitters to allow the pull-down resistor to hold eSE0. Refer to Table 7-16 for timing detail.

### 3.2.3 High-Speed Bus State and Signaling

High-Speed bus states of J and K are maintained by driving low swing differential voltage on eD+ and eD- during terminated and un-terminated conditions. Figure 3-2 defines the high-speed transmitting signals at eD+ and eD-, each is denoted as  $V_{TX(eD+)}$  and  $V_{TX(eD-)}$ . The differential signal  $V_{TX\_DIF\_TERM}$  (when terminated) or  $V_{TX\_DIF\_UNTERM}$  (when un-terminated) and the common mode signal  $V_{TX\_CM}$  are then represented by the following:

$$V_{TX\_DIF} = V_{TX(eD+)} - V_{TX(eD-)}$$

$$V_{TX\_CM} = \frac{V_{TX(eD+)} + V_{TX(eD-)}}{2}$$



**Figure 3-2: High-Speed Differential Signal Representations**

Accordingly, the differential and common mode signals at the receiving port can be similarly represented by the following equations.

$$V_{RX\_DIF\_UNTERM} = V_{RX(eD+)\_UNTERM} - V_{RX(eD-)\_UNTERM}$$

$$V_{RX\_DIF\_TERM} = V_{RX(eD+)\_TERM} - V_{RX(eD-)\_TERM}$$

$$V_{RX\_CM} = \frac{V_{RX(eD+)} + V_{RX(eD-)}}{2}$$

**Table 3-2: eUSB2 High-Speed Bus State Representations**

Bus State		At the source	At the sink
Differential '1'	Terminated	$V_{TX\_DIF} > V_{TX\_DIF\_TERM}(min)$	$V_{RX\_DIF} > V_{SQUELCH\_DIF}(max)$
	Unterminated	$V_{TX\_DIF} > V_{TX\_DIF\_UNTERM}(min)$	
Differential '0'	Terminated	$V_{TX\_DIF} < -V_{TX\_DIF\_TERM}(min)$	$V_{RX\_DIF} < -V_{SQUELCH\_DIF}(max)$
	Unterminated	$V_{TX\_DIF} < -V_{TX\_DIF\_UNTERM}(min)$	
Squelch state		NA	AC: $V_{RX\_DIF} < V_{SQUELCH\_DIF}(min)$ $V_{RX\_DIF} > -V_{SQUELCH\_DIF}(min)$
Data J state:		Differential '1'	
Data K state:		Differential '0'	
L0 idle/L1/L2 state		eSE0	
Start-of-Packet (SOP)		Same as USB 2.0	
End-of-Packet (EOP)		Same as USB 2.0	
End-of-Packet(EOP of $\mu$ SOF in Native Mode)		8 UIs	
Resume/Remote Wake		Same as FS. Refer to Section 3.3.5 and 3.3.6 for details.	

### 3.2.4 High-Speed Idle State Transition

High-Speed idle state is maintained by the pull-down resistors implemented at a downstream port. To ensure a swift transition to idle state (eSE0), the port shall drive the bus to eSE0 for  $T_{eSE0\_DR\_HS}$  when transitioning from a non-eSE0 to idle (eSE0) (i.e. at the end of EOP) before disabling its transmitters. Refer to Table 7-16 for timing detail.

### 3.2.5 High-Speed Squelch Operation

The squelch detector is used by the port to detect high-speed line activity. It is also used under the following scenarios for eDSPn/eUSPn and eUSPh/eDSPp to control the SE receivers.

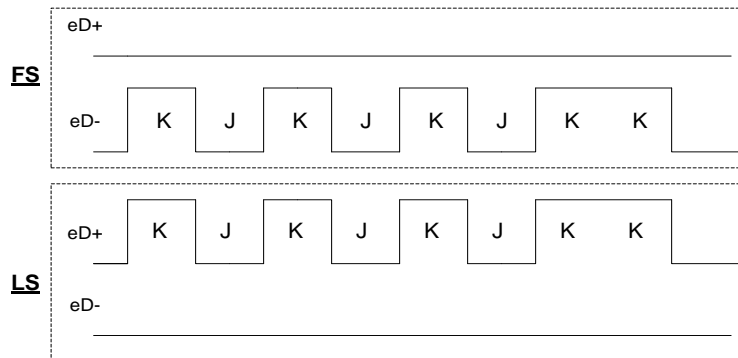
- When in un-squelched condition, an eUSPn, or eUSPh/eDSPp port receiving high-speed data may optionally disable its single-ended receivers.
- Under squelched condition, an eDSPn/eUSPn port shall turn on its single-ended receiver in anticipation of device soft disconnect or USB 2.0 Bus Reset. An eUSPh or eDSPp port shall turn on its SE receivers in anticipation of a control message from eDSPr or eUSPr.

### 3.3 Single-ended (SE) Signaling

eUSB2 employs SE signaling for low-speed/full-speed packet transmission in L0. The SE signal is also used for interactions between the two ports. Interactions include Connect, USB 2.0 Bus Reset, Resume, Remote Wake, high-speed detection and control messages. The interpretation of the SE signals depends on the link state, and the start of the SE signal.

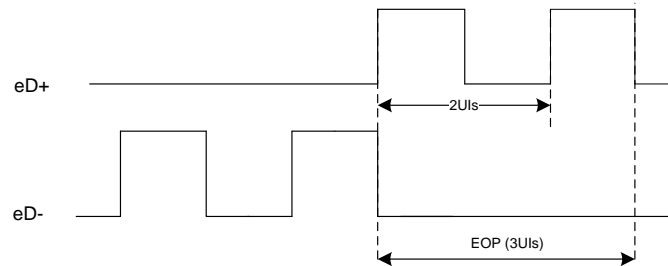
#### 3.3.1 FS/LS SYNC and EOP

- In FS operation, an eUSB2 port shall transmit the SYNC pattern and differential data prior to EOP on eD-. It shall maintain logic '0' on eD+ through  $R_{PD}$  **with the exception of repeater reporting possible SE0 glitches during cross-over. The sync pattern without SE0 crossover glitches** is illustrated in Figure 3-3. Refer also to Section 3.3.3 for cross-over glitch processing.
- In LS operation, an eUSB2 port shall transmit the SYNC pattern **and differential data prior to EOP** on eD+. It shall maintain logic '0' on eD- through  $R_{PD}$  **with the exception of repeater reporting possible SE0 glitches during cross-over. The sync pattern without SE0 crossover glitches** is illustrated in Figure 3-3. Refer also to Section 3.3.3 for cross-over glitch processing.
- For FS and LS operation, while transmitting the SYNC pattern and differential data, the logic '0' for Data J may be driven continuously or may be maintained by  $R_{PD}$  after being driven for  $T_{eSE0\_DR\_LSFS}$ .

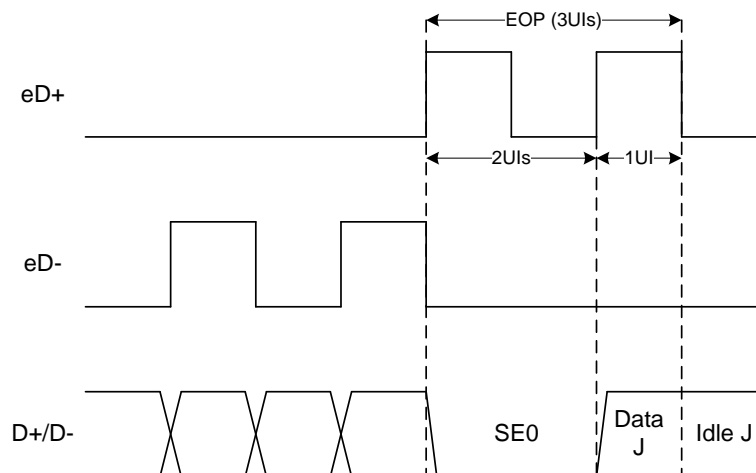


**Figure 3-3: FS/LS SYNC Pattern**

- A FS eUSB2 EOP, transmitted by eDSPn, eDSPr, eUSPn or eUSPr, shall be 3 UIs with the first UI of logic '1', followed by the second UI of logic '0', and a third UI of logic '1' at eD+, while eD- is maintained at logic '0' through  $R_{PD}$ . This is shown in Figure 3-4. Similarly, a LS EOP shall be 3 UIs with the first UI of logic '1', followed by a second UI of logic '0', and the third UI of logic '1' at eD-, while eD+ is maintained at logic '0' through  $R_{PD}$ . Note that the definition of EOP format is optimized towards repeater mode operation to provide timing support when an eUSB2 LS/FS EOP is converted to a USB 2.0 EOP. An example eUSB2 EOP to USB 2.0 EOP conversion in repeater mode is shown in Figure 3-5 and Figure 3-6. Note that in a special case of a FS hub forwarding a LS packet after Preamble, eDSPr may transmit LS EOP that consists of 2 LS UI for SE0 and 1 FS UI for data J. Refer to note 3 of Table 7-2 of the USB 2.0 specification.

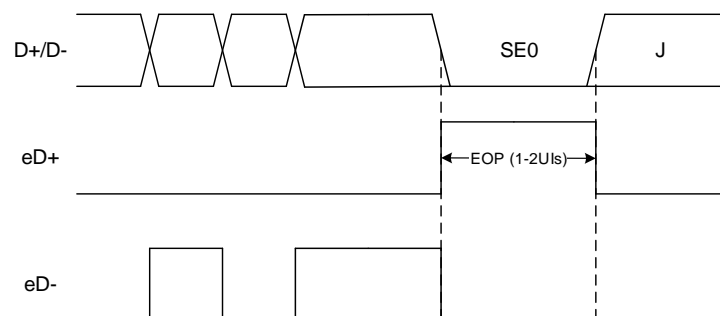


**Figure 3-4: FS EOP Pattern from eDSPr/eUSPr**



**Figure 3-5: Example of eUSB2 EOP to USB 2.0 EOP Conversion**

- A FS EOP transmitted by eUSPh at host repeater to eDSPr, or eDSPp from peripheral repeater to eUSPr, is based on received EOP at D+/D-, which may be between 1 to 2 UIs of logic '1' at eD+, and logic '0' at eD-. This is shown in Figure 3-6. Similarly, a LS EOP may be between 1 and 2 UIs of logic '1' at eD-, and logic '0' at eD+. An eDSPr or eUSPr port shall declare the reception of a FS/LS EOP within 3 UIs upon detecting the start of the EOP.



**(a). FS EOP**



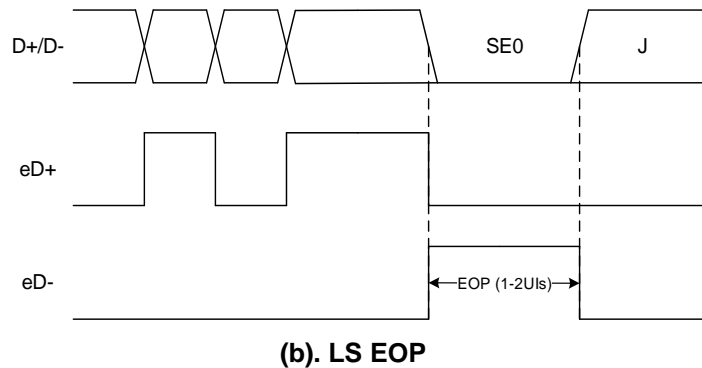


Figure 3-6: FS/LS USB2 EOP to eUSB2 EOP Conversion

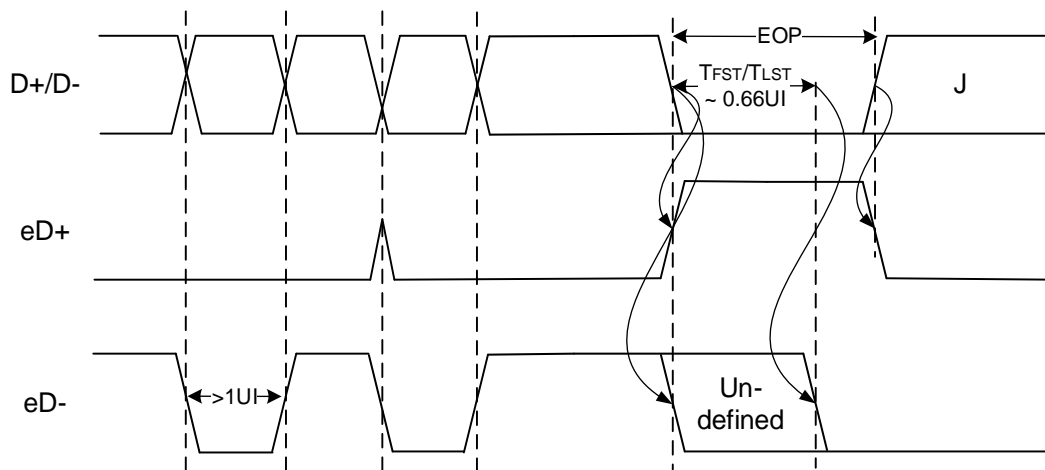
### 3.3.2 Low-Speed Keep Alive

Low-Speed keep alive is a specific case where LS EOP is transmitted by eDSPn or eDSPr to prevent a peripheral device from entering suspend. The low-speed keep alive signaling is the same as LS EOP.

### 3.3.3 Glitch Filtering in FS/LS Repeater Mode

Glitch filtering refers to preserving the USB packet integrity in FS/LS operation. It applies only to repeater mode. A FS/LS receiver at UDSP/UUSP may observe momentary SE0s or SE1s at D+/D- between every K-J or J-K transition within a received USB packet. This is primarily due to un-wanted asymmetry artifact introduced by the channel skew and the transceiver non-ideality. Shown in Figure 3-7 is an illustration of a glitch observed at eD+, and a single-bit data J (logic '0' at eD-) longer than 1 UI, both of which are associated with data crossover transition at D+/D-. Additionally, Figure 3-7 also illustrates the potential overlap or skew between eD+ and eD- which may produce an eSE1 or eSE0 at the beginning of EOP or additional toggling during EOP.

- A repeater shall map SE0 detected during cross-over at its USB 2.0 port to its eUSB2 port based on bus state mapping defined in Table 3-1, followed by driving eD+ (FS) or eD- (LS) to logic '0' for  $T_{eSE0\_DR\_LSFS}$  before switching to  $R_{PD}$ . In a highly unlikely situation where SE0 is detected in consecutive cross-overs and the repeater is still driving logic '0' at eD+ (FS) or eD- (LS) before switching to  $R_{PD}$ , it shall stop driving logic '0' and start mapping SE0 to eD+ (FS) or eD- (LS).
- Upon detecting SE0 at its USB 2.0 port, a repeater shall ensure SE0 is the start of EOP and not due to cross-over, by timing the SE0 duration for more than  $T_{FST}$  or  $T_{LST}$ , defined in Section 7.1.4.1 of USB 2.0 specification, and less than  $0.66UI$ . During this period, the value of the packet data may be undefined (K or J), because packet data is sourced from the FS/LS differential receiver on USB 2.0 and SE0 of EOP at the differential receiver input is out of its DC operating range. Note that  $0.66UI$  is less than  $T_{FEOPR}/T_{LEOPR}$  defined in USB 2.0 Tables 7-9 and 7-10.
  - Upon declaring EOP reception, the repeater shall drive eD- (FS) or eD+ (LS) to logic '0' for  $T_{eSE0\_DR\_LSFS}$  before switching to  $R_{pd}$ .
- eUSPh/eDSPp shall adhere to USB 2.0 Table 7-11 Hub/Repeater Electrical Characteristic in repeating D+/D- to eD+/eD-.
- eDSPr/eUSPr shall perform the glitch filtering as per USB 2.0 specification on eD+ (FS), or eD- (LS).
- eDSPr/eUSPr shall declare the EOP reception at eD+ (FS) or eD- (LS), and ignore any toggling at eD-(FS) or eD+(LS) within the EOP window.



**Figure 3-7: Transition glitches and asymmetry observed at eD- during FS operation**

### 3.3.4 USB 2.0 Bus Reset and End of Reset

eUSB2 signaling for USB 2.0 Bus Reset is different between native mode and repeater mode, and they are described in the following sections.

#### 3.3.4.1 FS/LS Reset

The Reset signaling between the native mode and repeater mode operation are different.

##### 3.3.4.1.1 Native Mode

In native mode, USB 2.0 Bus Reset shall be transmitted by eDSPn to eUSPn based on bus state mapping as defined in

Table 3-1.

- When in FS operation, eDSPn shall transmit Reset by driving logic '1' on eD+ and eUSPn shall map this as USB 2.0 Bus Reset SE0 on its UTMI+ interface to its device controller.
- When in LS operation, eDSPn shall transmit Reset by driving logic '1' on eD- and eUSPn shall map this as USB 2.0 Bus Reset SE0 on its UTMI+ interface to its device controller.
- When in FS operation, eDSPn shall stop driving logic '1' on eD+, and drive a logic '0', then a logic '1' (LS UI duration) on eD+ indicating end of Reset. Note that FS EOReset is defined with LS UI duration to be consistent with repeater implementation, which allows a lower clock frequency to detect end of reset. Refer to Section 3.3.4.1.2 for description.
- When in LS operation, eDSPn shall stop driving logic '1' on eD-, and drive a logic '0', then a logic '1' (LS UI duration) on eD- indicating end of Reset.
- eUSPn shall respond with a digital ping upon detecting the first falling edge of EOP and complete transmitting the digital ping after the last rising edge and before the last falling edge of EOP at the end of Reset to eDSPn. Refer to Section 4.2.3.2.1 for detail timing.
- A unique scenario may exist where a device chirp is observed from eUSPn, but the host does not return with host K-J chirp. In this case, the link will be settled into FS with eDSPn transmitting FS EOReset.
- eDSPn and eUSPn shall map LineState from SE0 to J until it completes EOReset. This is to ensure the host controller not assert TxValid for a packet transmission until the completion of USB 2.0 Bus reset.

- Refer to Figure 3-8 for FS Reset signaling.

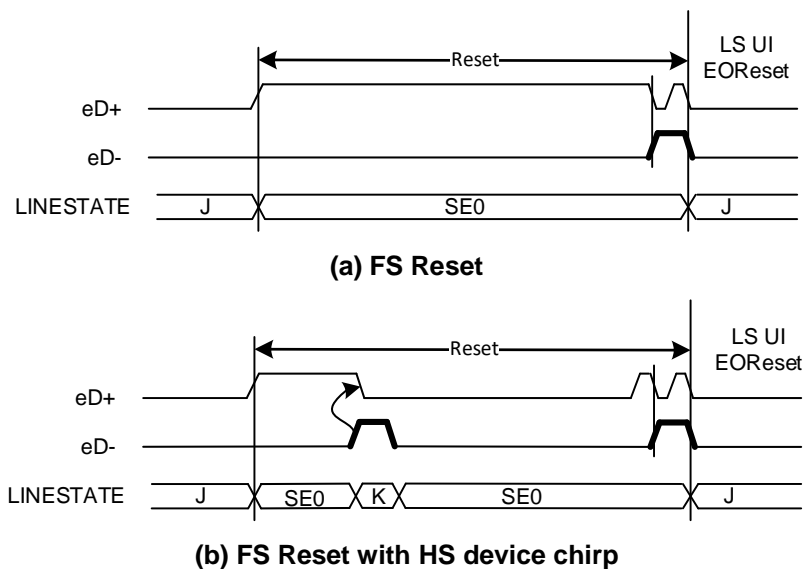
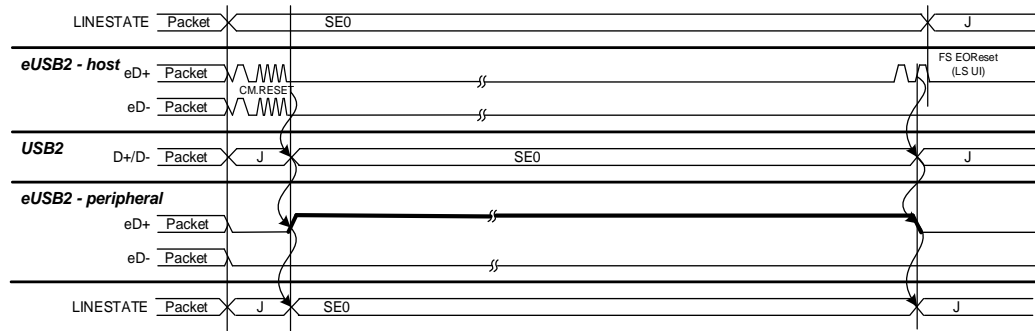


Figure 3-8: FS Reset in native mode

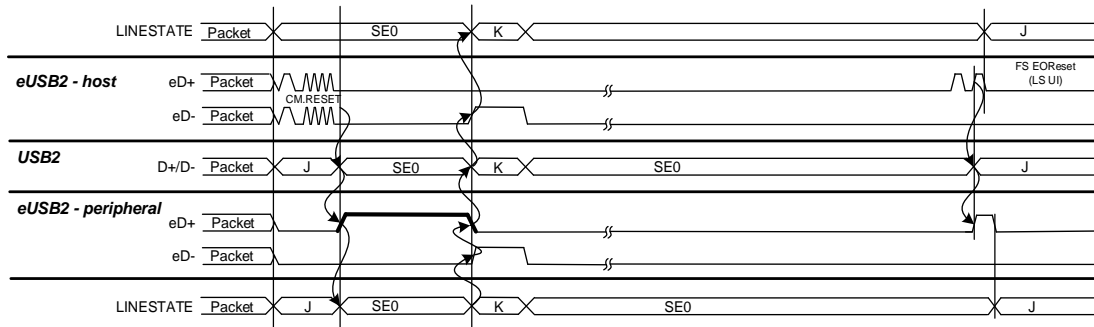
#### 3.3.4.1.2 Repeater Mode

- In host repeater mode, CM.Reset shall be transmitted by eDSPr to eUSPh. The host repeater shall initiate USB 2.0 Bus Reset on D+/D- after detecting CM.Reset.
- In peripheral repeater mode, USB 2.0 Bus Reset shall be mapped to the eUSB2 bus based on the following.
  - eDSPp shall transmit a logic '1' at eD+ and maintain logic '0' at eD- at FS operation or transmit a logic '1' at eD- and maintain logic '0' at eD+ at LS operation, to its eUSPr.
- A FS eUSB2 End of Reset (EOReset), transmitted by eDSPr, shall be 3 UIs (LS UI duration) with the first UI of logic '1', followed by the second UI of logic '0', and a third UI of logic '1' at eD+, while eD- is maintained at logic '0' through R<sub>PD</sub>. Note that FS EOReset is defined with LS UI duration to allow repeater to use a lower clock frequency to detect end of reset. Similarly, a LS EOReset shall be 3 UIs (LS UI duration) with the first UI of logic '1', followed by a second UI of logic '0', and the third UI of logic '1' at eD-, while eD+ is maintained at logic '0' through R<sub>PD</sub>. This is described in Section 3.3.1. Refer to Figure 3-9: (a) for an example.
  - eDSPr/eUSPr shall not map LineState from SE0 to J until it completes EOReset. This is to ensure the host controller not assert TxValid for a packet transmission until the completion of USB 2.0 Bus reset.
- A FS and LS eUSB2 End of Reset (EOReset), transmitted by eDSPp shall be a return to eSE0 from a logic '1' at eD+ or eD- respectively.
- If a HS capable device is connected to a FS only capable host, a device chirp may be observed from eUSPr. The peripheral repeater shall drive the device chirp K at UUSP using its HS transmitter, and subsequently map SE0 at UUSP to eSE0 at eDSPp. Upon host ending USB 2.0 Bus Reset, the peripheral repeater shall observe USSP bus state change from SE0 to J indicating the link settled into FS. The peripheral repeater shall issue EOReset at eDSPp with T<sub>STROBE</sub> on eD+.
- In a rare case where a FS host controller may initiate the first SOF immediately after the conclusion of USB 2.0 Bus Reset, there exists a possibility that a peripheral repeater may observe the beginning of the SOF at UUSP while sending EOReset at eDSPp. Under this scenario, the peripheral repeater shall complete EOReset even

during an incoming SOF at UUSP. It may forward the incomplete SOF. It is eUSP<sub>r</sub> and device controller's responsibility to ignore the corrupted SOF.



(a) FS Reset



(b) FS Reset with HS device chirp

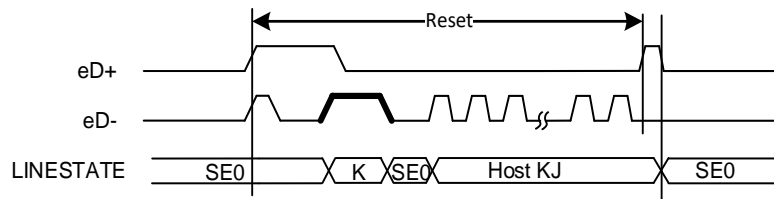
Figure 3-9: FS Reset in repeater mode

### 3.3.4.2 HS Reset

The Reset signaling between the native mode and repeater mode operation are different.

#### 3.3.4.2.1 Native Mode

- In HS L0 idle, USB 2.0 Bus Reset shall begin with eDSP<sub>n</sub> transmitting eSE1 for  $T_{CM\_eSE1\_8X}$  and continuously follow by a logic '1' on eD+. Note: USB 2.0 Bus Reset from HS Lx shall follow FS/LS mode signaling. The need for eSE1 in HS L0 is to allow eUSP<sub>n</sub>, upon detecting eSE1, to disable its squelch detector and switch to USB2 Bus Reset or XeSE1 detection.
- eUSP<sub>n</sub>, upon detecting USB 2.0 Bus Reset, shall map SE0 on its UTMI+ interface to the device controller.
- eUSP<sub>n</sub> shall transmit device chirp K as directed by its controller.
- eDSP<sub>n</sub> shall drop eD+ upon detecting a device chirp K from eUSP<sub>n</sub>.
- Upon the completion of device chirp K from eUSP<sub>n</sub>, eDSP<sub>n</sub> shall transmit host chirp K-J as directed by its host controller. Note: As opposed to repeater mode, eUSP<sub>n</sub> does not transmit a Device Termination enabled to eDSP<sub>n</sub> when its controller enters HS operation.
- eDSP<sub>n</sub> shall end UUSB 2.0 Bus Reset with a  $T_{STROBE}$  on eD+.
- Refer to Figure 3-10 for HS Reset signaling.



**Figure 3-10: HS Reset in native mode**

#### 3.3.4.2.2 Repeater Mode

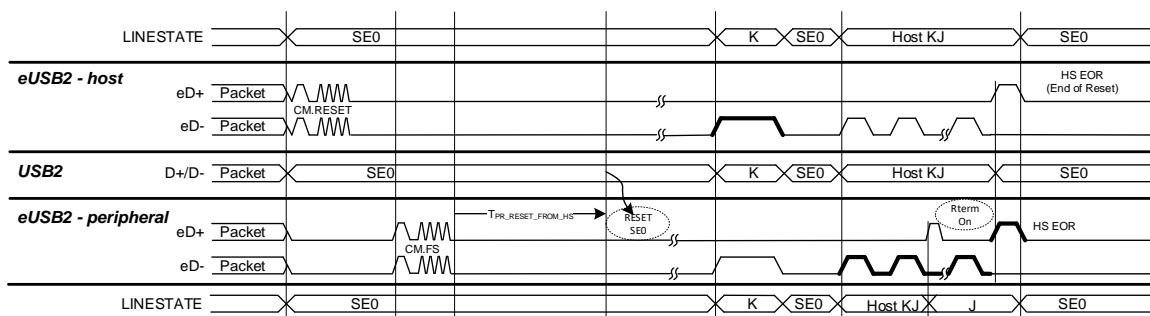
In host repeater mode, a CM.Reset shall be transmitted by eDSPr to eUSPh.

- The host repeater shall initiate USB 2.0 Bus Reset on D+/D- upon detecting CM.Reset.
- Upon detecting EOReset, the host repeater shall switch its transceiver from FS to HS and enter HS L0 with its receiver in squelched condition. Note that the repeater shall only enable its HS receiver terminations after the falling edge EOReset upon observing eSE0. This is to avoid single-ended EOReset signal at eD+ leaking through eD- that may lead to un-desired signal corruption.

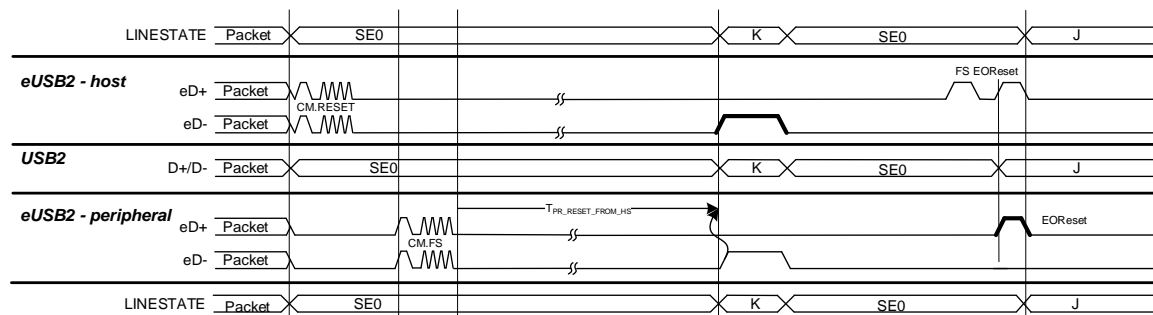
In peripheral repeater mode, the detection of USB 2.0 Bus Reset in HS operation may depend on the link state. If the link is in HS L0 idle, the peripheral repeater needs to distinguish between link entering Lx (L1 or Suspend) and USB 2.0 Bus Reset. In all other link states such as L1 or L2, the detection of USB 2.0 Bus Reset is the same as FS. Refer to Section 3.3.4.1.2 for FS USB 2.0 Bus Reset detection. The remain section describes the details of USB 2.0 Bus Reset detection in HS L0 idle and behavioral requirements of the peripheral repeater and eUSPr.

- Upon observing link idle for 3 ms, eUSPr shall be directed to issue CM.FS and configure its operation from HS to FS.
- Upon receiving CM.FS, the peripheral repeater shall disable its HS termination, enable its D+ pull-up at UUSP, and start a  $T_{PR\_RESET\_FROM\_HS}$  timer. This timer is employed to monitor the UUSP bus state to determine if the host has entered L1 or Suspend or it is issuing USB 2.0 Bus Reset. Note that there is no difference on the UUSP bus state change from L0 idle to L1 or to Suspend. The  $T_{PR\_RESET\_FROM\_HS}$  timer shall be disabled and reset in any of the following conditions.
  - It has observed the bus state change at UUSP from SE0 to J, indicating the host intention to enter L1 or Suspend. The peripheral repeater shall switch to FS configuration and enter L1. Note that eUSPr may issue CM.L2 to direct the peripheral repeater to enter Suspend based on CM.L2. Refer to Section 3.3.5.2.2 for details.
  - It has detected a device chirp K at eDSPp, indicating the host is issuing USB 2.0 Bus Reset and device is starting HS negotiation.
  - Upon expiration and no bus state changes are observed at UUSP and eDSPp maintaining eSE0 to indicate that the host is issuing USB 2.0 Bus Reset.
- eUSPr shall perform the HS negotiation if directed. The peripheral repeater shall participate the HS negotiation.
  - When directed, eUSPr shall start HS negotiation by transmitting device chirp K using FS mapping defined in Table 3-1.
  - Upon detecting device chirp at eDSPp, the peripheral repeater shall use its HS transmitter at UUSP to propagate the device chirp.
- Upon completing the device chirp, the peripheral repeater and eUSPr shall prepare for host responding to HS negotiation.

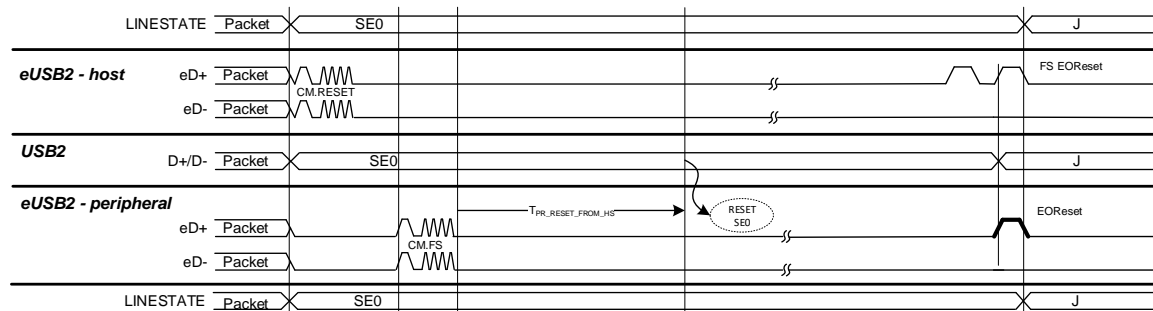
- If host KJ chirps is detected at UUSP, the following HS negotiation process shall occur. Refer to Figure 3-11(a) for details. Also refer to Figure 5-24 for further details regarding eUSPr interactions with UTMI+ interface.
  - The peripheral repeater shall map HS KJ chirps at UUSP to the FS KJ chirps at eDSPp. eUSPr shall map the KJ chirps at LineState.
  - Upon direction at UTMI+ interface, eUSPr shall transmit  $T_{STROBE}$  at eD+ to instruct the peripheral repeater to turn on its HS receiver termination and squelch detector at UUSP.
  - Upon enabling the receiver termination at UUSP, the peripheral repeater shall continue forwarding the KJ chirps at eDSPp and prepare for end of HS negotiation, and end of the USB 2.0 Bus Reset.
  - Upon detecting the squelched condition at UUSP, the peripheral repeater shall transmit EOReset with  $T_{STROBE}$  at eD+ to indicate end of the HS negotiation and USB 2.0 Bus Reset.
  - Upon detecting EOReset, eUSPr shall prepare to enter HS operation. It shall switch its transceiver to HS mode at the end of EOReset when eSE0 is observed. It shall then enter HS L0 with its receiver in squelched condition. Upon detecting EOReset, the host repeater shall switch its transceiver from FS to HS and enter HS L0 with its receiver in squelched condition. Note that eUSPr shall only enable its HS receiver terminations after the falling edge EOReset upon observing eSE0. This is to avoid single-ended EOReset signal at eD+ leaking through eD- that may lead to un-desired signal corruption.
  - Upon completing EOReset at eDSPp, the peripheral repeater shall switch its transceiver from FS to HS and enter HS L0 with its receiver in squelched condition. Note that the repeater shall only enable its HS receiver terminations after the falling edge EOReset upon observing eSE0. This is to avoid single-ended EOReset signal at eD+ leaking through eD- that may lead to un-desired signal corruption.
- If host KJ chirps are not detected at UUSP, the peripheral repeater shall observe the USB 2.0 bus state transition directly from SE0 to J to indicate a FS USB 2.0 Bus Reset.
  - Upon detecting J at UUSP, the peripheral repeater shall transmit FS EOReset as defined in Section 3.3.4.1.2. It shall switch to FS operation upon completing EOReset.
  - After completing device chirp, if a FS EOReset is detected at eD+, eUSPr shall update LineState at UTMI+, conclude USB 2.0 Bus Reset, and switch to FS operation. Refer to Figure 3-11(b) for details.
- In case a HS capable device entering USB 2.0 Bus Reset and deciding to operate at FS, it shall follow the FS USB 2.0 Bus Reset defined in Section 3.3.4.1.2. Refer to Figure 3-11(c) for details. Also refer to Figure 5-25 for further details regarding eUSPr interactions with UTMI+ interface.



(a) HS Reset ( $T_{PR\_RESET\_FROM\_HS}$  expired)



(b). HS Reset to FS link with device chirp ( $T_{PR\_RESET\_FROM\_HS}$  disabled)



(c). HS Reset to FS link ( $T_{PR\_RESET\_FROM\_HS}$  expired)

Figure 3-11: HS Reset in repeater mode

### 3.3.5 L1 and L2 Suspend

From eDSPn and eUSPn's perspective, Entry to L1 or L2 are both directed by their respective controllers. Entry to L1 is based on LPM-L1 token exchange. Entry to Suspend (L2), from the device perspective, is based on no bus activity for more than 3 ms, as defined in the USB 2.0 specification. The bus idle time is monitored by the device controller.

#### 3.3.5.1 FS/LS L1 and L2 Suspend

##### 3.3.5.1.1 Native Mode

- eDSPn and eUSPn shall enter L1 or L2 Suspend upon direction. Note that eDSPn or eUSPn may not be directed to enter L1 or L2. Under this situation, eDSPn or eUSPn may remain in L0 Idle. This should not affect eDSPn and eUSPn performing the Remote Wake and Resume operations to return the link to L0.

##### 3.3.5.1.2 Repeater Mode

- When directed, eDSPr or eUSPr shall issue CM.L1 or CM.L2 to eUSPh and perform the following.
  - It shall enter L1 or L2 Suspend if CM.L1 or CM.L2 transmission is successful. Refer to Section 3.3.8 for rules of CM transmission.
  - In a highly unlikely scenario where CM.L1 or CM.L2 transmission including retry fails, eDSPr shall issue Port Reset and inform the controller at UTMI+ interface by asserting HostDisconnect and updating LineState to SE0. Note that a CM issued by eUSPr to the peripheral repeater will not require retry since a peripheral repeater is capable of error correction. Refer to Section 3.3.8.1 for CM error recovery.
- A repeater shall transition to L1 or L2 Suspend if CM.L1 or CM.L2 is received. If the CM is corrupted, the following actions shall be performed.

- A host repeater shall follow the CM error recovery rules defined in Section 3.3.8.1. If CM retry is successful, it shall transition to L1 or L2 accordingly. If CM retry fails, it shall remain in L0.Idle.
- A peripheral repeater shall treat the corrupt CM as CM.L1 and transition to L1. Refer to Section 3.3.8.1 for CM error recovery.

Note that eDSPr or eUSPr may not be directed by its controller to enter L1 or L2 (e.g. SuspendM not asserted at UTMI+), eDSPr and the host repeater, or eUSPr and the peripheral repeater shall remain in L0.Idle.

- eUSBr shall not re-transmit CM.Lx in Lx. Note that there may exist situations in Lx, where the controller may only de-assert SleepM or SuspendM, in order to acquire the UTMI+ clock and perform some non-USB 2.0 related operations. The link remains in Lx and SleepM or SuspendM is re-asserted after the operation. This situation may also occur if the host controller is unable to respond timely to Remote Wake and therefore not able to initiate Resume before Remote Wake ends. It is eUSBr and its controller's responsibility that no CM.Lx be issued under this situation. Also note that this requirement shall also apply to HS operation.

### **3.3.5.2 HS L1 and L2 Suspend**

#### **3.3.5.2.1 Native Mode**

- eDSPn and eUSPn shall enter L1 or L2 Suspend upon direction.

#### **3.3.5.2.2 Repeater Mode**

The entry process to L1 or L2 Suspend are the same and shall include two stages of operations for both eDSPr and eUSPr.

- For eDSPr and the host repeater, the following operations shall be performed.
  - When directed, eDSPr shall issue CM.FS to the host repeater as defined in Section 3.3.8, and start a 4 ms HostDisconnect timer. This timer is defined to distinguish that the USB 2.0 bust state transition from SE0 to J is either entry to Suspend, or a device connect event.
  - Upon receiving CM.FS, the host repeater shall configure its eUSPh and UDSP from HS to FS.
  - Upon switching UDSP to FS, the host repeater shall monitor the USB 2.0 bus state. If the BUS 2.0 bus state transition to J from SE0, the host repeater shall send T<sub>STROBE</sub> at eD+, and switch to FS bus state mapping from USB 2.0 bus to eUSB2 bus as defined in Table 3-1.
  - Upon detecting T<sub>STROBE</sub> from eUSPh before the HostDisconnect timer expiration, eDSPr shall report J state on its UTMI+ LineState and stop its HostDisconnect timer. When UTMI+ SleepM or SuspendM is asserted, eDSPr shall issue CM.Lx to enter Lx. The host repeater shall enter Lx upon receiving CM.Lx. If T<sub>STROBE</sub> is not detected upon the HostDisconnect timer expiration, eDSPr shall declare device disconnect. It shall issue Port Reset to the repeater and assert HostDisconnect at UTMI+.
- For eUSPr and the peripheral repeater, the following operations shall be performed.
  - When directed, eUSPr shall issue CM.FS to the peripheral repeater as defined in Section 3.3.8.
  - Upon receiving CM.FS, the peripheral repeater shall configure its eDSPp from HS to FS. It shall configure its UUSP by enabling its HS transceiver with its termination disabled and also enabling the pull-up at D+.
  - Upon completing the port configuration after CM.FS, the peripheral repeater shall enable the T<sub>PR\_RESET\_FROM\_HS</sub> timer and monitor the USB 2.0 bus state. Refer to Section 3.3.4.2.2 for the definition and operation of the the T<sub>PR\_RESET\_FROM\_HS</sub> timer. If the BUS 2.0 bus state transition to J from SE0 before the T<sub>PR\_RESET\_FROM\_HS</sub> timer expiration, the peripheral repeater shall reset the timer, send T<sub>STROBE</sub> pulse at eD+, configure its UUSP to FS, and enter Lx state. It shall



also switch to FS bus state mapping from USB 2.0 bus to eUSB2 bus as defined in Table 3-1.

- Upon detecting  $T_{\text{STROBE}}$  from eDSPp, eUSPr report J state on its UTMI+ LineState. When UTMI+ SleepM or SuspendM is asserted, eUSPr shall issue CM.Lx to enter Lx. The peripheral repeater shall enter Lx upon receiving CM.Lx.

Shown in Figure 3-12 is an illustration of a HS link entering L2 Suspend. Note that there may exist an alternative host controller implementation that XcvrSelect and SleepM or SuspendM at UTMI+ may assert simultaneously. Under that situation, eDSPr shall issue CM.Lx only after it has detected  $T_{\text{STROBE}}$  pulse at eD+ from the host repeater.

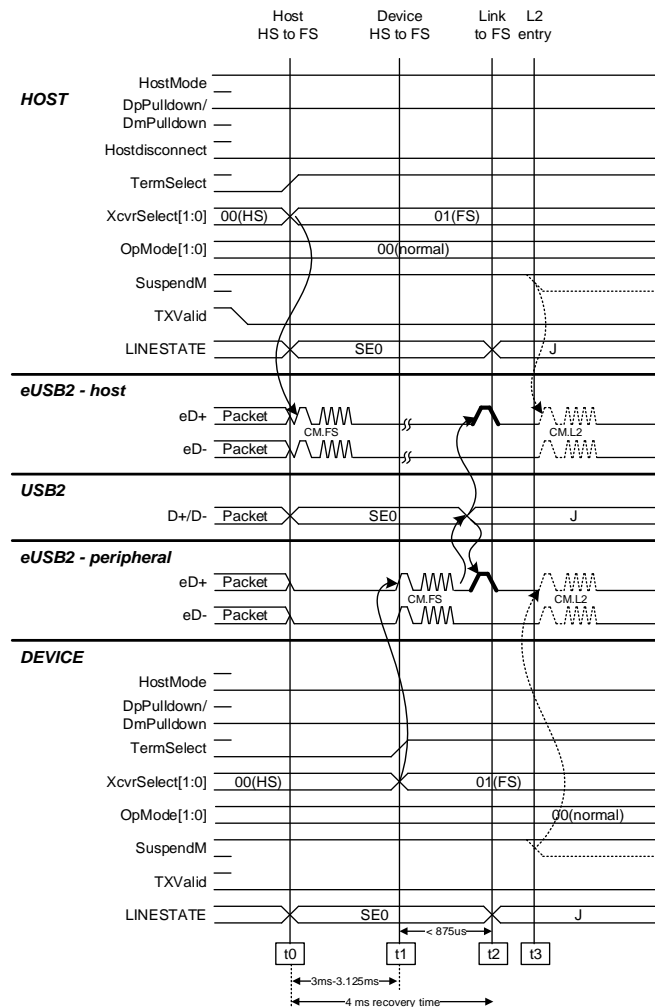


Figure 3-12: HS Link L2 entry

### 3.3.6 Resume

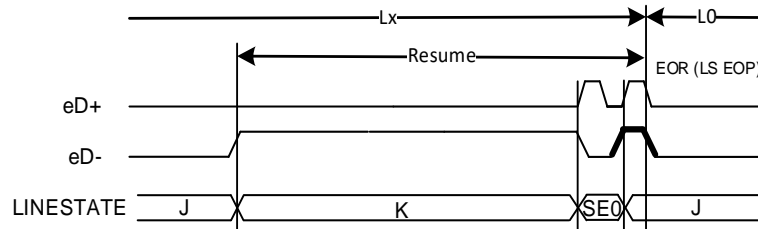
Resume in LS/FS and HS operations are both based on single-ended signaling.

#### 3.3.6.1 FS/LS Resume

The Resume signaling between the native mode and repeater mode operation are different.

### 3.3.6.1.1 Native Mode

- eDSPn shall adhere to the following rules to perform the Resume operation. Figure 3-13 shows the FS Resume signaling.
  - If it is in FS operation, it shall start Resume by driving Data K on eD- and conclude Resume with a FS EOResume on eD+ as shown in Figure 3-13. Note that a FS EOResume is the same as a FS EOP but with LS EOP timing. Refer to Section 4.3.4 for details.
  - If it is in LS operation, it shall start Resume by driving Data K on eD+ and conclude Resume with a LS EOResume on eD-. Note that a LS EOResume is the same as a LS EOP. Refer to Section 4.3.4 for details.
- eUSPn shall adhere to the following rules to perform Digital Ping at the end of Resume.
  - In both FS and LS operation, it shall start transmitting the digital ping upon detecting the first falling edge of EOP and complete transmitting the digital ping after the last rising edge and before the last falling edge of EOP. Refer to Section 4.2.3.2.1 for detail timing.



**Figure 3-13: FS Resume in native mode**

### 3.3.6.1.2 Repeater Mode

- If it's FS/LS host repeater, eDSPr/eUSPh shall adhere to the following rules to perform the Resume operation. Refer to Figure 3-14 for details of Resume.
  - eDSPr shall start Resume with SOResume followed immediately with Resume K. It shall conclude Resume with a EOResume. Note that SOResume is defined as eSE1 for  $T_{DR\_K\_eSE1\_1X}$  OR  $T_{DR\_K\_eSE1\_8X}$  duration, where  $T_{DR\_K\_eSE1\_8X}$  is selected if CM.L2 had been sent. Refer to Section 5.3.5.2 and Table 7-16 for details.
  - eUSPh, upon detecting SOResume, it shall start driving Resume K at D+/D- and conclude Resume if an EOResume is detected.
- If it's FS/LS Peripheral repeater, eDSPp/eUSPr shall adhere to the following rules to perform the Resume operation. Refer to Figure 3-14 for details of FS Resume.
  - eDSPp shall map Resume K at D+/D- to Resume K at eD+/eD-. It shall conclude Resume with EOResume matching the SE0 timing at D+/D-.
  - eUSPr shall update LineState upon detecting Resume K at eD+/eD-. It shall conclude Resume upon detecting EOResume. Refer to Section 5.3.5.2 for details.

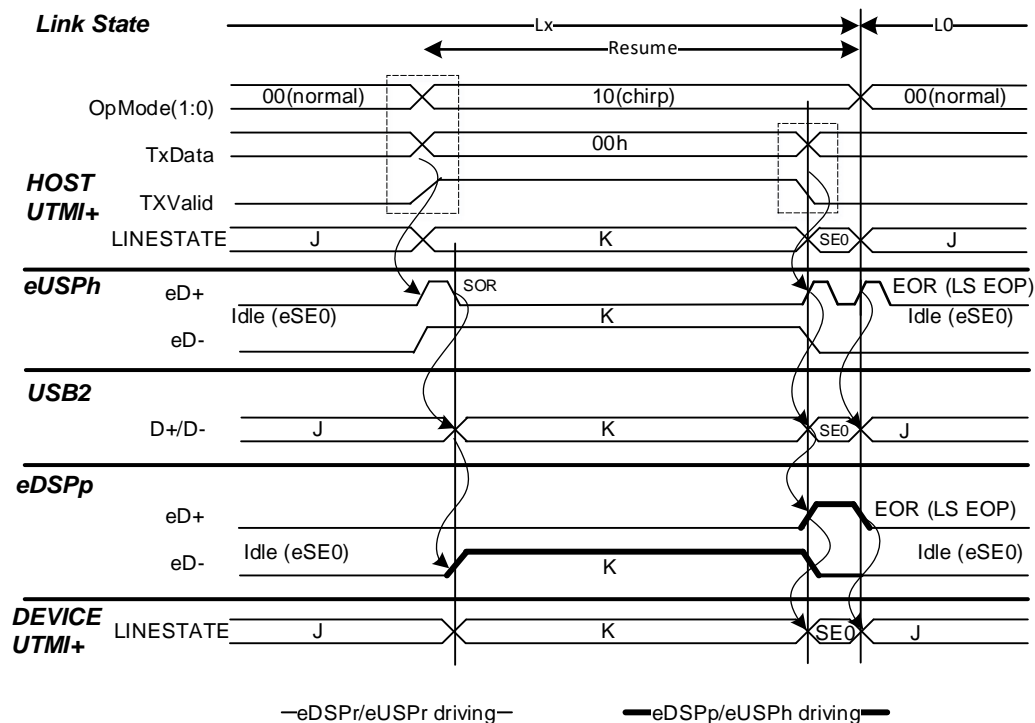


Figure 3-14: FS Resume in repeater mode operation

### 3.3.6.2 HS Resume

#### 3.3.6.2.1 Native Mode

HS Resume follow the same rule of FS Resume, except EOResume.

Shown in Figure 3-15 is the native mode Resume sequence. Compare with FS EOResume, a HS EOResume is used instead and is defined as  $T_{\text{STROBE}}$ .

- eDSPn/eUSPn shall use FS bus state mapping during Resume, and switch to HS bus state mapping upon entry to L0.
- eDSPn/eUSPn shall enable its HS transceiver upon entry to L0.

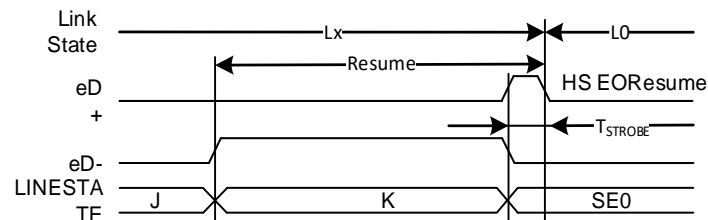


Figure 3-15: HS Resume in native mode

#### 3.3.6.2.2 Repeater Mode

Shown in Figure 3-16 is the repeater mode Resume sequence.

- Upon transmitting or detecting SOResume, eDSPr/eUSPh shall use FS bus state mapping to start Resume, and switch to HS bus state mapping upon entry to L0. The host repeater shall only enable its HS receiver terminations after the falling edge EOResume upon observing eSE0. This is to avoid single-ended EOResume signal at eD+ leaking through eD- that may lead to un-desired signal corruption.

- Upon detecting Resume at D+/D-, eDSPp shall drive Resume K to eUSPr, and conclude Resume with HS EOResume of  $T_{\text{STROBE}}$ .
- Upon detecting Resume K, eUSPr shall proceed to exit from Lx. It shall conclude Resume and transition to L0 upon the end of HS EOResume. It shall only enable its HS receiver terminations after the falling edge EOResume upon observing eSE0. This is to avoid single-ended EOResume signal at eD+ leaking through eD- that may lead to undesired signal corruption.

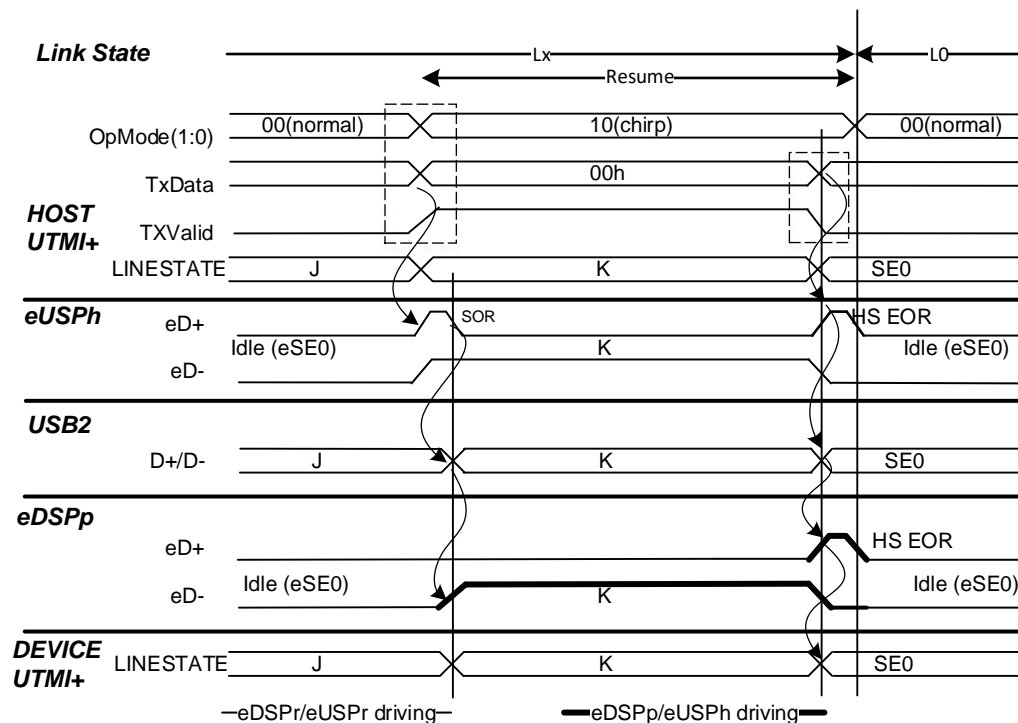


Figure 3-16: HS Resume in Repeater mode

### 3.3.7 Remote Wake

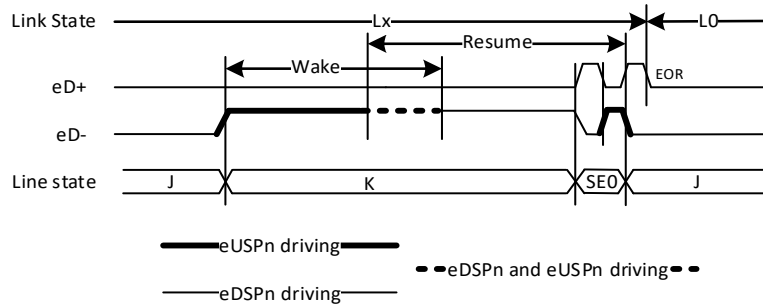
The Remote Wake signalings between the native mode and repeater mode operation are also different.

#### 3.3.7.1 FS/LS Remote Wake

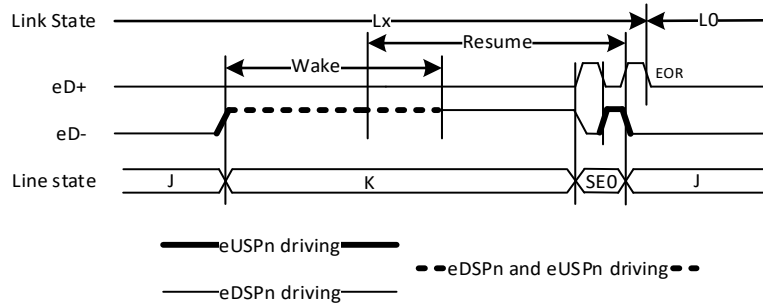
##### 3.3.7.1.1 Native mode

- If it is in FS/LS operation, eUSPn/eDSPn shall adhere to the following rules to perform the Remote Wake operation.
  - eUSPn shall drive Remote Wake K and conclude Remote Wake by disabling its SE Tx at eD-(FS) or eD+(LS). Note that under normal operation, eDSPn has already started Resume by driving Resume K. Disabling SE Tx by eUSPn, instead of driving logic '0' to conclude Remote Wake ensures the continuation of Resume K. Note also that if eDSPn does not initiate Resume before the end of Remote Wake, eUSPn may continue to observe Data K until residue charge is dissipated. A FS example is shown in Figure 3-18. This behavior should be like existing USB 2.0 if Remote Wake completes without Resume. Under this condition, eUSPn shall return to L2 and wait for eDSPn to initiate Resume, or initiate Remote Wake after an implementation specific idle time in L2.

- eDSPn, upon detecting Remote Wake, shall update LinkState, and start driving Resume K when directed. It may optionally perform auto-resume by driving Resume K before being directed. It shall conclude Resume with EOP. Shown in Figure 3-17 is the FS Remote Wake. If it is unable to drive the Resume signal within the 1 ms (TURSM) hub resume timing requirement defined by the USB 2.0 specification, it may remain in L2, prepare for the system exit from low power state and initiate Resume.

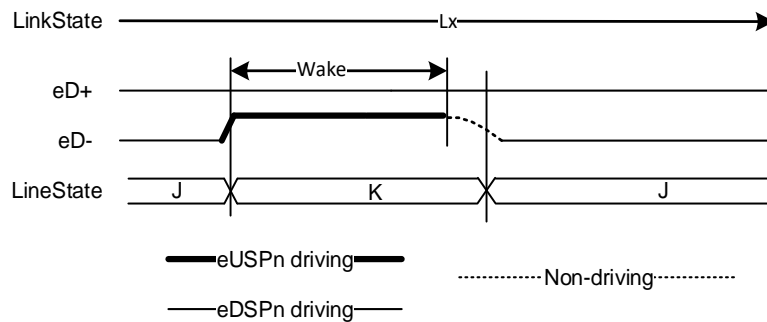


**a. Normal behavior without auto-resume**



**b. Remote Wake with optional auto-resume**

**Figure 3-17: FS Remote Wake in native mode**



**Figure 3-18: FS Remote Wake in native mode (host not responding)**

### 3.3.7.1.2 Repeater Mode

- If it is in FS/LS peripheral repeater mode, eUSPr/eDSPp shall adhere to the following rules to perform the Remote Wake operation. Refer to Figure 3-19 for details of Remote Wake.
  - eUSPr shall start Remote Wake with SOWake followed continuously with Remote Wake K. It shall conclude Remote Wake with a FS EOWake. Note that

SOWake is defined as an eSE1 for  $T_{DR\_K\_eSE1\_1X}$  or  $T_{DR\_K\_eSE1\_8X}$  duration, where  $T_{DR\_K\_eSE1\_8X}$  is selected if CM.L2 had been sent and  $T_{DR\_K\_eSE1\_1X}$  otherwise. A FS EOWake is defined as a strobe of duration  $T_{STROBE}$  at eD+ with SE Tx at eD- disabled. A LS EOWake is defined as a strobe of duration  $T_{STROBE}$  at eD- with SE Tx at eD+ disabled. During the EOWake period, it shall continue the LineState mapping from eD+/eD-. Refer to Sections 5.5.14, 5.5.15 and Table 7-16 for details.

- eDSPp, upon declaring SOWake (Refer to Table 7-16 for SOWake receive timing), shall start driving Remote Wake K at D+/D- and eD+/eD-. It shall conclude Remote Wake upon detecting the start of EOWake by stopping the forwarding of Remote Wake K at D+/D- and starting the bus state mapping from D+/D- to eD+/eD- based on the following.
  - It shall enable a  $T_{SE0\_FILTER}$  SE0 filter timer upon detecting the start of EOWake.
  - It shall perform the bus state mapping defined in Table 3-3 before and after the  $T_{SE0\_FILTER}$  SE0 filter timer timeout. Note that a momentary SE0, and more likely SE1 may be present during the transition from the conclusion of Remote Wake K to Idle J at D+/D-. the Peripheral repeater shall prevent mapping SE0 or SE1 from contending with EOWake.

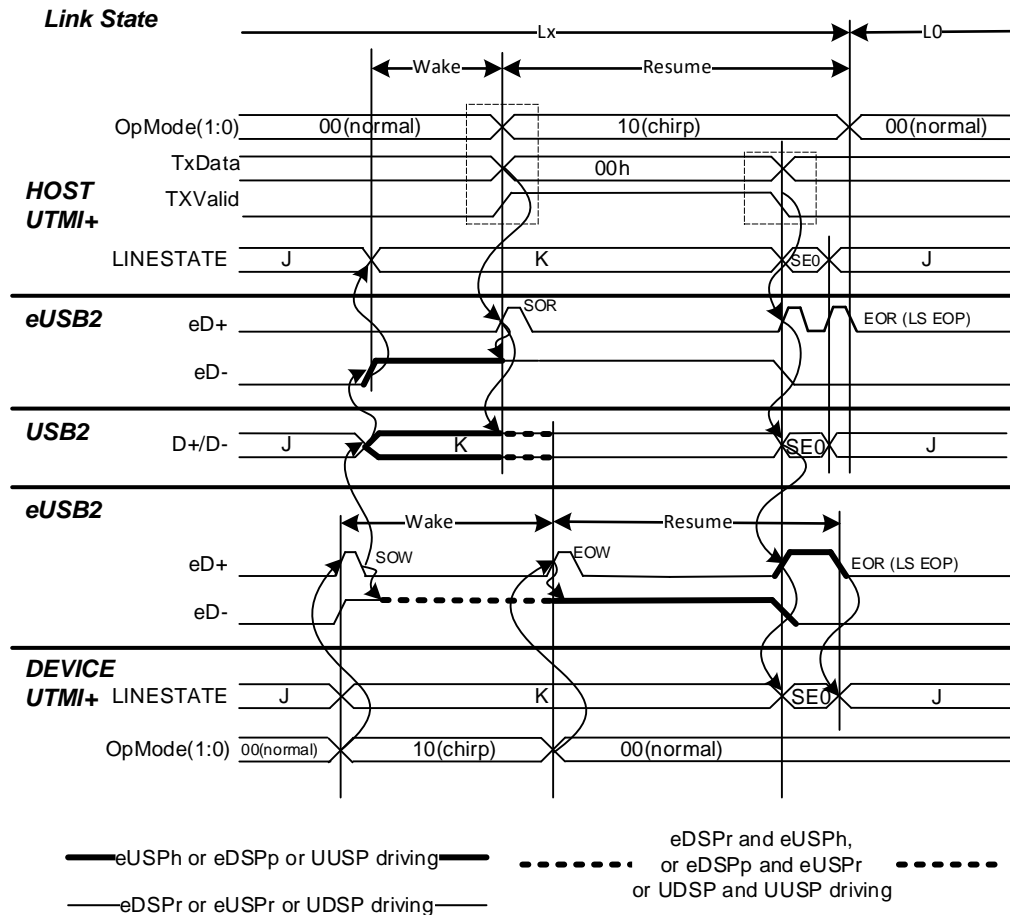
**Table 3-3: USB 2.0 to eUSB2 bus state Mapping During Remote Wake**

<b><math>T_{SE0\_FILTER}</math> SE0 filter timer</b>	<b>D+/D-<sup>1</sup></b>	<b>eD+/eD-</b>
Initial bus state upon start of the timer	K (peripheral repeater) or non-K (host repeater)	K
Before timeout	K	K
	J	Driven J
	SE0	K or J
	SE1 <sup>2</sup>	Driven J
After timeout	K	K
	J, SE1	Idle J (eSE0)
	SE0 <sup>3</sup>	FS: eD+ = '1'/eD- = '0' LS: eD+ = '0'/eD- = '1'
Note 1: USB 2.0 bus state from the SE receivers. Note 2: during the transition between K to idle J, D+ pull-up with Rpu will be faster than D- pull-down with Rpd. Note 3: this is an error situation at the peripheral repeater since USB 2.0 Bus Reset is disabled during Remote Wake. This is also a highly unlikely case when a device is disconnected at the end of Remote Wake.		

- If it is in FS/LS host repeater mode, eDSPr and the host repeater shall adhere to the following rules to perform the Remote Wake operation. Refer to Figure 3-19 for details of Remote Wake.
  - The host repeater shall reflect Remote Wake K at D+/D- to Remote Wake K at eD+/eD-. It shall conclude Remote Wake in either one of the following conditions.

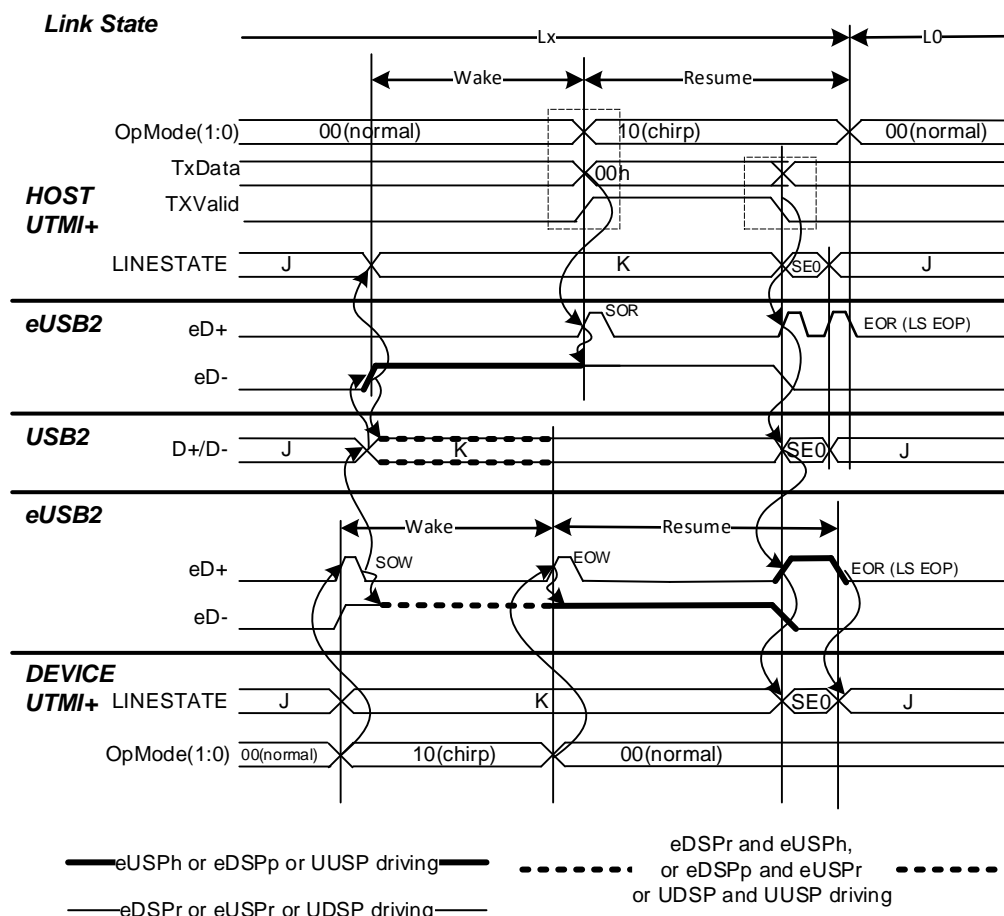
It may perform the optional auto-resume in L2 by driving Resume K at D+/D- simultaneously until SOResume is received. Note that the introduction of the host repeater auto-resume is to meet the 1 ms (TURSM) hub resume timing requirement defined by the USB 2.0 specification, while allowing sufficient time for the host controller and the system to exit from a low power state. Note also that the host repeater auto-resume may also apply to Remote Wake from L1 for ease of implementations.

- The host repeater shall conclude Remote Wake in either one of the following conditions.
  - If SOResume (eSE1 on eD+/eD-) from eDSPr is detected and the bus state at D+/D- is still maintained, it shall conclude Remote Wake by disabling its SE Tx without driving logic '0' for  $T_{eSE0\_DR\_LSFS}$  at eD-(FS) or eD+(LS). It shall start driving or in the case of auto-resume, continue driving Resume K at D+/D- until EOResume is detected. Note that not driving logic '0' at eD-(FS) or eD+(LS) for  $T_{eSE0\_DR\_LSFS}$  is to maintain continuity between Remote Wake and Resume signaling.
  - In cases where auto-resume is not supported and Remote Wake K at D+/D- concluding without SOResume, it shall drive  $T_{eSE0\_DR\_LSFS}$  at eD-(FS) or eD+(LS) to allow for immediate logic '1' to logic '0' transition before disabling its SE Tx. It shall start a  $T_{SE0\_FILTER}$  SE0 filter timer upon detecting a non-K condition at D+/D- and continue the bus state mapping from D+/D- to eD+/eD- as defined in Table 3-3. Refer to Sections 5.5.16 and 5.5.19 for timing diagram.
- eDSPr shall update LineState upon detecting Remote Wake. It shall start SOResume followed immediately with Resume K upon direction. It shall conclude Resume with EOResume.



(a). Host repeater propagates Resume upon SOResume





(b). Optional normative behavior of host repeater auto-resume

(Note: Remote Wake ends before Resume. Host repeater auto-resume maintains signaling continuity between Remote Wake and Resume at D+/D-)

**Figure 3-19: FS Remote Wake in repeater mode**

Remote Wake system implementation note:

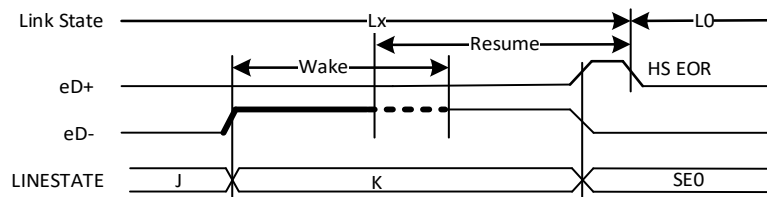
It is highly recommended that system implementation of Remote Wake be such that the host is capable of meeting the 1 ms ( $T_{URSM}$ ) Resume timing requirement defined by the USB 2.0 specification. This is to ensure ~~the~~ maximum interoperability with the USB 2.0 device ecosystem where some devices may fail after an unsuccessful event of Remote Wake. The preferred solution is for a host repeater to implement auto-resume. No auto-resume is needed if the host controller with its associated root port is capable of initiating Resume within 1 ms ( $T_{URSM}$ ) upon detecting Remote Wake. It is expected that auto-resume will be enabled by default, Whether and how to optionally disable it are implementation specific.

### 3.3.7.2 HS Remote Wake

The Remote Wake signaling at HS is the same as FS. Shown in Figure 3-20 and Figure 3-21 are a timing diagrams of Remote Wake and Resume in native mode and repeater mode.

#### 3.3.7.2.1 Native mode

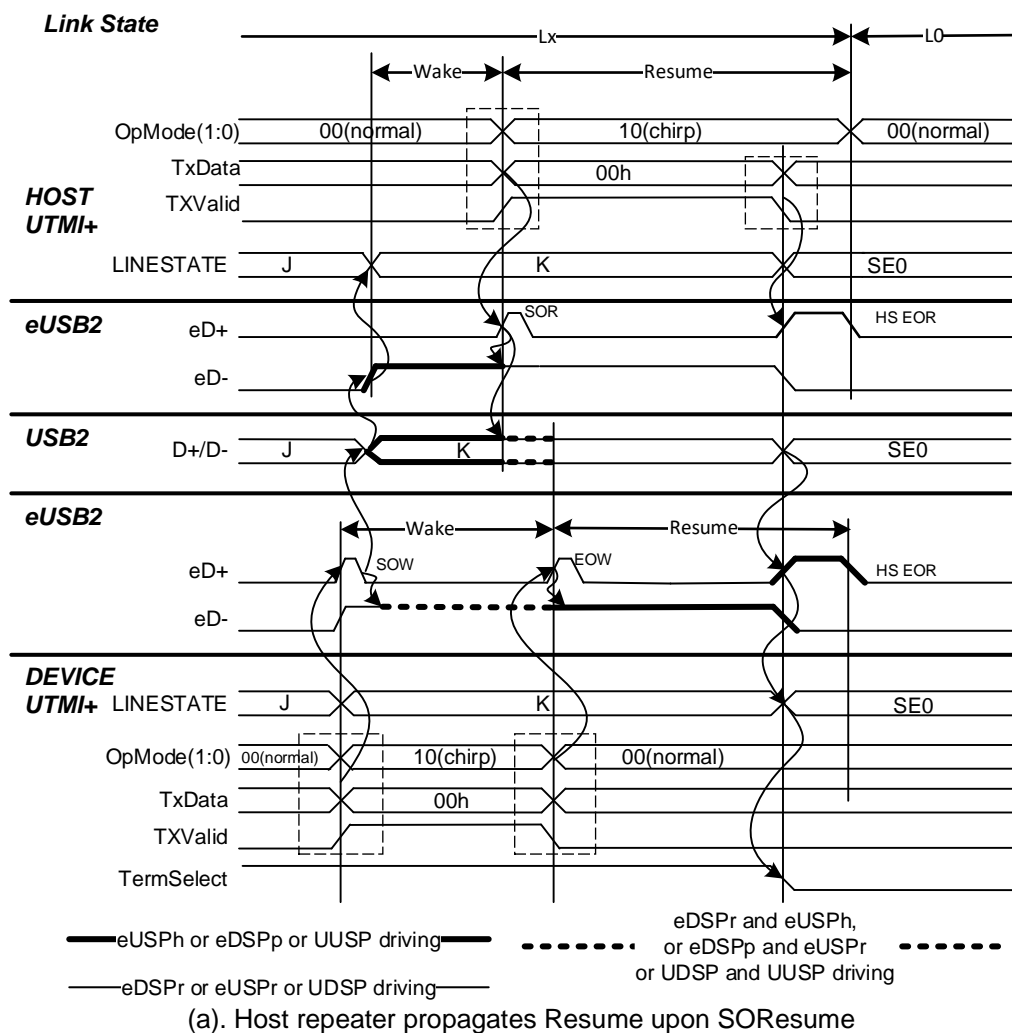
As shown in Figure 3-20, a logic '1' is presented on eD- as a wake, follow by Resume and EOResume of  $T_{STROBE}$ .

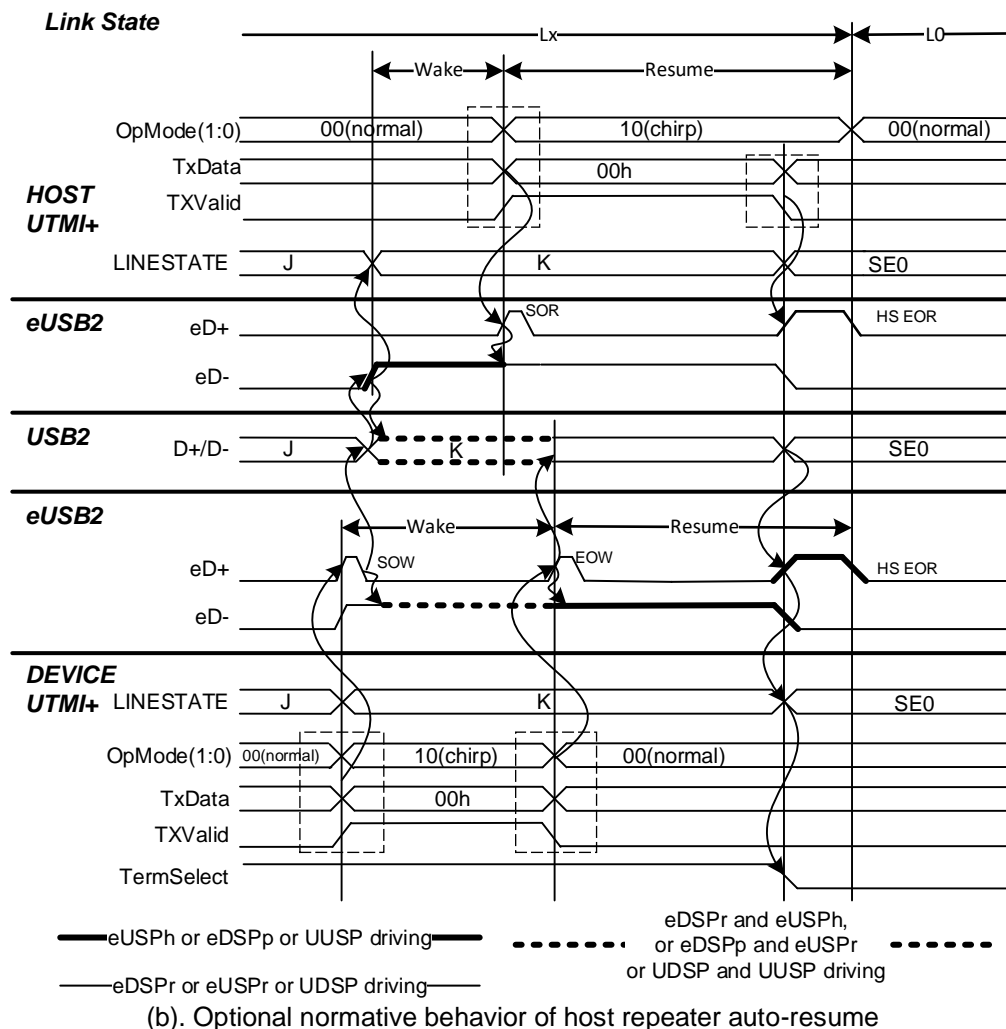


**Figure 3-20: HS Remote Wake in native mode**

### 3.3.7.2.2 Repeater mode

As shown in Figure 3-21, a wake to HS is like a FS/LS Remote Wake except for EOResume of TSTROBE.





(b). Optional normative behavior of host repeater auto-resume

Figure 3-21: HS Remote Wake in repeater mode

### 3.3.8 Control Message Signaling

Control messages (CMs) in eUSB2 are defined for various USB 2.0 and non-USB 2.0 usages in native mode and repeater mode. A CM may be issued by eDSPn, eDSPr or eUSPr. It either indicates reset, entry to L1/L2, or start of register access. Note that in native mode, only CM.RAP is used by eDSPn.

The structure of the CM is shown in Figure 3-22. It contains a 4-bit control message (CM), followed by an odd parity bit. A port transmitting a CM shall adhere to the following rules.

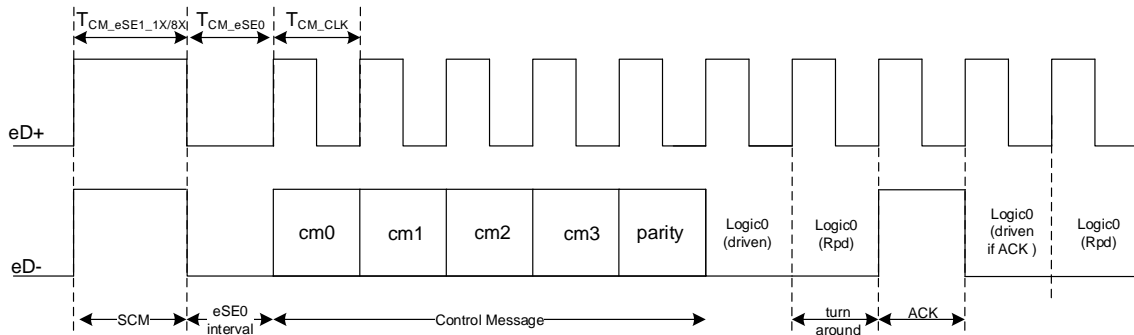
- It shall wait until the eUSB2 bus state is non-eSE1 before initiating the CM.
- It shall begin CM transmission with eSE1 as Start of Control Message (SCM).
- In the event of transmitting back-to-back CMs, the port shall allow an idle time  $T_{CMB2B}$  (end to start) between the CMs.
- The order of the control message is little endian.
- After transmitting the parity bit, it shall transmit five additional clock cycles at eD+, with each progressive clock cycle performing the following actions at eD- by the CM transmitter or the receiver.
  - CM transmitter drive logic '0'.
  - CM transmitter maintain logic '0' and enable SE Rx.

- CM transmitter check if an ACK is received. Note: The receiver to the CM message shall perform a parity check and transmit an ACK if the correct parity is detected. Note that an exception applies to the peripheral repeater, eDSPp shall always return ACK regardless of the parity check. Refer to Section 3.3.8.1 for error recovery.
- CM receiver drive logic '0' following the ACK.
- CM transmitter and receiver maintain logic '0' with  $R_{PD}$ .
- SCM of CM is defined as  $T_{CM\_eSE1\_1X}$  or  $T_{CM\_eSE1\_8X}$ ; eSE0 of CM is defined as  $T_{CM\_eSE0}$ ; Clock pulses of CM message is defined as  $T_{CM\_CLK}$ ; CM clk to data delay is defined as  $T_D$ .
- In the event of NO ACK, both TX and RX shall wait for the end of CM (not after without detecting ACK) before moving to the next operation.

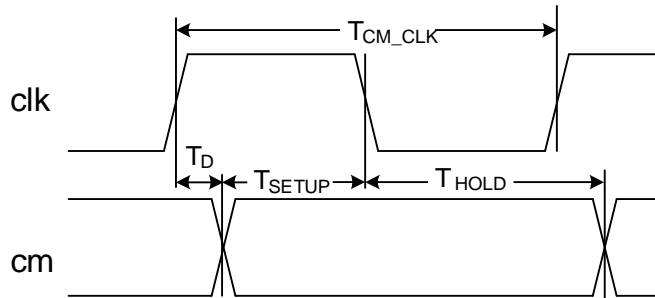
A port receiving a CM, if HS L0 idle, shall adhere to the following rule.

- It shall remove its HS termination as soon as it recognizes a proper SCM in order to enable receiving the CM clock on eD+ and CM data on eD-.

Refer to Table 7-16 for the timing specification.



(a) eUSB2 Control Message Encoding



(b) eUSB2 Control Message Timing

Figure 3-22: eUSB2 Control Message

**Table 3-4: Encoding of eUSB2 Control Message**

CM[3:0]	Parity	Description	Control Message Name	Usage Cases
0	1	HS: revert to FS terminations <sup>[2]</sup>	CM.FS	Repeater mode only <sup>[1]</sup>
		FS/LS: Enter L1 power state	CM.L1	
1	0	Enter lowest physical power state	CM.L2	Repeater mode only
2	0	USB 2.0 Bus Reset <sup>[3]</sup>	CM.Reset	Repeater mode only Note: SCM for CM.Reset is 8X longer than other CMs. Implementation may use this to distinguish CM.Reset to others.
3-6	X	Reserved	Reserved	Reserved
7	0	Enable HS terminations without enumeration (Test Mode) <sup>[4]</sup>	CM.Test	Repeater mode only For compliance use
8-14	X	Reserved	Reserved	Reserved
15	1	Start of register access <sup>[5]</sup>	CM.RAP	Native mode: For eDSPn to access the register space in eUSPn. Repeater mode: For eUSPr or eDSPr to access the register space in its associated repeater.

**Note 1.** Entry to L1 for native mode is based on a LPM extended transaction.

**Note 2.** Repeater to remove HS termination and enter L1 power state. This is also a transitional state to L2. Refer to Sections 3.3.5, 5.3.5 and 5.4.5 for details.

**Note 3.** Transmitted with  $T_{CM\_eSE1\_8X}$  timing parameters when SuspendM at UTMI+ interface is asserted (i.e. CM. L2 has been transmitted); else it is transmitted with  $T_{CM\_eSE1\_1X}$  timing.

**Note 4.** Host Mode HS Compliance Test mode entry. Refer to Section 5.3.1.1 for details.

**Note 5.** Indication of the start of register access protocol. It is only allowed before the configuration is started in native mode and repeater mode. Refer to Chapter 5 and Chapter 6 for details.

### 3.3.8.1 CM Retry and Recovery Rules

CM retry rules apply to every CM except CM.RAP. Refer to Chapter 6 for CM.RAP retry and error recovery.

- If NACK is received, eDSPr may retry CM only once  $T_{CMRETRY}$  after the end of CM. If CM retry fails, it shall issue Port Reset as described in Section 3.3.8.
  - While transmitting Port Reset, eDSPr shall inform the controller at UTMI+ interface by asserting HostDisconnect and updating LineState to SE0.
  - When the Port Reset is received, eUSPh shall enter Default.

- eDSPp shall always respond with ACK regardless of parity error or undefined CM detected. It shall adhere to the following rules for CM error recovery.
  - If in HS L0, the first CM eDSPp receives shall always be treated as CM.FS.
  - If in FS/LS L0/L1, it shall treat the received CM as CM.L1. Note that only CM.L1 or CM.L2 will be received under these link states. CM.L1 allows the repeater to stay in L1 that is compatible with L2.
  - In unconnected state (pullup has not been enabled), it shall ignore the received CM after responding with ACK. Note that the possible CM in this state is CM.L2, and the peripheral repeater should already be at their power level.
- eUSPr shall not retry CM. If ACK is not received, it shall issue Port Reset.

### 3.3.9 Extended eSE1

Extended eSE1 (XeSE1), shown in Figure 3-23, is defined with eSE1 duration of  $T_{XeSE1}$ . It is used under various circumstances for an eUSB2 port to announce an event of device disconnect or Port Reset (Note that is not equivalent to USB 2.0 Bus Reset).

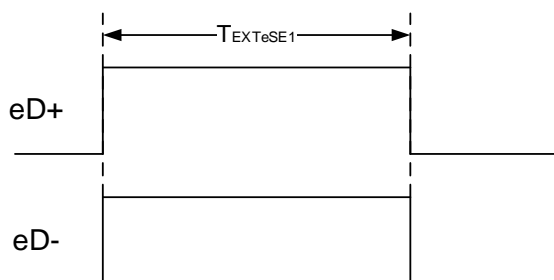


Figure 3-23: Extended eSE1 (XeSE1)

#### 3.3.9.1 XeSE1 Functional Definitions

XeSE1 is defined to cover the following scenarios.

- As Port Reset in native mode,
  - For eDSPn to indicate power-on and ready for operation.
  - For eDSPn/eUSPn to terminate a USB 2.0 session, or to recover from an error event.
  - For eUSPn to inform eDSPn device (soft) disconnect when directed by its device controller.
- As Port Reset in repeater mode,
  - For eUSBr to indicate power-on and ready for operation to its associate repeater.
  - For eDSPr/eUSPr to terminate a USB 2.0 session, or to recover from an error event.
  - For eDSPr to reset the host repeater upon qualifying a logic '1' on eD+ for disconnect (map to a disconnect SE0 condition on D+/D-) while operating in FS idle.
  - For eDSPr to reset the host repeater upon qualifying a logic '1' on eD- for disconnect (map to a disconnect SE0 condition on D+/D-) while operating in LS idle.
  - For eDSPr or eUSPr to reset the host or peripheral repeater respectively when directed (this is implementation specific between the controller and its physical layer).
  - For eUSPr to direct its peripheral repeater to perform device disconnect.
- As Device Disconnect Announcement in repeater mode, for the host repeater to inform eDSPr a device disconnect event in HS L0. Refer to Section 5.3.4.3 and 5.5.7 for details.  
 Note: A peripheral repeater shall never transmit XeSE1.

#### 3.3.9.2 XeSE1 Transmit and Detection

The timing of XeSE1 is specified such that it shall survive any bus contention without corruption except device babbling.

The transmission of XeSE1 shall adhere to the following rules.

- When directed, a port shall transmit XeSE1 regardless of the eUSB2 bus state.

- In native mode, eUSPn shall not transmit XeSE1 upon power-on to avoid potential EOS stress to eDSPn. Note: In the case that the device in native mode is powered off or silent disconnected after it is enabled (Port Configuration) by its associated eDSPn, system implementation shall ensure a sideband communication to inform eDSPn.
- In repeater mode, eUSPh and eDSPp shall not transmit XeSE1 upon power-on. This implies that both host and peripheral repeaters shall not power off once they have been enabled (Host/Peripheral enable) by its associated eDSPr or eUSPr. It is implementation specific to use sideband communication to inform eDSPr or eUSPr if powering down the repeater is required.
- In case of device babbling, existing mechanisms such as VBus cycle at the system level shall be implemented to stop device babbling. A system may also employ sideband signal to reset the host repeater.

XeSE1 detection and declaration shall be based on the following.

- A port, upon detecting eSE1, shall declare the reception of XeSE1 based on the  $T_{XeSE1}$  receive timing (with exception of  $T_{HSDISC\_eSE1}$  for HS disconnect and  $T_{NATIVE\_eSE1}/T_{NATIVE\_XeSE1}$  in Native Mode) in Table 7-16. Note that concurrent XeSE1 may exist when both link partners drive XeSE1 at the same time. Under this situation, the conclusion of XeSE1 may likely be asynchronous. If the port concludes XeSE1 earlier, it may drive eSE0 before switching to pull-down. Contention may occur between eSE0 and eSE1. It is recommended that a momentary eSE1 discontinuity up to  $T_{eSE0\_DR\_HS}$  or  $T_{eSE0\_DR\_LSFS}$  be ignored.

The following actions shall be taken at the end of XeSE1.

- Upon completing Port Reset transmission, a port shall ensure an idle time of  $T_{CONFIG\_IDLE}$  before initiating Port Configuration.
- Upon completing Port Reset or Device Disconnect Announcement, an eUSB2 port or repeater shall transition to Default.

Note that when Port Reset is transmitted by eDSPn to eUSPn, or eUSBr to repeater respectively upon POR, eUSPn and repeater may still be in the process of POR. In this case, the full duration or  $T_{XeSE1}$  receive timing of Port Reset may not be met by eUSPn and repeater. As eUSPn and the repeater are in POR default state, they may ignore or declare XeSE1 (Note: eUSPn and the repeater is recommended to have a timer to distinguish between XeSE1 and CM.RAP) even with the potential shortened Port Reset duration. eUSPn and the repeater shall wait for Port/Repeater Configuration if Port Reset is ignored. Also, if a controller reset or UTMI+ reset occur during Port Reset, eDSPn or eUSBr may choose to complete or terminate Port Reset. If Port Reset is terminated, eDSPn or eUSBr shall retransmit Port Reset.

### 3.3.10 Port/Repeater Configuration

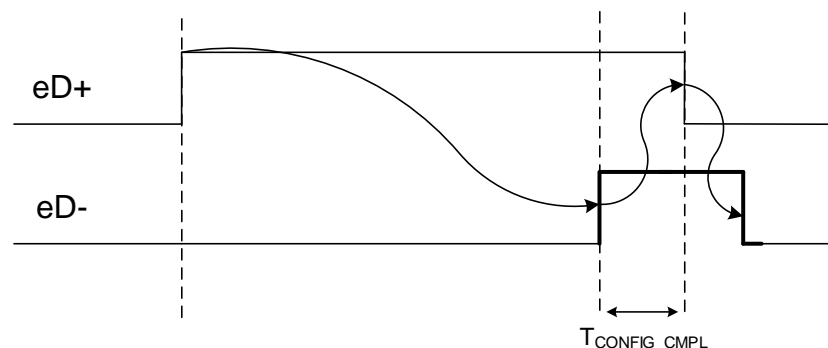
Port/Repeater Configuration is a handshake defined to establish an initialization connection between link partners (eDSPn and eUSPn, eUSBr and repeater). Refer to Figure 3-24 for signaling detail.

- Port/Repeater Configuration is issued by eDSPn/eDSPr/eUSPr and acknowledged by eUSPn/eUSPh/eDSPp respectively upon detecting the logic '1' on eD+/eD-.

Port/Repeater Configuration is defined to cover the following scenarios

- To establish an initialization between eDSPn and eUSPn as well as to convey HS receiver termination setting to eUSPn.
  - A logic '1' on eD+ from eDSPn to eUSPn to indicate to eUSPn to enable its HS receiver termination. And eUSPn shall acknowledge on eD-.

- A logic '1' on eD- from eDSPn to eUSPn to indicate to eUSPn to disable its HS receiver termination. And eUSPn shall acknowledge on eD+.
- eDSPn shall complete Port Configuration upon detecting an acknowledgment from the eUSPn by  $T_{\text{CONFIG\_CMPL}}$ .
- To establish an initialization between eUSBr and its repeater for Host or Peripheral operation mode.
  - A logic '1' on eD+ from eUSBr to its repeater to enable its repeater for Host operation mode. The repeater shall acknowledge on eD- and configure itself as a host repeater.
  - A logic '1' on eD- from eUSBr to its repeater to enable its repeater for Peripheral operation mode. The repeater shall acknowledge on eD+ and configure itself as a peripheral repeater.
- eUSBr shall complete Repeater Configuration upon detecting an acknowledgment from the repeater by  $T_{\text{CONFIG\_CMPL}}$ , and configure itself as eDSPr or eUSPr respectively.



**Figure 3-24: Port/Repeater Configuration**

### 3.3.11 Implementation Recommendations for eSE1 Detection

Based on SE operations described in the previous sections, the transmission of eSE1 indicates the start of various eUSB2 link or state transitions. A summary of eSE1 transmission is listed in the following.

- In native mode and repeater mode, for start of Port Reset, or CM.RAP.
- In native mode, for start of the USB 2.0 Bus Reset and device soft disconnect.
- In repeater mode, for start of a control message (CM.Reset, CM.FS, CM.L1, CM.L2, or CM.Test), Resume, Remote Wake, and Device Disconnect Announcement.

Various eSE1 signatures are defined and can be summarized in the following three categories.

- For SCM which follows with eSE0 and fixed-width control message. Refer to Section 3.3.8 for details.
- For error recovery through Port Reset, or device soft disconnect in native mode and Device Disconnect Announcement in repeater mode, where the duration of eSE1 is defined to survive any contention at eUSB2 bus. Refer to Section 3.3.9 for details.
- For Resume and Remote Wake in repeater mode, and USB 2.0 Bus Reset in native mode, where eSE1 does not end with eSE0, but is immediately followed with either logic '1' at eD+ or eD-.

The following eUSB2 port implementation guidelines are recommended when detecting eSE1 and subsequent processing of eSE1.

- It shall not declare eSE1 reception, if it is driving both eD+ and eD-.
- If it is driving logic '1' only at eD+ (or eD-) and observing logic '1' at eD- (or eD+) that is non-driving (maintained to logic '0' with Rpd), it shall perform one of the following.



- If during Remote Wake, when it is forwarding Remote Wake K and receiving SoReume from eDSPr, the host repeater shall declare the reception of eSE1. Refer to Figure 3-19 for details.

In all other cases, it shall not declare eSE1 reception, but monitor the non-driving eD+ or eD- if observed logic '1' is expected under normal operating conditions, or un-expected with XeSE1 as an asynchronous event described in Section 3.3.9, or highly unlikely with SCM as a concurrent event described in Section 3.3.8. It is recommended that if an un-expected logic '1' is observed at non-driving eD+ or eD-, an eUSB2 port transition to SCM or XeSE1 detection, and suspend or stop other on-going operations that may block SCM or XeSE1 detection.

## 4 eUSB2 Native Mode Architecture and Operation

### 4.1 eUSB2 Native Mode Configuration and Usage

Native mode eUSB2 operation is defined to support in-box interconnect where the speed of the eUSB2 operation maybe preconfigured. This usage model may allow an opportunity for a downstream port to support only a single or selected speed configurations, and hence, implementation optimization may be possible based on port customization. However, it is a system's responsibility to be aware of a downstream port's capability and to ensure proper device configuration and interoperability.

- A customized downstream port supporting a single or selected data rates shall follow the eUSB2 specification as defined in Section 4.3 in terms of device connect, reset and speed detection. Note that a downstream port that supports high-speed only operation is still required to perform speed detection protocol, even it is known prior that an attached device is high-speed capable.

Examples of downstream port configurations include but are not limited to the following:

- LS, FS, HS
- LS, FS only
- FS, HS only
- FS only
- HS only

### 4.2 eUSB2 Native Mode Protocol Signaling

The below section describes protocol and signaling that is applicable to Native Mode only.

#### 4.2.1 Port Reset (XeSE1)

Port Reset is used only after an eUSB2 port is configured to be either eDSPn or eUSPn. An eUSB2 port may be default to eDSPn or eUSPn upon power-on, or configured to eDSPn or eUSPn after power-on reset. Port Reset is defined to perform the following:

- eUSPn shall initiate Port Reset when it is directed to terminate its current USB session. This is also referred to as soft disconnect. It is the only instance where Port Reset is transmitted from eUSPn. Note: In the event where eUSPn may be disconnected without its associated eDSPn being aware or not being able to transmit Port Reset before disconnecting/powering off (especially in L1 or L2), it is implementation specific to use sideband communication to inform eDSPn. This is referred to as silent disconnect
- eDSPn shall initiate Port Reset under one of the following conditions.
  - Upon power-on and default to eDSPn.
  - After power-on reset and configured to be eDSPn.
  - Implementation specific HW reset to terminate the current USB session or to recover from an error situation.

A declaration of Port Reset reception is defined below:

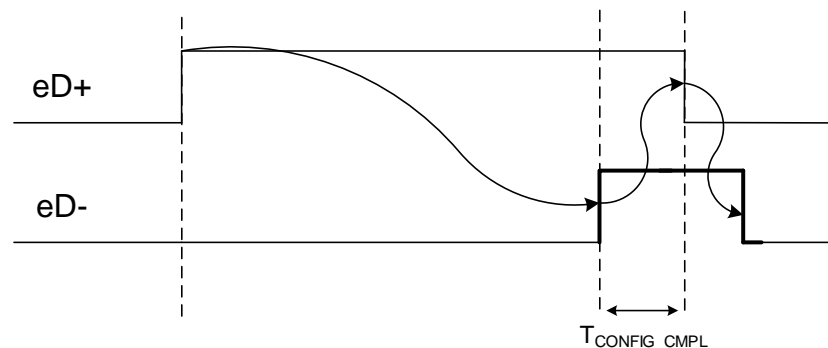
- eUSPn upon POR detecting eSE1 on the eUSB2 bus, shall declare the reception of XeSE1 based on the  $T_{XeSE1}$  receive timing, or determine if eSE1 is either a truncated XeSE1, or SCM of CM.RAP. Note: As both eDSPn and eUSPn power up asynchronously, eUSPn may not observe the complete XeSE1 to declare Port Reset. eUSPn may ignore this and continue to wait for Port Configuration. Note also that eSE1 that is shorter than  $T_{XeSE1}$  may also be SCM of CM.RAP from eDSPn before Port Configuration.
- If an eDSPn or eUSPn port is not transmitting eSE1, and upon detection of eSE1 for  $T_{NATIVE\_eSE1}$ , it shall stop and disable its transmitter to prevent any contention with eSE1 reception.

- eDSPn/eUSPn shall declare the reception of soft disconnect/Port Reset respectively upon detecting eSE1 condition for  $T_{NATIVE\_XeSE1}$ . Note that this receive timing is shorter than the receive timing  $T_{XeSE1}$  in repeater mode, it is to allow for timely Port Reset declaration with assumption that in Native Mode eUSB2 operations, it is expected that both eDSPn and eUSPn have the necessary clock frequency to detect it. SCM of CM.RAP and start of USB 2.0 Bus Reset in HS operation are the only other eSE1 conditions.

#### 4.2.2 Port Configuration

Port Configuration is a handshake defined to initialize connection as well as conveying receiver termination scheme between eDSPn and eUSPn. Port Configuration signaling is defined to perform the following. Refer to Figure 4-1 for signaling detail.

- Port Configuration is issued by eDSPn and acknowledged by eUSPn upon detecting the logic '1' on eD+ or eD-, depending on whether eUSPn should enable its HS receiver termination or not.
- Upon POR and after transmitting Port Reset, eDSPn shall drive a logic '1' on either of the following.
  - eD+ as a Port Configuration to eUSPn. This is to direct eUSPn to enable its HS receiver termination. And eUSPn shall acknowledge on eD-.
  - eD- as a Port Configuration to eUSPn. This is to direct eUSPn to disable its HS receiver termination. And eUSPn shall acknowledge on eD+.
- eDSPn shall complete Port Configuration upon detecting an acknowledgment from the eUSPn by  $T_{CONFIG\_CMPL}$ .



**Figure 4-1: Port Configuration with HS Differential Receiver Termination Enable**

#### 4.2.3 Disconnect Detect

The mechanisms of eUSB2 disconnect detect at LS/FS and HS are different from USB 2.0. Section below describes the disconnect detection in LS/FS/HS and under different link states.

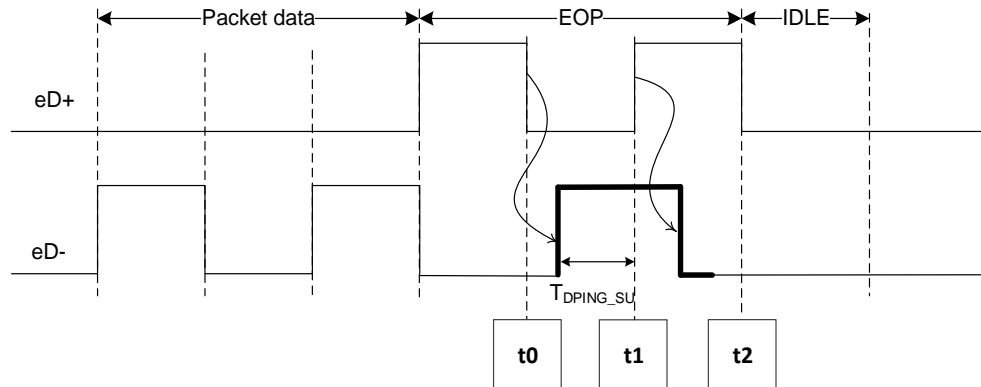
##### 4.2.3.1 Low-Speed/Full-Speed Disconnect Detect during L0

The eSE0 idle state of eUSB2 is maintained by both ports through their  $R_{PD}$  in FS/LS L0. This is different from idle state J defined in USB 2.0 that allows for disconnect detect during idle state. A digital mechanism and Port Reset are defined for eUSB2 device disconnect detect during L0.

##### 4.2.3.1.1 Digital Ping

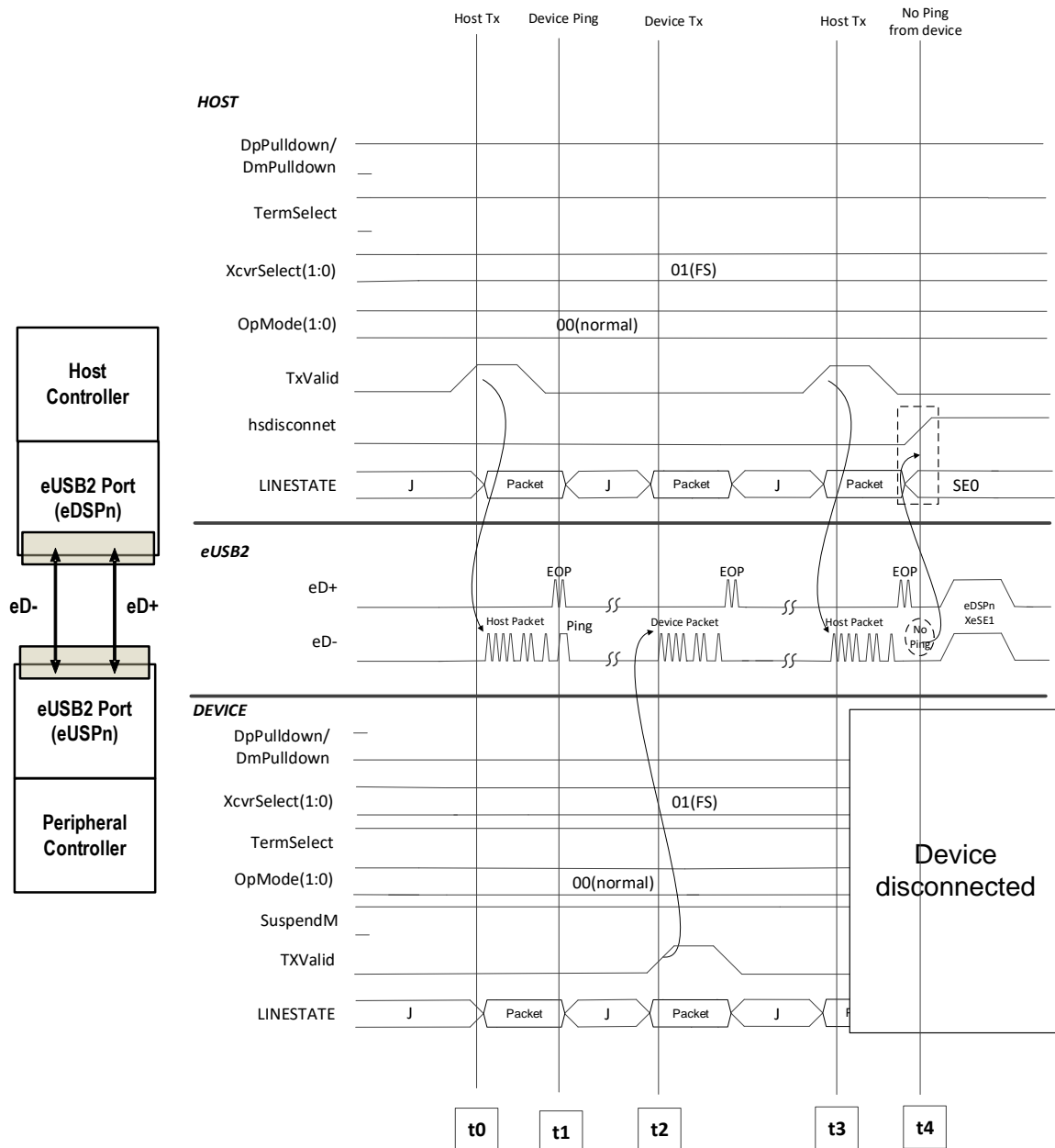
eUSPn in L0 periodically transmits a digital ping, as illustrates in Figure 4-2, to announce its presence. In L0, during silent disconnect, the absence of the digital ping from eUSPn within EOP of any packet transmitted from eDSPn is an indication of device disconnect. A digital ping is defined as a digital pulse of variable duration transmitted at eD- or eD+ during EOP reception.

- eUSPn shall transmit a digital ping within the window of EOP. It shall transmit the digital ping based on the following:
  - It shall start transmitting the digital ping upon detecting the first falling edge of EOP as shown in t0 of Figure 4-2. It shall allow  $T_{DPING\_SU}$  for eDSPn to sample the digital ping.
  - It shall complete transmitting the digital ping after the last rising edge and before the last falling edge of EOP as shown in t1 and t2 respectively of Figure 4-2. Note that the combined propagation delays from the rising edge of eDSPn EOP and from the falling edge of the eUSPn digital ping are sufficient to meet the hold time needed for eDSPn to sample the digital ping.
- eDSPn in FS operation shall sample at eD- for digital ping on the second rising edge of EOP as shown in t1 of Figure 4-2.
- eDSPn in LS operation shall sample at eD+ for digital ping on the second rising edge of EOP.
- eDSPn shall declare device disconnect upon detecting missing of the digital ping.



**Figure 4-2: FS Digital Ping on EOP**

Figure 4-3 illustrates an established FS link with a silent device disconnect.



**Figure 4-3: FS disconnect in L0**

- t0:
  - eDSPn transmits data packet.
- t1:
  - eUSPn transmits digital ping at EOP.
- t2:
  - eUSPn transmits data packet.
  - Digital ping not required from eDSPn.
- t3:
  - eDSPn transmits data packet.
  - eUSPn disconnected, hence no digital ping returns to eDSPn during EOP.
- t4:
  - eDSPn declares device disconnect reflecting UTMI+ disconnect to its host.

- eDSPn transmits Port Reset for a potential new USB session (as an attempt to recover the link from a possible error condition).

#### 4.2.3.1.2 Port Reset (XeSE1)

eUSPn and eDSPn utilize Port Reset (XeSE1) to reset the link as described below:

- eUSPn as directed by its controller to perform a soft disconnect.
- eDSPn shall declare device disconnect when Port Reset is detected.

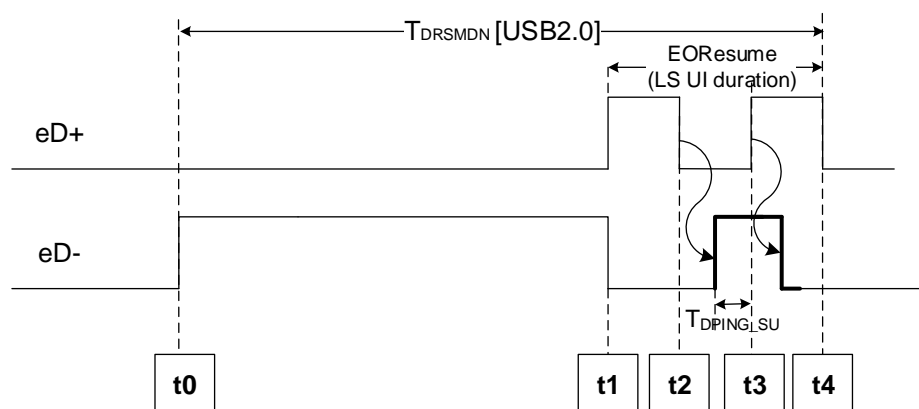
#### 4.2.3.2 Low-Speed/Full-Speed Disconnect Detect during L1, L2, End of Resume, or End of Reset

The eSE0 idle state of eUSB2 is maintained by both ports through their  $R_{PD}$  during L1 and L2. This is different from idle state J defined in USB 2.0 that allows for disconnect detect during these states. A digital mechanism and Port Reset are defined for eUSB2 device disconnect detect during L1 and L2.

##### 4.2.3.2.1 Digital Ping

eUSPn in L1 or L2 transmits a digital ping to announce its presence within EOResume/EOReset as indication of device presence. A digital ping is defined as a digital pulse of variable duration transmitted at eD- or eD+ during EOP reception. An example of the FS digital ping transmission at the end of Resume is shown in Figure 4-4.

- eUSPn shall transmit a digital ping within the window of EOResume or EOReset. It shall transmit the digital ping based on the following:
  - It shall start transmitting the digital ping upon detecting the first falling edge of EOP as shown between  $t_2$  and  $t_3$  of Figure 4-4.
  - It shall complete transmitting the digital ping after the second rising edge and before the second falling edge of EOP as shown in  $t_3$  and  $t_4$  respectively of Figure 4-4. Note that the propagation delay from eDSPn is sufficient to meet the hold time needed for eDSPn to sample the digital ping.
  - Note that eUSPn shall ensure the assertion of digital ping before  $T_{DPING\_SU}$  to ensure proper sampling by eDSPn.
- eDSPn in FS operation shall sample at eD- for digital ping on the second rising edge of EOP as shown in  $t_3$  of Figure 4-4.
- eDSPn in LS operation shall sample at eD+ for digital ping on the second rising edge of EOP.
- eDSPn shall declare device disconnect upon detecting missing of the digital ping.



**Figure 4-4: Illustration of eUSPn Transmitting Digital Ping at the FS End of Resume**

- t0. eDSPn drives eD- to logic '1' to start Resume.
- t1. eDSPn transmits FS EOResume (LS UI duration) to conclude Resume.
- t2. eUSPn, upon detecting EOResume, transmits a digital ping.

- t3. eDSPn sample digital ping to declare device present or disconnect.
- t4. Link enters L0.

#### 4.2.3.2.2 Port Reset (XeSE1)

eUSPn and eDSPn utilize Port Reset (XeSE1) to reset the link as described below:

- eUSPn as directed by its controller to perform a soft disconnect.
- eDSPn shall declare device disconnect when Port Reset is detected.

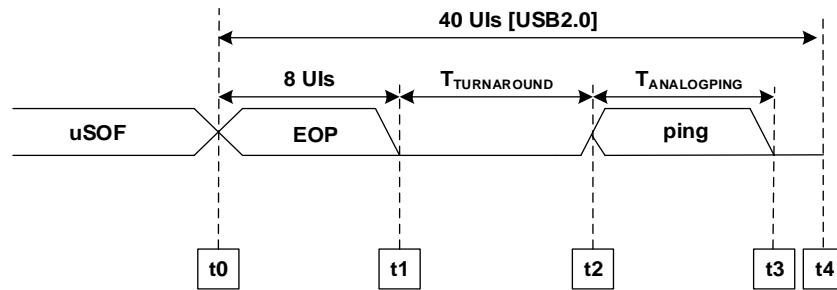
#### 4.2.3.3 High-Speed Disconnect Detect during L0

The eSE0 idle state of eUSB2 is maintained by both ports through their  $R_{PD}$  in HS L0. A mechanism of analog ping and Port Reset are defined for eUSB2 HS device disconnect detect during L0.

##### 4.2.3.3.1 Analog Ping

For eDSPn, high-speed disconnect detect is performed based on eUSPn periodically transmitting an analog ping to eDSPn to announce its presence. This is illustrated in Figure 4-5 .

- eDSPn shall transmit an  $\mu$ SOF packet upon directed by its controller with 8 UIs of EOP length (instead of 40UIs as in USB 2.0) and allow for eUSPn to transmit an analog ping within the remaining 32 UIs.
- While eDSPn transmits the 8 UI  $\mu$ SOF EOP, it shall maintain LineState to its host controller as 40UIs to prevent subsequent TX by the controller during analog ping.
- eUSPn shall transmit an analog ping after detecting the end of HS EOP as defined in Figure 4-5.
- eUSPn may require maintaining 40UI  $\mu$ SOF EOP on LineState of its UTMI+ interface to the controller depending on device controller implementation requirement.
- An analog ping shall be a high-speed data K with pulse width of  $T_{ANALOGPING}$  as shown in Figure 4-5.
- eDSPn shall enable its squelch detector no later than the minimum time of  $T_{TURNAROUND}$  after the completion of  $\mu$ SOF EOP transmission.
- eDSPn shall declare device disconnect if It has not received any analog pings from the device after the end of HS EOP of a  $\mu$ SOF packet.



**Figure 4-5: Illustration of Device Transmitting an Analog Ping**

- t0. eDSPn starts transmitting EOP of  $\mu$ SOF. Note that it is only 8 UIs instead of 40 UIs. This allows 32 UIs for the eUSB2 bus to turnaround and eUSPn to transmit the analog ping.
- t1. eDSPn completes packet transmission and both eDSPn/eUSPn enter L0 idle.
- t2. eUSPn starts transmitting the analog ping to announce its presence.
- t3. eUSPn completes the analog ping transmission.
- t4. eDSPn and eUSPn enter L0 idle.

Figure 4-6 illustrates a device silently disconnecting from an established HS link.



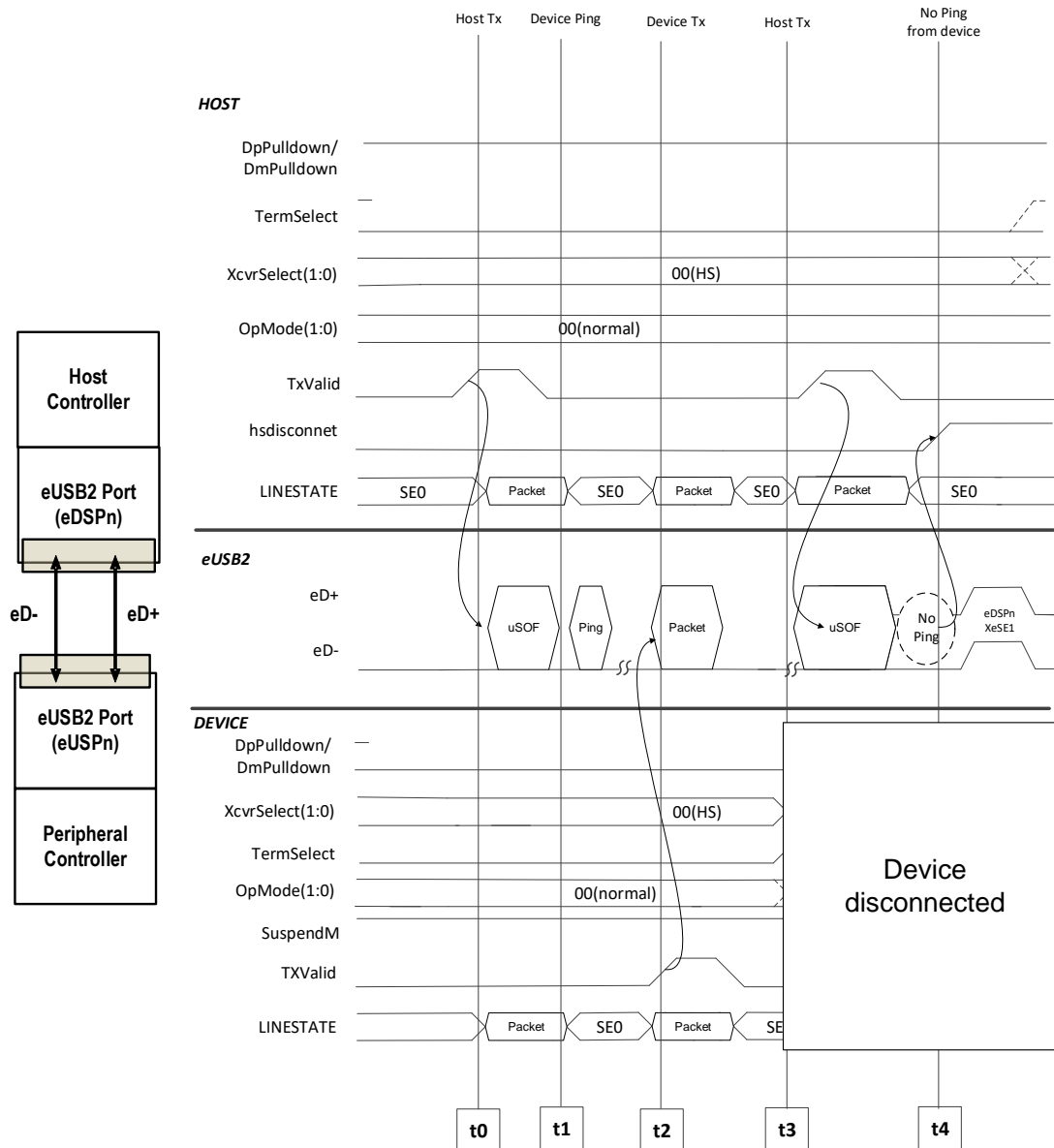


Figure 4-6: HS disconnect in L0

- t0:
- eDSPn transmits  $\mu$ SOF packet.
- t1:
- eUSPn transmits analog ping at  $\mu$ SOF EOP.
- t2:
- eUSPn transmits data packet.
  - Analog ping not required from eDSPn.
- t3:
- eDSPn transmits  $\mu$ SOF packet.
  - eUSPn disconnected, hence no analog ping returns to eDSPn.
- t4:
- eDSPn declares device disconnect after not receiving analog ping within 32 UIs of  $\mu$ SOF and reflecting UTMI+ disconnect to its host.

- eDSPn transmits Port Reset for a potential new USB session and to recover the link from a possible error condition.

#### 4.2.3.3.2 *Port Reset (XeSE1) in L0*

eUSPn and eDSPn utilize Port Reset (XeSE1) to reset the link as described below:

- eUSPn as directed by its controller to perform a soft disconnect.
- eUSPn shall perform Port Reset upon reconnect if a silent disconnect occurred.
- eDSPn shall also declare device disconnect when a device Port Reset is received.

#### **4.2.3.4 *High-Speed Disconnect Detect during L1, L2, End of Resume, or End of Reset***

##### 4.2.3.4.1 *Digital/Analog Ping*

eDSPn does not perform disconnect detection at the end of Reset or end of Resume to HS as opposed to FS/LS since eUSPn is not expected to transmit digital/analog ping at the end of Reset or Resume when entering HS. HS disconnect during these scenarios will be detected during the next SOF transmission from eDSPn.

##### 4.2.3.4.2 *Port Reset (XeSE1) in L1 or L2*

eUSPn and eDSPn utilize Port Reset (XeSE1) to reset the link in L1 or L2 as described below:

- eUSPn as directed by its controller to perform a soft disconnect.
- eDSPn shall declare device disconnect when Port Reset is detected.

### 4.3 PHY State Transition and Power Management

A conceptual eUSB2 PHY state machine is shown in Figure 4-7. It summarizes the basic behavior of the eUSB2 native operation during power-up, Connect, Reset, Resume and and Remote Wake. The state machine and native mode operation are described in detail in this section. Note that the state machine only describes the state transitions under normal operating conditions. Error situations may exist. It is implementation's responsibility to deal with potential error conditions in each state. It is recommended that eDSPn and eUSPn issue Port Reset to recover from these error conditions.

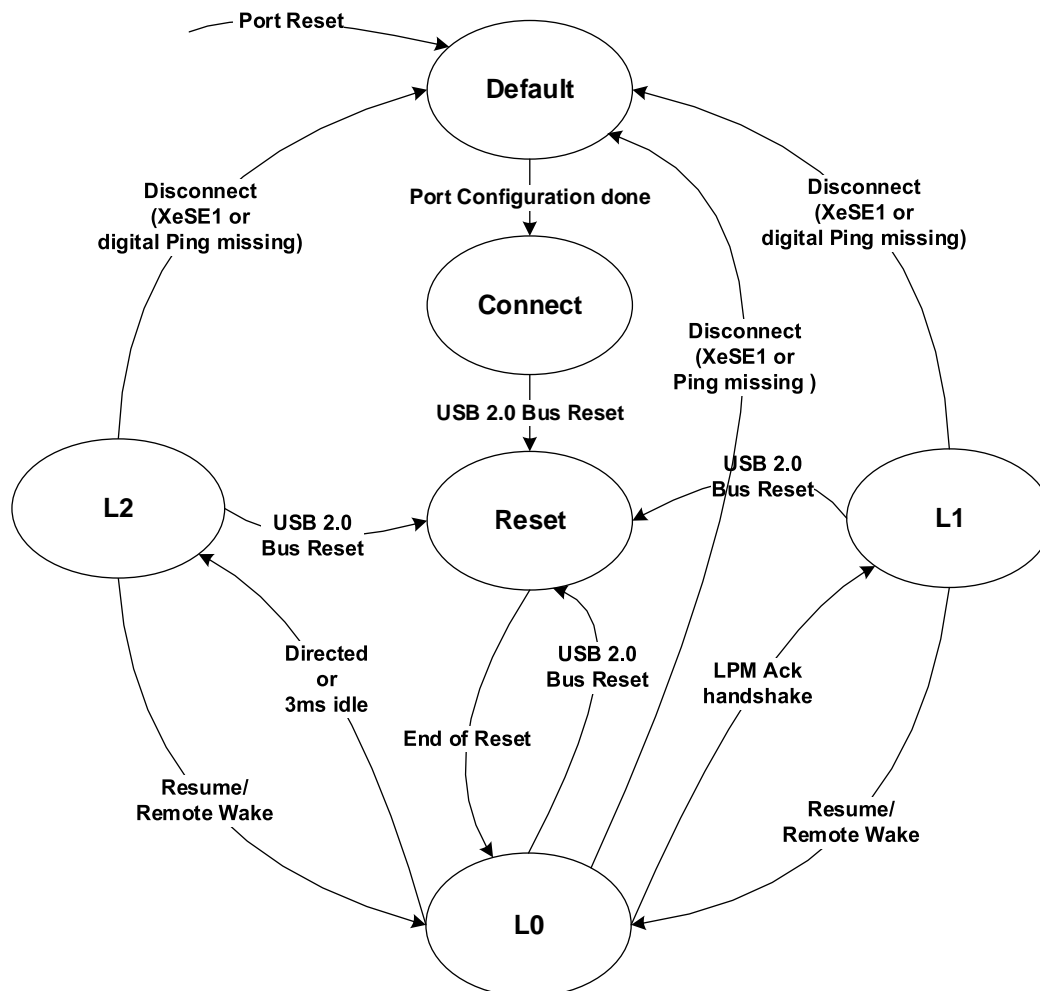


Figure 4-7: eUSB2 Native Link State Machine

#### 4.3.1 Default

The power-up sequence may be asynchronous between a downstream port and an upstream port. The mechanism for connect detection is different. Refer to Figure 4-8 for a power-up timing diagram. The port shall perform the following upon power-up:

eDSPn shall perform the following:

- It shall enable  $R_{PD}$  at eD+ and eD-.

- It shall transmit Port Reset (XeSE1) as defined in Section 3.3.8 before disabling its transmitters.
- Upon completing Port Reset, it shall transmit Port Configuration as Section 4.2.2 and wait for eUSPn to acknowledge. Note that it may initiate RAP operation before Port Configuration. Refer to Chapter 6 for details about RAP operations.

eUSPn shall perform the following:

- It shall enable  $R_{PD}$  at eD+ and eD-.
- It shall monitor for Port Reset, Port Configuration or CM.RAP from eDSPn. Note that due to the asynchronous POR of eDSPn and eUSPn, eUSPn may miss Port Reset completely. It may also sample at any point of the Port Reset (XeSE1), or CM.RAP that may be un-recognizable. eUSPn shall ignore these incomplete signalings. For example, it shall differentiate RAP address or write data that is all ones from Port Configuration.
- It shall transmit an acknowledgement upon detecting eDSPn Port Configuration as defined in Section 4.2.2.

eDSPn and eUSPn shall make the following transition from Default.

- eDSPn and eUSPn shall transition to Connect upon completion of Port Configuration.

### 4.3.2 Connect

Connect is a state where the eUSPn is attaching to its eDSPn.

- eUSPn shall perform the following after acknowledging to eDSPn Port Configuration:
  - If the port operates at full-speed/high-speed, and observes eSE0 at eD+/eD- and UTMI+ OpMode is not non-driving, it shall drive logic '1' at eD+.
  - If the port operates at low-speed and observes eSE0 at eD+/eD- and UTMI+ OpMode is not non-driving, it shall drive logic '1' at eD-.
  - Upon declaring an acknowledgement from eDSPn, eUSPn shall perform the following:
    - If it operates at full-speed/high-speed, it shall drive logic '0' at eD+ for  $T_{eSE0\_DR\_LSFS}$  and then disable its eD+ transmitter.
    - If it operates at low-speed, it shall drive logic '0' at eD- within  $T_{eSE0\_DR\_LSFS}$  and disable its transmitter.
- eDSPn shall perform the following:
  - It shall monitor for device connect.
  - Upon detecting device connect, It may (shall debounce with mechanical hotplug) perform debounce. The debounce period is implementation specific depending on the platform requirements. It shall declare device connect and acknowledge the device accordingly based on one of the following:
    - If it has detected logic '1' at eD+ and logic '0' at eD-, it shall start driving logic '1' at eD-.
    - If it has detected logic '0' at eD+, and logic '1' at eD-, it shall start driving logic '1' at eD+.
  - eDSPn shall complete the connect acknowledgement and declare the following:
    - If it is driving logic '1' at eD- for acknowledgement, and observes logic '0' at eD+, it shall drive logic '0' at eD- and declare full-speed/high-speed device connect.
    - If it is driving logic '1' at eD+ for acknowledgement, and observes logic '0' at eD-, it shall drive logic '0' at eD+ and declare low-speed device connect.

Refer to Figure 4-8 for a FS connect timing diagram.

eDSPn and eUSPn shall make the following transitions from Connect.

- eDSPn and eUSPn shall transition to Reset upon completion of device connect.
- eDSPn and eUSPn shall transition to Default if directed or upon detecting Port Reset.

### 4.3.3 Reset

In the Reset state, both eUSPn and eDSPn are waiting for or performing a USB 2.0 Bus Reset and high-speed negotiation, respectively.

- eUSPn shall perform the following:
  - It shall declare USB 2.0 Bus Reset upon detection of logic '1' on eD+ for FS or logic '1' on eD- for LS.
  - It shall transmit Chirp K directed by its controller to start the high-speed negotiation.
  - It may expect host chirp K-J from eDSPn before the end of reset and shall reflect this to its UTMI+ interface to its device controller. Refer to Figure 4-9 for HS negotiation. Note: eUSPn may not observe host K-J chirp (for a FS only host). In this event eUSPn shall maintain eSE0 at eD+/eD- after Chirp K and expect FS EOReset from eDSPn.
  - It shall end USB 2.0 Bus Reset and reflect this to its UTMI+ interface, if it detected EOReset as defined in Section 3.3.4.
- eDSPn shall perform the following:
  - When directed by the host controller, it shall transmit a logic '1' on eD+ for FS device connect or logic '1' on eD- for LS device connect respectively to initiate USB 2.0 Bus Reset.
  - It shall perform the high-speed detection as defined in USB 2.0 specification.
  - It may expect Chirp K from the eUSPn indicating a HS capable device.
  - It shall perform host K-J chirp as directed by its controller. Note: eDSPn may not be directed to transmit host K-J chirp if it is not HS capable.
  - When directed by its host, it shall conclude USB 2.0 Bus Reset with EOReset as defined in Chapter 3.
- eDSPn and eUSPn shall make the following transition from Reset.
  - eDSPn and eUSPn shall transition to L0 upon completion of USB 2.0 Bus Reset.

#### 4.3.3.1 FS link Reset timing diagram

Figure 4-8 below illustrate the timing flow of a native eUSB2 host and device establishing a FS link.

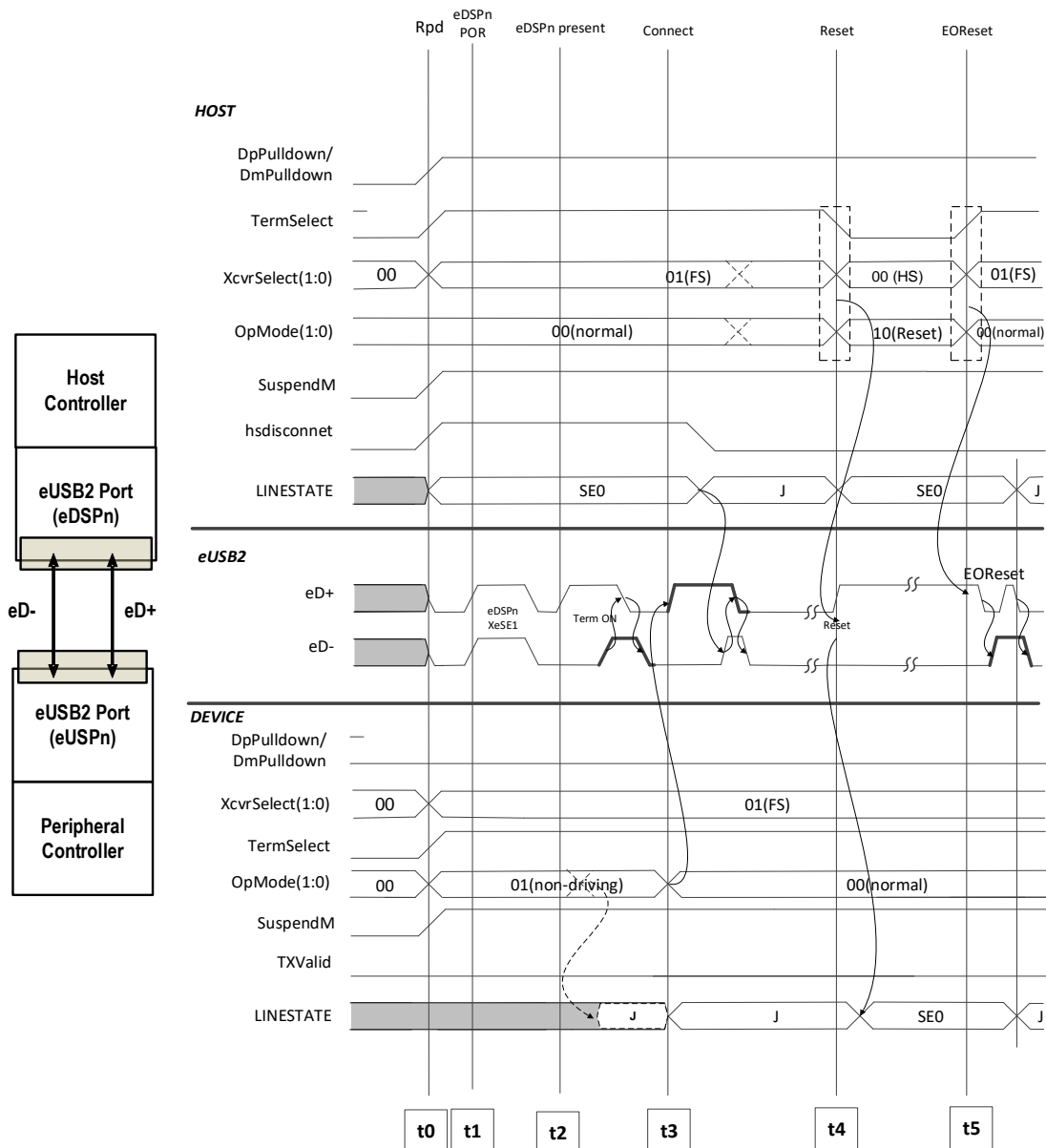


Figure 4-8: FS connect

- t0:
- Both eDSPn and eUSPn power up and turn on its R<sub>PD</sub> respectively. Note: This event may be asynchronous as both eDSPn and eUSPn may be powered up at a different time.
- t1:
- eDSPn POR and transmits Port Reset.
- t2:
- eDSPn initiates Port Configuration with termination enabled.
  - eUSPn acknowledge present announcement.

t3:

- eUSPn signals connect with logic '1' on eD+ as directed by its device controller.
- eDSPn acknowledges eUSPn device connect with a logic '1' on eD- and reflect device connect on its UTMI+ interface.
- Note: as illustrated with the dotted arrow, UTMI+ opmode may have transition to "normal" earlier (or at time zero). In this scenario, eUSPn shall change its UTMI+ LineState to J but only transmit logic '1' on eD+ after it has completed port reset announcement.
- eUSPn drives a logic '0' (before releasing to R<sub>PD</sub> idle), upon detecting a logic '1' acknowledgement from eDSPn,
- eDSPn drives logic '0' (before releasing to R<sub>PD</sub> idle), upon detecting a logic '0' from eUSPn.

t4:

- eDSPn drives logic '1' on eD+ (R<sub>PD</sub> on eD-) representing a USB 2.0 Bus Reset SE0. Note: Depending on implementation, UTMI+ xcvrselect and opmode and termselect may change at same UTMI clock cycle or few cycles apart with respect to each other. The trigger for USB 2.0 Bus Reset will be at the UTMI clock cycle at which all the signals reach their relevant values.
- eUSPn reflects USB 2.0 Bus Reset to its UTMI+ interface.

t5:

- eDSPn ends USB 2.0 Bus Reset with Reset EOP. Note: Depending on implementation, UTMI+ xcvrselect and opmode and termselect may change at same UTMI clock cycle or few cycles apart with respect to each other. The trigger for USB 2.0 Bus Reset will be at the UTMI clock cycle at which all the signals reach their relevant values.
- eUSPn responds with a digital ping as defined in Section 4.2.3.2.

#### 4.3.3.2 HS link Reset timing diagram

Figure 4-9 below illustrate the timing flow of a native eUSB2 host and device establishing a HS link.

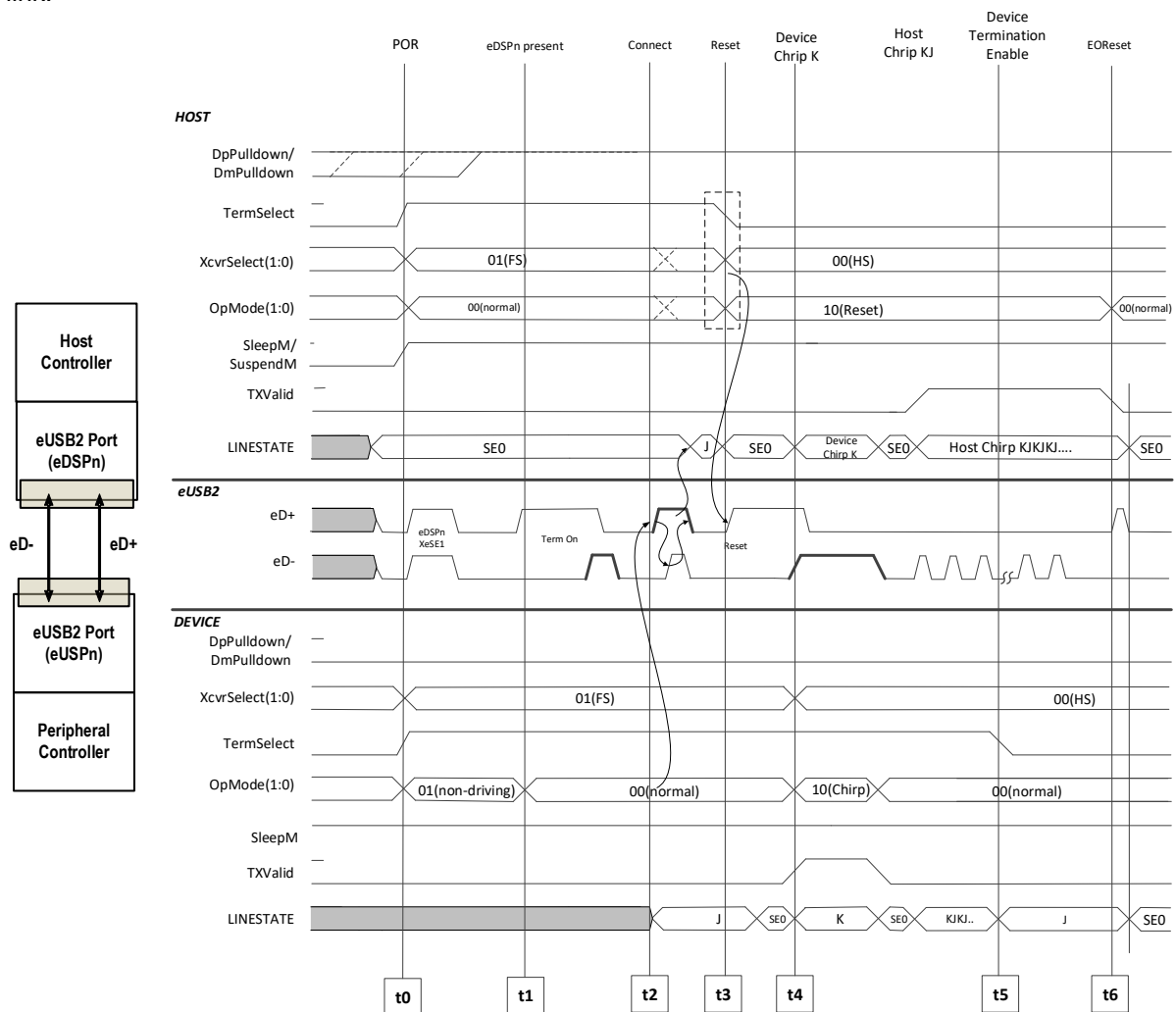


Figure 4-9: HS connect

- t0:
- eDSPn POR transmits Port Reset.
- t1:
- eDSPn initiates Port Configuration with termination enable.
  - eUSPn acknowledge.
- t2:
- eUSPn announces device connect with logic '1' on eD+ as directed by its device controller.
  - eDSPn acknowledges eUSPn device connect with a logic '1' on eD- and reflects device connect on its UTMI+ interface.
  - eUSPn drives a logic '0' (before releasing to R<sub>PD</sub> idle), upon detecting a logic '1' acknowledgement from eDSPn,
  - eDSPn drives logic '0' (before releasing to R<sub>PD</sub> idle), upon detecting a logic '0' from eUSPn.



- t3:
- eDSPn drives logic '1' on eD+ (R<sub>PD</sub> on eD-) presenting a USB 2.0 Bus Reset.
  - Note: Depending on implementation, UTMI+ xcvrselect and opmode and termselect may change at same UTMI clock cycle or few cycles apart with respect to each other. The trigger for USB 2.0 Bus Reset will be at the UTMI clock cycle at which all the signals reach their relevant values.
  - eUSPn reflects USB 2.0 Bus Reset to its UTMI+ interface.
- t4:
- eUSPn transmits device chirp as directed by its device controller.
  - eDSPn drops eD+.
  - eDSPn HS K-J chirp sequence follows.
- t5:
- eUSPn observes a change on TermSelect from 1 to 0 and starts emulating LineState as J at UTMI+ until HS EOReset is completed. It shall not send any HS termination pulse at eD+ to eDSPn.
- t6:
- eDSPn transmits EOReset to complete speed negotiation.
  - Note: Depending on implementation, UTMI+ xcvrselect and opmode and termselect may change at same UTMI clock cycle or few cycles apart with respect to each other. The trigger for USB 2.0 Bus Reset will be at the UTMI clock cycle at which all the signals reach their relevant values.
  - Note: no digital ping transmitted from eUSPn in HS operation.

#### 4.3.4 L0

The policies of the link operation in L0 are the same as USB 2.0. eDSPn and eUSPn shall meet the following requirements.

- eDSPn and eUSPn shall adhere to the rules defined in Chapter 3 and Section 4.2.3 for USB 2.0 packet transfer and device disconnect detection.
- In L0 idle, eDSPn and eUSPn shall have its SE Rx enabled for Port Reset or device soft disconnect. In HS operation, both ports shall enable the Squelch detector at the receiver.
- In FS/LS operations, in case a controller did not direct eDSPn or eUSPn to L1 or L2, eDSPn and eUSPn may remain in L0. eDSPn and eUSPn shall map the eUSB2 bus state to LineState, perform Remote Wake and Resume as directed by their controllers. The operation behaviors of Remote Wake and Resume in L0 shall be the same as L1 or L2.

eDSPn and eUSP shall make the following transitions from L0.

- eDSPn shall transition to Reset if directed to transmit USB 2.0 Bus Reset. eUSPn shall transition to Reset if USB 2.0 Bus Reset is detected. Refer to Section 3.3 for USB 2.0 Bus Reset Signaling.
- eDSPn and eUSPn shall transition to L1 or L2 when directed.
- eDSPn shall transition to Default if absence of device Ping is declared.
- eDSPn and eUSPn shall transition to Default if directed or upon detecting Port Reset.

#### 4.3.5 L1, L2

L1 and L2 are two low power link states defined by the USB 2.0 specifications. The behavioral requirements of eDSPn and eUSPn are similar except for exit latency and power state in L1 and L2. The policies for Resume and Remote Wake are the same as USB 2.0.

##### 4.3.5.1 Resume

For Resume from L1 and L2, the port shall adhere to the following rules.

eUSPn shall perform the following:

- Upon detecting the Resume signal, it shall proceed to exit from suspend based on the following:
  - If operating at full-speed, it shall transmit a digital ping at eD- as defined in Chapter 3 upon detecting EOResume eD+ and enter L0.
  - if operating at low-speed, it shall transmit a digital ping at eD+ as defined in Chapter 3 upon detecting EOResume at eD- and enter L0.
  - If operating at high-speed before entering L1 or L2, it shall enter L0 upon detecting the end of Resume.

eDSPn shall perform the following:

- It shall initiate Resume by transmitting the Resume K defined below with timing defined in USB 2.0.
  - If operating at full-speed/high-speed, it shall drive the Resume K at eD-.
  - If operating at low-speed, it shall drive the Resume K at eD+.
- It shall conclude Resume by signaling EOResume as defined in Section 3.3.5.

Figure 4-10 shows the timing diagram of a FS link suspend entry and Resume.

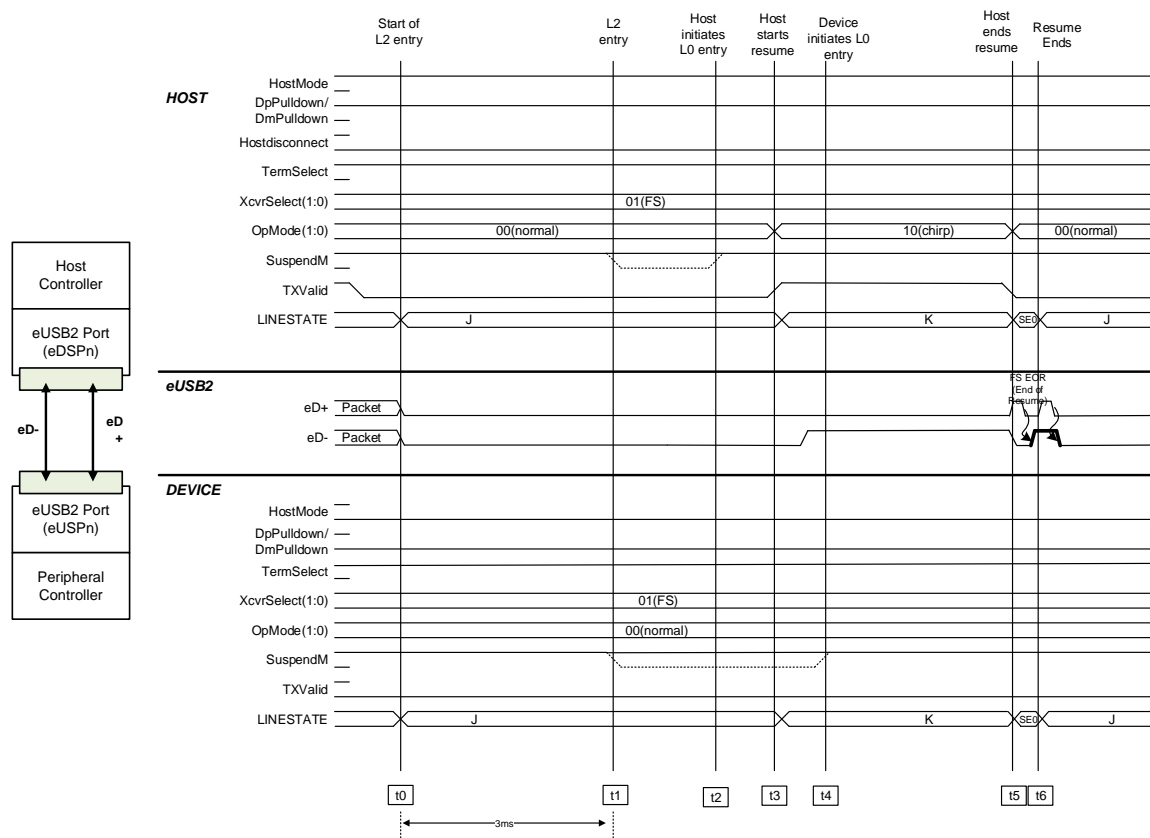


Figure 4-10: FS L2 & Resume

t0:

- eDSPn initiates L2 entry as directed by its host controller with link going idle.

t1:

- eUSPn initiates L2 entry upon 3ms as directed by its device controller.
- Link enters L2.

- t2:
- eDSPn initiates L0 entry as directed by its controller.
- t3:
- eDSPn starts Resume process as directed through its controller.
  - eDSPn transmits logic '1' on eD- as Resume.
- t4:
- eUSPn prepares for L0 entry as directed by its controller.
- t5:
- eDSPn ends Resume with EOResume.
- t6:
- if FS or LS, eUSPn responds with a digital ping as defined in Section 3.3.5.1.1.
  - Both eDSPn and eUSPn enter L0.

#### **4.3.5.2 Remote Wake from L1 and L2**

For Remote Wake from L1 and L2, the port shall adhere to the following rules.

- eUSPn shall initiate Remote Wake based on the signaling defined in Section 3.3.6. Note that in the event of host not responding to the wake, an RC discharge would be observed on the eUSB2 bus as illustrated in Section 3.3.6.1.1.
- eDSPn, upon detecting Remote Wake, shall acknowledge with the Resume signaling defined in Section 3.3.6 within  $T_{URSM}$  as defined by the USB 2.0. It shall complete Resume with EOResume as defined in Section 3.3.5.1.1. If host controller may not be able to direct eDSPn to start resume within  $T_{URSM}$ , eDSPn may implement the optional auto-resume defined in Section 3.3.7.1.1 to initiate Resume.

Shown in Figure 4-11 is an example timing diagram of a link operating in FS from entry to L2, to eUSPn initiating Remote Wake, and eDSPn responding with Resume.

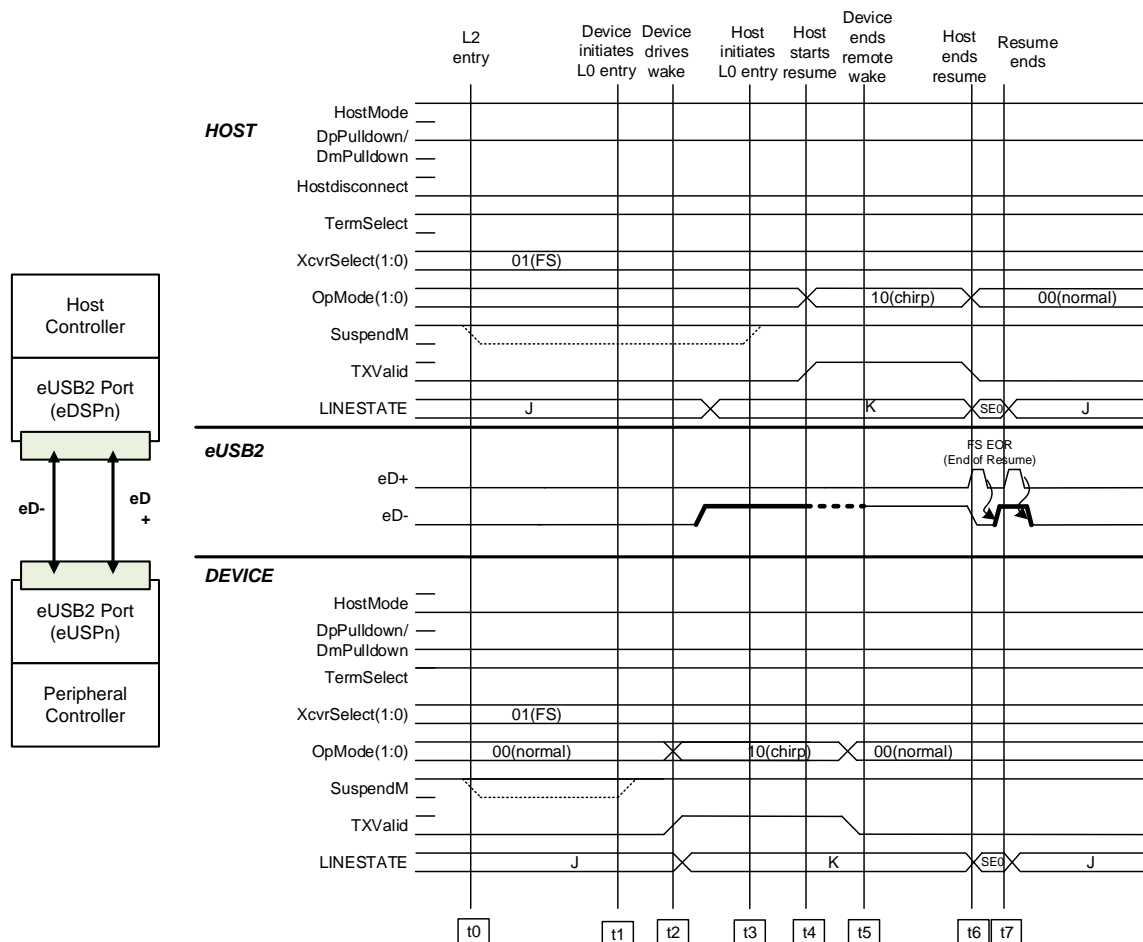


Figure 4-11: FS L2 &amp; Remote Wake

- t0:
- Link enters L2 upon SuspendM assertion.
- t1:
- eUSPn prepares for return to L0 entry as directed by its controller.
- t2:
- eUSPn starts Remote Wake process as directed by its controller.
  - eUSPn transmit logic '1' on eD- as wake.
- t3:
- eDSPn prepares for return to L0 entry as directed by its controller.
- t4:
- eDSPn starts Resume process as directed by its controller.
  - eDSPn transmits logic '1' on eD- as Resume.
- t5:
- eUSPn ends Remote Wake as directed through its controller.
- t6:
- eDSPn ends Resume with EOResume.
  - eUSPn responds with a digital ping as defined in Section 3.3.5.1.1.
  - Both eDSPn and eUSPn enter L0.

#### **4.3.5.3 Disconnect in L1 or L2**

As the eUSB2 bus would remain as eSE0 before and after disconnect, eUSPn and eDSPn shall perform the follow during disconnect and reconnect.

- Upon directed to perform a soft disconnect, eUSPn shall transmit a Port Reset announcement, XeSE1 to eDSPn to terminate the current session.
- If the device is undergoing a silent disconnect, it is system level implementation to ensure a sideband communication to inform eDSPn.

#### **4.3.5.4 Reset during L1 or L2**

An upstream port in L1, or L2 shall enter reset if it has detected Bus Reset as defined in Section 3.3.4.

#### **4.3.5.5 Exit from L1 or L2**

The exit conditions from L1 to other link states are the same as the ones from L2. eDSPn and eUSPn shall make the following transitions.

- eDSPn shall transition to Reset if directed to issue USB 2.0 Bus Reset. eUSPn shall transition to Reset is USB 2.0 Bus Reset is detected
- eDSPn and eUSPn shall transition to L0 when a successful Resume is achieved.
- In FS/LS operation, eDSPn shall transition to Default is the digital Ping is not received during EOResume.
- eDSPn and eUSPn shall transition to Default if directed or upon detecting Port Reset.

## **5 eUSB2 Repeater Architecture and Operation**

This chapter describes the architecture and operation of an eUSB2 Repeater compliant to USB 2.0 specification.

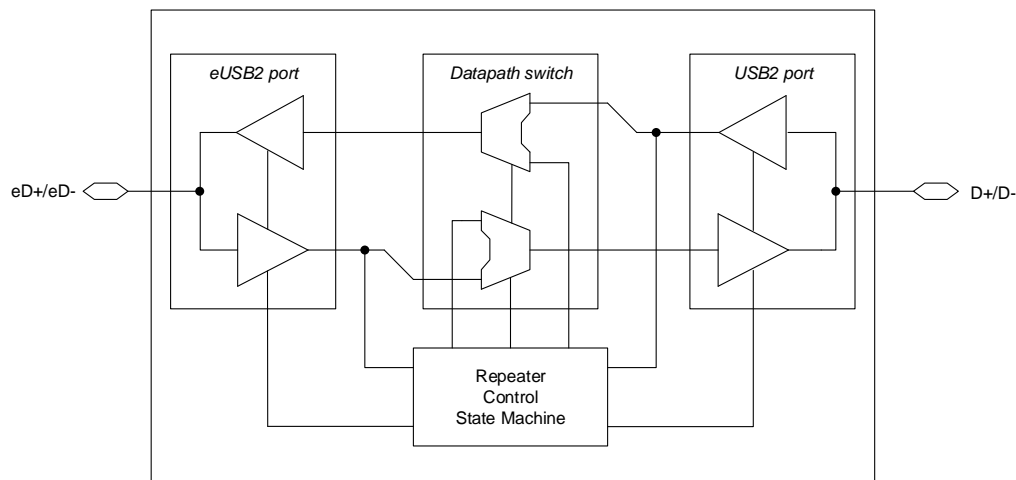
### **5.1 eUSB2 Repeater**

An eUSB2 Repeater is working with an eUSB2 PHY in SOCs to support these possible configurations.

- USB 2.0 host root hub DFP (Host Repeater)
- USB 2.0 peripheral UFP (Peripheral Repeater)
- USB 2.0 Dual-role port (Dual-role Repeater)

#### **5.1.1 Architecture and Interface**

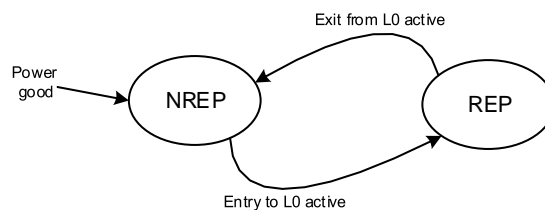
The architecture of an eUSB2 repeater is a half-duplex non-linear redriver. A simplified eUSB2 repeater block diagram is shown in **Figure 5-1**.



**Figure 5-1: Dual-Role Repeater Architecture**

### 5.1.2 Signaling Modes

An eUSB2 Repeater at any given time operates in one of the two signaling modes. This is shown in Figure 5-2.



**Figure 5-2: eUSB2 Repeater Operation Mode**

- REP is a repeating signaling mode where packets are forwarded between eD+/eD- and D+/D-, with end to end timing preserved to meet the timing requirements defined by USB 2.0 and eUSB2 specifications.
- NREP is a non-repeating signaling mode when the link is in one of the following states.
  - Initialization during Configuration, Connect, Reset and Speed Negotiation.
  - Resume and Remote Wake in L1 and L2 Suspend with additional XeSE1 and CM.Reset.
  - L0 while a control message or XeSE1 is being transmitted by local eDSPr/eUSPr to its associated Repeater. Possible control messages include CM.Reset or CM.FS (CM.L1) or CM.L2.

Timing in NREP mode is not as critical as in REP mode since the information transmitted is for control and status reporting purposes such as Wake, Resume, USB 2.0 Bus Reset, Disconnect or Connect announcement (XeSE1), Control Message, Chirp, or Repeater Configuration.

### 5.1.3 Repeater Operation

Shown in Figure 5-3 are example block diagrams of a host repeater and a peripheral repeater with their respective host and peripheral eUSB2 port and controller. Note that the eUSB2 port and

the repeater may be implemented as dual-role capable. The details of a dual-role repeater implementation are described in the following sections.

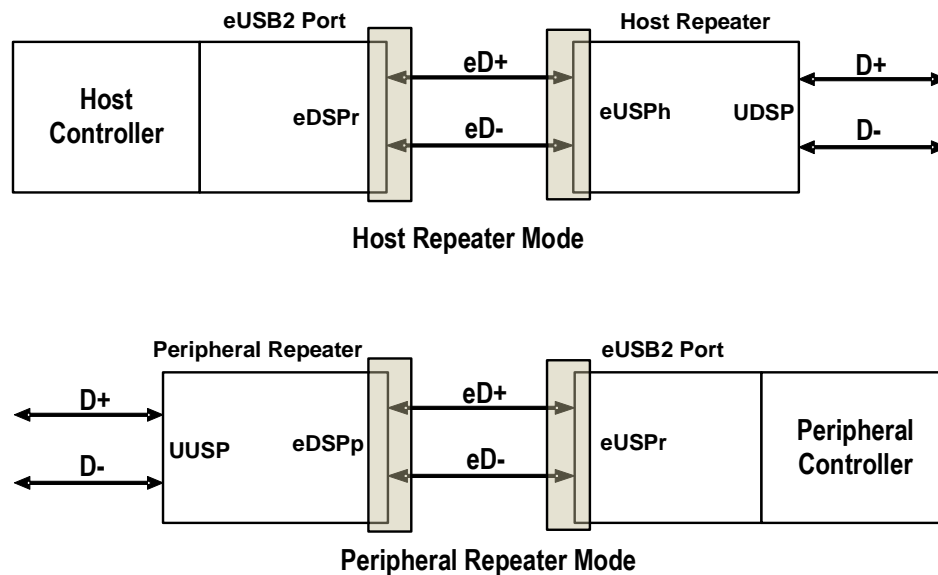


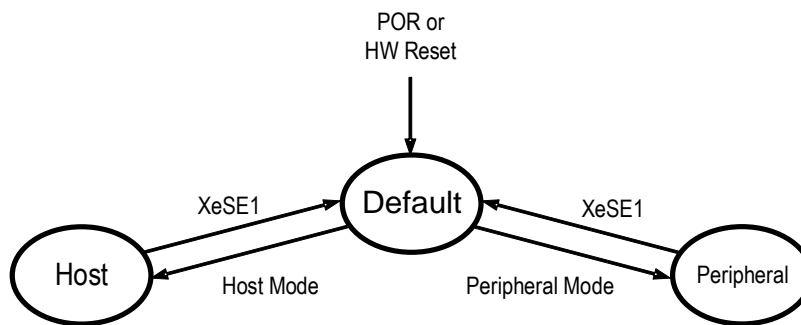
Figure 5-3: eUSB2 Repeater in Host or Peripheral Mode

## 5.2 Dual-Role Repeater State Machine

An informative two-level state machine of an eUSB2 dual-role repeater is defined. The top-level state machine defines the operation of an eUSB2 repeater from power-up. The second-level state machine defines the repeater operation in the host or peripheral mode upon entering the USB session.

### 5.2.1 Top Level Repeater State Machine

Shown in Figure 5-4 is the top-level dual-role repeater state machine. Note that the state machine also applies to a single-role host or peripheral repeater.



**Figure 5-4: Top-Level eUSB2 State Machine**

### 5.2.2 Default

Default is the power-on state upon POR or HW reset. In this state the repeater is waiting for configuration from eUSBr (yet to be configured eUSB2 port). To decouple any USB 2.0 protocol from CM.RAP and to avoid unnecessary contention, CM.RAP communication shall occur only in this state (prior to Repeater Configuration).

- This is a state the repeater or eUSBr shall transition to upon transmitting or receiving Port Reset.
- A repeater in this state shall disable its USB 2.0 transceiver and enable its SE receivers at eD+/eD-.
- The repeater's eUSB port shall be maintained as eSE0 with  $R_{PD}$ .
- The repeater in this state shall not transmit any signaling but monitor its eUSB2 port for Port Reset, Repeater Configuration or CM.RAP from eUSBr. Due to the asynchronous POR of both the repeater and the associated eUSBr port, the repeater may sample at any point of the Port Reset (XeSE1), or CM.RAP that may be un-recognizable. The repeater shall ignore these incomplete signalings and move on to receiving the next CM.RAP or Repeater Configuration.
- eUSBr, upon POR or HW reset, shall transmit Port Reset.
- eUSBr, upon completing Port Reset, shall configure the repeater by transmitting Repeater Configuration when directed. An eUSBr shall perform one of the following.
  - It shall transition to Host as eDSPr after Host repeater configuration is acknowledged.
  - It shall transition to Peripheral as eUSPr after Peripheral repeater configuration is acknowledged.
- A repeater, upon detecting Repeater Configuration, shall send an ACK and transition to Host mode or Peripheral mode operation accordingly.
- eUSBr shall end Repeater Configuration and declares itself as eDSPr or eUSPr upon detecting an acknowledgment from the repeater by  $T_{CONFIG\_CMPL}$ .
- Upon completing Repeater Configuration, eDSPr/eUSPr shall ensure an idle time of  $T_{CONFIG\_IDLE}$  before transmitting the next signaling (e.g. Connect announcement from eUSPr)
- eUSBr may keep its UTMI+ interface to the controller to implementation specific idle state (i.e. SE0 on LineState) while configuring its repeater.



- eDSPr shall reconfigure its repeater with Repeater Configuration if Port Reset is received for HS device disconnect. Note that eDSPr may utilize Port Reset to instruct its repeater to transition to Default if its port is disabled (it is implementation specific how a host controller indicates port disable to its physical layer).

### 5.2.3 Host

Host is a state where an eUSB2 repeater is configured as a host repeater, and its associated eUSBr acts as eDSPr.

- eDSPr shall enter Default if one of the following conditions is met.
  - Upon completing Port Reset, if directed. Note that this is implementation specific on the interface from host controller to direct its associated PHY to perform Port Reset or terminate an existing USB session. One possibility for triggering Port Reset is the Non-driving UTMI+ OpMode setting. Alternately, if the UTMI+ DpPulldown or DmPulldown toggles, the eDSPr would signal Port Reset to reconfigure the repeater.
  - Upon detecting the Device Disconnect Announcement from the host repeater in HS operation.
- A host repeater shall enter Default if one of the following conditions is met.
  - Upon completing the HS Device Disconnect Announcement.
  - Upon detecting Port Reset.

### 5.2.4 Peripheral

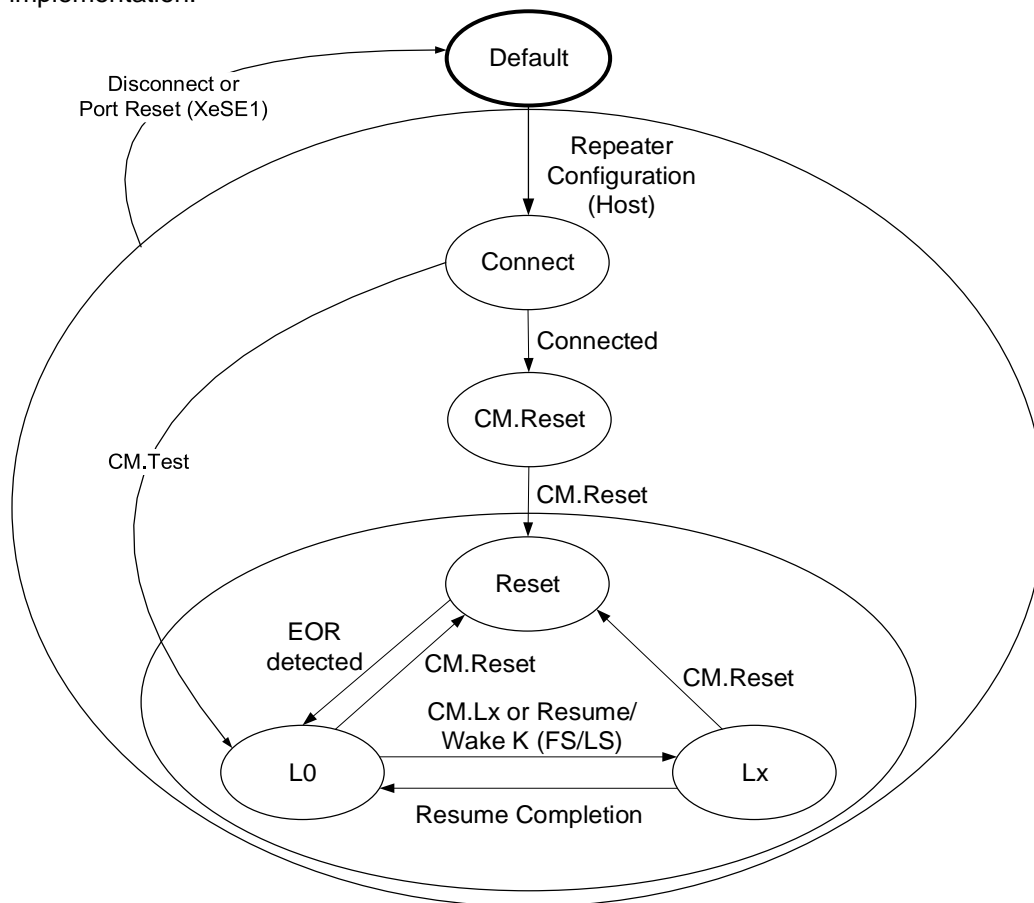
Peripheral is a state where a repeater is configured as a peripheral repeater, and its associated eUSBr acts as eUSPr.

- eUSPr shall enter Default if directed and after Port Reset is transmitted.
- A peripheral repeater shall enter Default if Port Reset is received.

### 5.3 Host Repeater Operation

This section describes basic operations of an eUSB2 host repeater with its associated eDSPr. An example host mode repeater state machine is shown in Figure 5-5.

Note: eDSPr implementation may have a different state or state transition than the repeater. Below diagrams and description are an informative, not normative guide to eDSPr implementation.



**Figure 5-5: Host Mode Repeater State Machine**

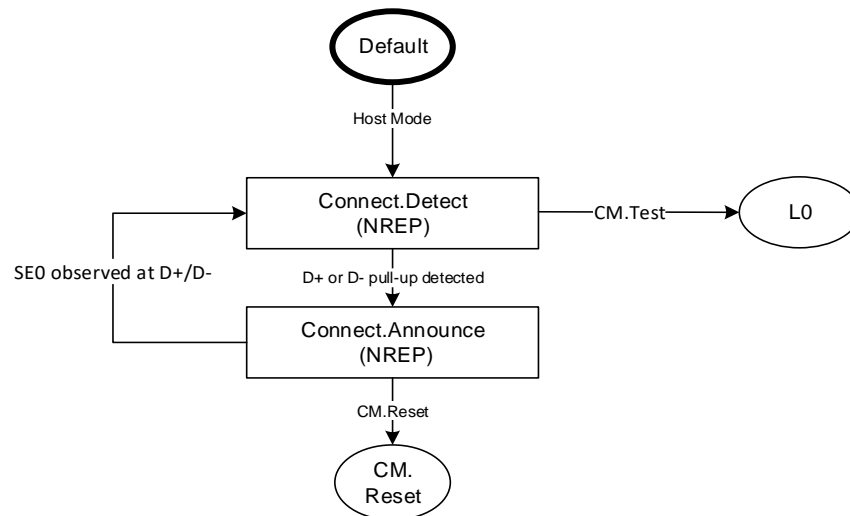
#### 5.3.1 Connect

Connect is a state where the repeater operates under NREP mode. Repeater in this state shall monitor for device connect.

Section 5.5.1 illustrates a host repeater link detecting a FS connection upon POR.

Section 5.5.4 shows a host repeater detecting a peripheral connection and establishing a HS link upon POR.

Connect contains two substates (implementation may combine these to one state) as shown in Figure 5-6.



**Figure 5-6: Connect Substates**

### 5.3.1.1 **Connect.Detect**

Connect.Detect is a substate where the host repeater enables the FS transceiver at its UDSP in preparation for device connect.

#### 5.3.1.1.1 *Connect.Detect Requirements*

The repeater shall meet the following conditions.

- It shall keep its  $R_{PD}$  enabled at both eD+ and eD-.
- The FS transceiver at its UDSP shall be enabled.
- It shall perform USB 2.0 device connect by monitoring the USB 2.0 bus state at D+/D-.
- It shall return to Default if Port Reset is received.
- It should be in the lowest power state while monitoring for a device attach at the USB 2.0 bus or Port Reset from eDSPr where both events are not timing critical. Note: It may turn off its UDSP SE receiver if device attach detection is performed out-of-band.
- It shall perform SCM detection and control message decoding for CM.Test.

eDSPr shall meet the following conditions.

- It shall keep its  $R_{PD}$  enabled at both eD+ and eD-.
- It shall transmit CM.Test as directed with the UTMI+ xcvrselect and termselect in HS and LineState is SE0. Note that additional UTMI+ interface signals may change in other host controller implementations. Further, CM.Test shall be transmitted in an unconnected state where the eUSB2 bus state is eSE0.

#### 5.3.1.1.2 *Exit from Connect.Detect*

The repeater shall perform the following tasks.

- It shall transition to Connect.Announce if D+ or D- pull-up is detected.
- It shall transition to Default if Port Reset is received.
- It shall transition to L0 and enable its HS termination for USB 2.0 HS Compliance Test if CM.Test is received.

eDSPr shall perform the following tasks.

- It shall transition to L0 and enable its HS termination for USB 2.0 HS Compliance Test upon successfully completing CM.Test to eUSPh.

### 5.3.1.2 **Connect.Announce**

Connect.Announce is a substate where the repeater relays the USB 2.0 device connect event through its eUSB2 port to eDSPr until it detects the host CM.Reset.

#### 5.3.1.2.1 *Connect.Announce Requirements*

The repeater shall meet the following conditions.

- It shall map the USB 2.0 to eUSB2 bus state as defined in Table 5-1. Note that the repeater's bus state mapping defined in Table 3-1 does not apply in this state. It is applicable only after CM.Reset.
- It is not required to perform debounce or de-glitching on the USB 2.0 bus in any of the ensuing states.
- The repeater shall monitor for CM.Reset coming from its eDSPr for USB 2.0 Bus Reset.

**Table 5-1: USB 2.0 to eUSB2 bus state mapping during connect**

D+/D-	eD+/eD-	Note
SE0	eSE0	eD+/eD- are being maintained with R <sub>PD</sub>
SE1	eSE0	The host repeater shall not drive eSE1 on the eUSB2 bus. SE1 on USB 2.0 line is mapped to eSE0 on eUSB2 with R <sub>PD</sub>
High/Low	Logic '1'/R <sub>PD</sub>	Indicating a FS/HS device attach
Low/High	R <sub>PD</sub> /Logic '1'	Indicating a LS device attach
{High → Low}/Low	{Logic '1' → Logic '0' (T <sub>eSE0_DR_LSFS</sub> ) → R <sub>PD</sub> }/R <sub>PD</sub>	The host repeater shall drive eD+ logic '0' for T <sub>eSE0_DR_LSFS</sub> before maintaining logic '0' with R <sub>PD</sub>
Low/{High → Low}	R <sub>PD</sub> {Logic '1' → Logic '0' (T <sub>eSE0_DR_LSFS</sub> )} → R <sub>PD</sub>	The host repeater shall drive eD- logic '0' for T <sub>eSE0_DR_LSFS</sub> before maintaining logic '0' with R <sub>PD</sub>

eDSPr shall meet the following conditions.

- It shall enable its R<sub>PD</sub> at both eD+ and eD-.
- It shall reflect the eUSB2 bus state from eUSPh to its UTMI+ interface with the host controller.
- It shall not transmit CM.Lx to the repeater for Lx entry if UTMI+ SuspendM or an L1 enable is asserted..
- It shall stay in this state if USB 2.0 device connect is not declared.

#### 5.3.1.2.2 *Exit from Connect.Announce*

The repeater shall perform the following tasks.

- It shall transition to CM.Reset if it has detected CM.Reset from eDSPr.
- It shall transistion to Default if it has received Port Reset.

eDSPr shall perform the following tasks.

- It shall transition to CM.Reset when directed to perform USB 2.0 Bus Reset.

### 5.3.2 CM.Reset

CM.Reset is a state where the repeater operates under NREP mode. In this state, the repeater is receiving CM.Reset from eDSPr to perform a USB 2.0 Bus Reset.

#### 5.3.2.1.1 CM.Reset Requirements

The repeater shall meet the following conditions.

- It shall keep its R<sub>PD</sub> enabled at both eD+ and eD-.
- It shall perform SCM detection and control message decoding. Note that a repeater may also receive Port Reset and shall be able to distinguish it from SCM based on its local timer.
- It shall sample D+/D- to determine the attached device speed (i.e. FS/HS if D+ is pulled high, LS if D- is pulled high) upon detecting CM.Reset.
- UDSP of the repeater shall be in FS and continue monitoring the bus state at D+/D-.

eDSPr shall meet the following conditions.

- It shall keep its R<sub>PD</sub> enabled at both eD+ and eD-.
- It shall transmit CM.Reset when directed by its Host controller on its UTMI+ interface to perform a USB 2.0 Bus Reset.

#### 5.3.2.1.2 Exit from CM.Reset

The repeater shall perform the following tasks.

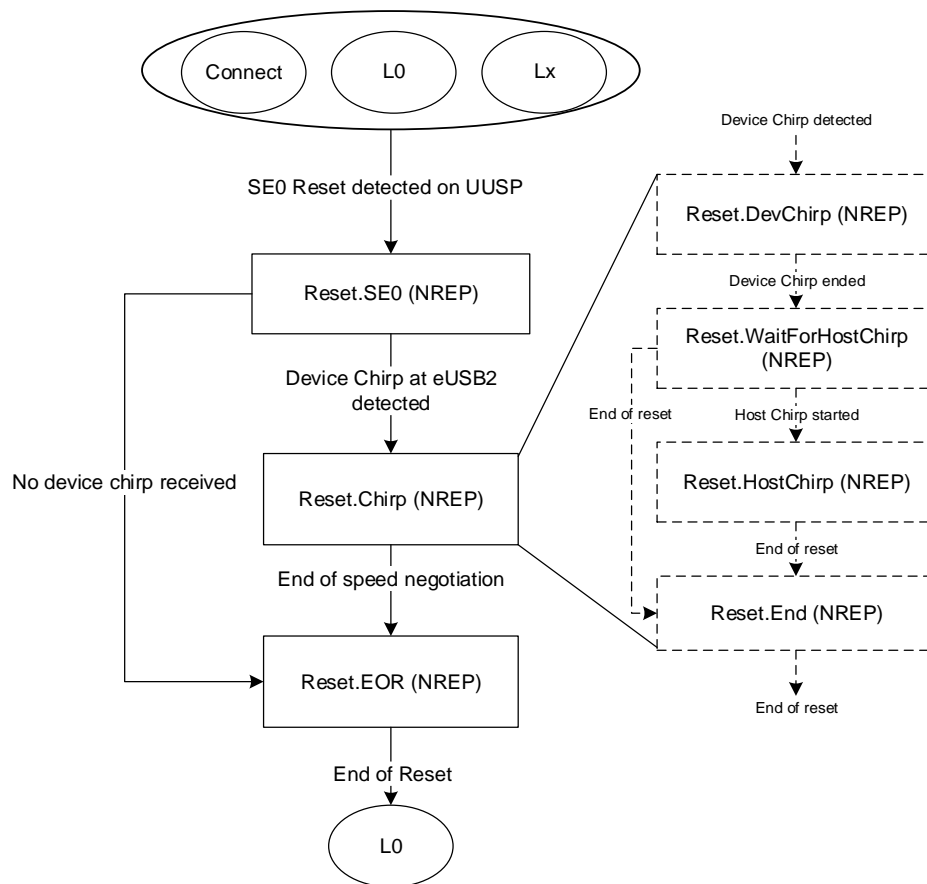
- It shall transition to Reset if eSE0 at eD+/eD- is detected after CM.Reset.
- The repeater shall transition to Default if it has detected Port Reset.

eDSPr perform the following task:

- It shall transition to Reset upon completing CM.Reset.

### 5.3.3 Reset

Reset is a state where the repeater operates under NREP mode. In this state: Reset contains multiple substates as shown in Figure 5-7. Sections 5.5.8, 5.5.9, 5.5.10, and 5.5.11 show various USB 2.0 Bus Reset and speed detection timing waveforms.



**Figure 5-7: Reset Substate Machine**

#### 5.3.3.1 Reset.SE0

Reset.SE0 is a substate where the repeater is driving USB 2.0 Bus Reset and expecting either speed negotiation or conclusion of reset.

##### 5.3.3.1.1 Reset.SE0 Requirements

The repeater shall meet the following condition:

- It shall keep its SE receivers enabled on eUSB2 bus.
- UDSP of the repeater shall drive USB 2.0 Bus Reset and monitor for device chirp to start speed negotiation.

eDSPr shall meet the following condition:

- It shall keep its SE receivers enabled in the event of device chirp.

##### 5.3.3.1.2 Exit from Reset.SE0

The repeater shall perform the following tasks.

- The repeater shall transition to Default if it has detected Port Reset.
- The repeater shall transition to Reset.Chirp if device chirp is detected at UDSP.

- The repeater shall transition to Reset.EOR if it is in FS operation and has detected logic '1' at eD+.
- The repeater shall transition to Reset.EOR if it is in LS operation and has detected logic '1' at eD-.

eDSPr shall perform the following tasks.

- It shall transition to Reset.Chirp if logic '1' is detected on eD-.
- It shall transition to Reset.EOR when directed to end USB 2.0 Bus Reset.

### 5.3.3.2 *Reset.Chirp*

Reset.Chirp is a substate where a high-speed device is connected, and the speed negotiation is performed. There are multiple stages of operations within Reset.Chirp to complete the speed negotiation, as shown in Figure 5-7. Section 5.5.4 shows the timing waveform of the reset chirp sequence.

#### 5.3.3.2.1 *Reset.Chirp Requirements*

The repeater shall meet the following conditions.

- It shall keep its high-speed transceivers and receiver terminations disabled at eD+/eD- during speed negotiation.
- UDSP shall meet the requirements defined by USB 2.0. The operation of speed negotiation shall meet the following conditions. The repeater shall perform the following during device Chirp K detection, reception, and forwarding:
  - If the device Chirp K is received, it shall drive logic '1' at eD-.
  - If the device Chirp K is concluded, it shall drive logic '0' at eD- for  $T_{eSE0\_DR\_FSLs}$  before switching to pull-down.
  - Upon completion of device Chirp K forwarding, it shall disable its SE transmitter.
- The repeater shall perform the following to forward the K-J chirps from eDSPr:
  - It shall drive Chirp K at D+/D- if it has detected logic '1' at eD-.
  - It shall drive Chirp J at D+/D- if it has detected logic '0' at eD-.
- For a FS capable only host, the repeater may not observe host K-J chirp. Under this situation, it shall maintain eSE0 on both eD+/eD- and D+/D- and expect a FS EOReset from eDSPr. Refer to Section 5.5.10 for timing diagram of Bus Reset with FS Host and HS capable device.

eDSPr shall meet the following conditions.

- It shall enable its SE receiver on eD- for logic '1' device chirp.
- Once device chirp is concluded on eD-, and eDSPr is directed by its host controller, it shall drive logic '1' on eD- for host Chirp K and logic '0' on eD- for host Chirp J.
- In the event that the host controller is only FS capable, eDSPr shall maintain eSE0 on eD+/eD- expecting to end USB 2.0 Bus Reset to FS as directed by its controller. Refer to Section 5.5.10 for Bus Reset of a FS Host timing diagram.

#### 5.3.3.2.2 *Exit from Reset.Chirp*

The repeater shall perform the following:

- The repeater shall transition to Default if it has detected Port Reset.
- The repeater shall enter Reset.EOR in one of the following conditions.
  - After completion of K-J Chirp forwarding and upon detecting HS EOReset.
  - Upon detecting the start of FS/LS EOReset.

eDSPr shall perform the following:

- It shall enter Reset.EOR as directed by UTMI+ to transmit EOReset.

Refer to Sections 5.5.8, 5.5.9, 5.5.10, and 5.5.11 for various timing diagrams of USB 2.0 Bus Reset at different link speeds.

### **5.3.3.3 *Reset.EOR***

Reset.EOR is a substate where the eUSB2 host port concludes USB 2.0 Bus Reset.

#### **5.3.3.3.1 *Reset.EOR Requirement***

The repeater shall meet the following conditions.

- For LS/FS operation, the repeater shall perform the eUSB2 EOReset to USB 2.0 EOReset mapping like the conversion of LS/FS eUSB2 EOP to USB 2.0 EOP. Refer to Section 3.3.4 for details.
- For HS operation, the repeater shall meet the following conditions.
  - It shall drive SE0 at UDSP upon detecting rising edge of eD+.
  - It shall enable its HS transceivers and squelch detectors at its eUSPh and UDSP upon detecting the falling edge of eD+.

eDSPr shall meet the following conditions.

- For LS/FS operation, it shall perform the eUSB2 EOReset as described in Section 3.3.1.
- For HS operation, it shall meet the following conditions.
  - It shall drive logic '1' for  $T_{\text{STROBE}}$  duration on eD+ indicating EOReset.
  - It shall disable its transmitter and maintain eSE0 with its  $R_{\text{PD}}$  upon completing EOReset and enable its HS transceivers and squelch detectors at its eUSB port.

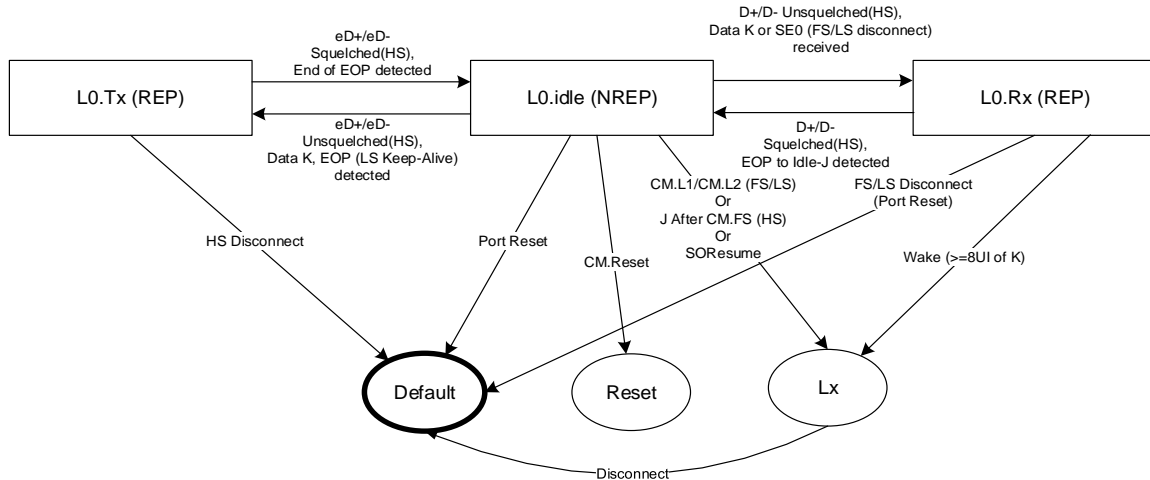
#### **5.3.3.3.2 *Exit from Reset.EOR***

- The repeater shall transition to Default if it has detected Port Reset.  
The repeater and eDSPr shall enter L0 upon completing the EOReset transmission. Note that the repeater shall determine and keep the established HS, FS, or LS link speed based on the Connect and Reset handshake for subsequent L0 HS or FS/LS data forwarding, line mapping, Lx entry, and disconnect detection operations.



### 5.3.4 L0

L0 is a state where the repeater forwards packets between eUSB2 and USB 2.0. L0 contains three substates as shown in Figure 5-8.



**Figure 5-8: L0 Substate Machine**

#### 5.3.4.1 L0.Idle

L0.Idle is a substate where the link is idle. The repeater transitions from this substate to L0.Tx/L0.Rx based on the incoming signals from eUSPh and UDSP. If it's eSE1, it remains in this substate and determines if it's SCM or XeSE1. If it's non eSE1, it implies an incoming packet, Resume or Remote Wake (in the FS/LS case where the repeater stays in L0, but the link is in Lx) that needs to be forwarded.

##### 5.3.4.1.1 L0.Idle Requirements

The repeater shall meet the following conditions.

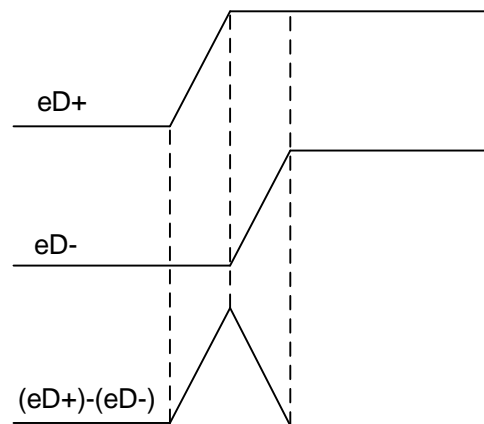
- Its UDSP shall meet the condition defined by USB 2.0.
- eUSPh shall meet the following requirements.
  - It shall enable its SE receivers at eD+/eD-.
  - It shall enable its eSE1 detector for CM.Reset, CM.L1, CM.L2, CM.FS, CM.Test, Port Reset, or SOResume. Note: Scenario could exist in FS/LS operations, where eDSPr may not transmit CM.Lx to the repeater. In this event, the repeater would remain in L0.Idle while eDSPr is in Lx.
  - If HS, it shall enable its squelch detectors on eUSPh and on UDSP.
  - Upon recognizing SCM, it shall remove its HS termination on eUSPh for CM reception.
  - Upon receiving CM.FS in high-speed operation, the repeater shall perform the following:
    - It shall switch to NREP mode.
    - It shall reconfigure to FS termination.
    - It shall maintain eSE0 at eUSPh and monitor the bus state at UUSP. If the bust state at UUSP switches from SE0 to J, it shall transmit a T<sub>STROBE</sub> at eD+.
 Note: this is a transitional state in which the HS link shall eventually enter Lx when a J is detected at UDSP.
  - If CM.Test is received, it shall enable it HS termination for HS Compliance Test. Note: Exiting a Compliance Test condition may be a power cycle or Port Reset depending on Implementation.

eDSPr shall meet the following conditions.

- If HS, it shall enable its squelch detector.
- If directed, it shall issue CM.Reset to start USB 2.0 Bus Reset.
- In HS mode, upon transmitting CM.FS and starting the 4 ms timer for disconnect detection, it shall maintain SE0 at LineState and monitor for  $T_{\text{STROBE}}$  at eDSPr. If  $T_{\text{STROBE}}$  is detected before the 4 ms timer expiration, it shall update the LineState to J, indicating device entering L1. If  $T_{\text{STROBE}}$  is not detected before the 4 ms timer expiration, it shall assert HostDisconnect on its UTMI+ and issue Port Reset to its repeater.

Implementation note:

Due to intra-pair skew defined as  $T_{\text{eSE1\_SKEW}}$  in Table 7-16 between eD+ and eD-, an eSE1, upon reaching eDSPr/eUSPh, may be distorted, as shown Figure 5-9.



**Figure 5-9: SCM Distortion Observed by eUSB2 Repeater**

This distortion may exhibit one of the following false conditions to the eUSB2 repeater:

1. If the rising edge of eD+ precedes the rising edge of eD-, it may initially present itself as the first bit of SYNC in LS operation.
2. If the rising edge of eD- precedes the rising edge of eD+, it may present itself as the first bit of SYNC in FS operation, or a LS keep-alive in LS operation.
3. If either of the above two mentioned conditions occur during HS operation (L0.Idle), it may present itself as a HS K or J that may lead to HS squelch detector exiting from squelched condition.

It is highly recommended for an implementation to apply proper filtering mechanisms to avoid unintended action to those false conditions. Some possible mechanisms include, but are not limited to the following:

1. For FS/LS operation it shall adhere to USB 2.0 FS/LS hub repeater timing, with the exception of next transition jitter from eUSB2 to USB 2.0 and paired transition in both directions. The jitter to next transition follows eUSB2 parameter  $T_{\text{e\_to\_U\_DJ1}}$ , instead of the corresponding USB 2.0 parameter  $T_{\text{HDJ1}}$ .  $T_{\text{HDJ1}}$  still applies to USB 2.0 to eUSB2. The jitter to paired transition follows eUSB2 parameter  $T_{\text{DJ2}}$ , instead of the corresponding USB 2.0 parameter  $T_{\text{HDJ2}}$ .
2. For HS operation, reduce the squelch detector sensitivity to not respond to the short pulse, and have the eSE1 detector disable squelch detector upon declaring eSE1 detection.

The eUSB2 channel construction shall meet the requirements defined in Table 7-6 (Electrical).

#### 5.3.4.1.2 *Exit from L0.Idle*

The repeater shall perform the following tasks.

- It shall transition to L0.Tx if an un-squelched condition (HS) or idle J (LS/FS) to K (logic '1' at eD- for FS or eD+ for LS) or EOP (LS Keep-Alive) transition is detected at eD+/eD-.
- It shall transition to L0.Rx if an un-squelched condition (HS), or an idle J to K (FS/LS) transition, or SE0 (FS/LS device disconnect) is detected at D+/D-.
- It shall transition to Lx if CM.L1 or CM.L2 (Lx.Idle)/SOREsume (Lx.Resume) is received at eUSPh.
- In HS mode, it shall transition to Lx after detecting J at UDSP and having completed sending T<sub>STROBE</sub> to eDSPr. (Note: this is a transitional state in which the HS link shall eventually enter Lx when a J is detected at UDSP) if CM.FS is received for a HS link operation.
- It shall transition to Reset if CM.Reset is received at eD+/eD-.
  - It shall transition to Default if Port Reset is received.

eDSPr shall perform the following tasks.

- It shall transition to L0.Tx if directed by its host to transmit data packet.
- It shall transition to L0.Rx if an un-squelched condition (HS) or an idle J to K transition at eD- (FS) or eD+ (LS) is detected.
- In FS/LS mode, it shall transition to Lx once completing CM.L1/CM.L2 to its repeater, if directed by its host through UTMI+ interface to perform a Lx entry.
- In HS mode, it shall transition to Lx upon detecting T<sub>STROBE</sub> from eUSPh before the 4 ms timer expiration and having updated the LineState to J.
- It shall transition to Reset once completing CM.Reset if directed by its host through UTMI+ interface to perform a USB 2.0 Bus Reset.
- If in FS mode, it shall transition to Default and transmit Port Reset to eUSPh if a logic '1' on eD+ (FS mapping as SE0 on D+/D-) is received and qualified as device disconnect.
- If in LS mode, it shall transition to Default and transmit Port Reset to eUSPh if a logic '1' on eD- (LS mapping as SE0 on D+/D-) is received and qualified as device disconnect.

Section 5.5.4 illustrates the timing flow of detecting FS disconnect and reconnecting.

#### 5.3.4.2 **L0.Rx**

L0.Rx is a substate where a USB packet is received and forwarded from UDSP to eUSPh.

##### 5.3.4.2.1 *L0.Rx Requirements*

The repeater shall meet the following conditions.

- It shall operate at REP mode.
- In HS operation, it shall forward the USB packets upon detection of the un-squelched condition at UDSP. Note: The repeater can consume 4 SYNC bits on the exit from Squelch. While forwarding USB packets from UDSP to eUSPh, the repeater may transmit the 1<sup>st</sup> bit (within the 4 allowable SYNC bits that a repeater can consume) of the SYNC pattern with random UI duration and add EOP dribble up to 5 random (SE0 or K or J) bit duration. Any intermediate dribble value, SE0, K or J, may be any duration, as long as total dribble is within 5 UI.
- In FS/LS operation, it shall perform packet forwarding based on FS/LS mapping described in Section 3.3.1 upon detection of K (including Wake) or SE0 (FS/LS disconnect) condition at UDSP. Note that observing SE0 at UDSP implies potential device disconnect. The repeater does not perform device disconnect detection. It maps SE0 mapping from UDSP to eUSPh as described in Figure 3-6. It is eDSPr's responsibility to perform device disconnect detection.
- In FS/LS operation, it shall implement a Wake timer that is capable of determining the input signal from UDSP if it is the start of a packet or Remote Wake. Note that scenarios

exist where eDSPr may not transmit CM.Lx to the repeater after entering Lx. Under this situation, eDSPr is in Lx while the repeater still remains in L0.Idle. Although a non-ideal configuration with higher power consumption, the link shall remain operational and the repeater in L0.Rx shall be able to use this timer to distinguish between an incoming USB 2.0 packet and Remote Wake K. The mechanism of the Wake timer operation is optional normative. It may be based on, but not limited to one of the the following two methods. Note that for both methods, the min-max range of the timer threshold is defined to accommodate a +/-30% repeater clock frequency and LS UI is specified for both FS and LS operations to cover a scenario when a FS hub is forwarding a packet from a LS device. In this case, the hub UFP operates at FS edge rate and polarity, but with LS unit interval.

- If the Wake timer is only enabled to distinguish Remote Wake K from the first bit of SYNC K, the following operations shall be performed.
  - The Wake timer threshold shall be between 2 LS UI and 4 LS UI.
  - The Wake timer shall start upon detecting data K at UDSP.
  - The Wake timer shall expire if the duration of data K exceeds the timer threshold.
  - The Wake timer shall reset if the duration of data K is less than the timer threshold.
- If the Wake timer is always enabled whenever a data K is detected, including in the middle of the packet, the following operations shall be performed.
  - The Wake timer threshold shall be between 8 LS UI and 16 LS UI. Note that 8 LS UI is specified to consider bit stuffing, where the maximum duration of data K is 7 FS/LS UI.
  - The Wake timer shall start upon detecting data K.
  - The Wake timer shall expire if the duration of data K exceeds the timer threshold.
  - The Wake timer shall reset if the duration of data K is less than the timer threshold.

eDSPr shall meet the following conditions.

- In HS operation, it shall receive differential data packets from eUSPh.
- In HS operation, it shall filter squelch for up to 5 UI to ignore SE0 from the repeater during EOP dribble.
- In FS/LS operation, it shall receive either a data packet, or USB 2.0 SE0 mapping (disconnect) from eUSPh.

#### 5.3.4.2.2 *Exit from L0.Rx*

The repeater shall perform the following tasks.

- In HS operation, it shall transition to L0.Idle upon completion of the packet forwarding, and a squelched condition at UDSP is detected.
- In FS/LS operation, it shall transition to L0.Idle upon completing the packet forwarding, including EOP, and detecting an idle J condition at UDSP.
- In FS/LS operation, it shall transition to Lx (Lx.Wake) if the Wake timer expires.
- it shall transition to Default if Port Reset is detected.

eDSPr shall perform the following tasks.

- In HS operation, it shall transition to L0.Idle upon detecting a squelched condition and the last byte of the packet has been reported over UTMI+.
- In FS/LS operation, it shall transition to L0.Idle upon detecting the end of EOP.

#### 5.3.4.3 **L0.Tx**

L0.Tx is a substate where a USB packet is received and forwarded from eUSPh to UDSP.

#### 5.3.4.3.1 *L0.Tx Requirements*

The repeater shall meet the following conditions.

- It shall operate in REP mode.
- In FS/LS operation, it shall forward packet based on FS/LS mapping respectively as described in Section 3.3.1 upon detection of logic '1' condition (idle J to K) at eUSPh from eDSPr.
- Also, in LS operation, it shall forward LS Keep-Alive, which is a LS EOP, on UDSP as described in Section 3.3.1.
- In HS operation, it shall forward the USB packets based on the following.
  - It shall start forwarding the packet upon detection of the un-squelched condition at eUSPh.
  - It may consume up to 4 SYNC bits for exit from Squelch and the 1<sup>st</sup> bit (within the 4 allowable SYNC bits that a repeater can consume) of the SYNC pattern may be with random UI duration.
  - It may add up to 4 UI of random (K or J) EOP dribble with no SE0. Note that prohibiting SE0 within dribble is to ensure interoperability with legacy USB 2.0 devices.
- In HS operation, it shall enable its high-speed disconnect detector at UDSP and shall adhere to  $T_{\text{DISC\_DLY}}$  in announcing HS disconnect to its associated eDSPr. Refer to Section 5.5.7 that describes the timing flow of host repeater and its associated eDSPr detecting device disconnect in HS link.

Implementation note:

High-Speed disconnect detect in L0 is performed by a downstream port during EOP of  $\mu\text{SOF}$ . It is the responsibility of the repeater to identify the EOP of an  $\mu\text{SOF}$ . A repeater may implement a digital filter based on its local clock to detect the EOP of an  $\mu\text{SOF}$ , and subsequently control the operation of the high-speed disconnect detector. A repeater may sample the disconnect detector output upon detection of the squelched condition at eUSPh.

eDSPr shall meet the following conditions.

- In HS operation, it shall transmit differential data packets to eUSPh.
- In FS/LS operation, it shall transmit SE data packets to eUSPh as described in Section 3.3.1.

#### 5.3.4.3.2 *Exit from L0.Tx*

The repeater shall perform the following tasks.

- The repeater shall transition to Default if it has detected Port Reset.
- The repeater shall transition to L0.Idle if the following conditions are met.
  - It has completed the transmission of the USB packet at its UDSP.
  - It has detected squelched condition at its eUSPh, if it is in HS operation.
  - It has detected EOP as described in Section 3.3.1 at its eUSPh, if it is in FS/LS operation.
- In HS operation, it shall transition to Default if a Device Disconnect Announcement is sent to eDSPr upon detecting USB 2.0 device disconnect.

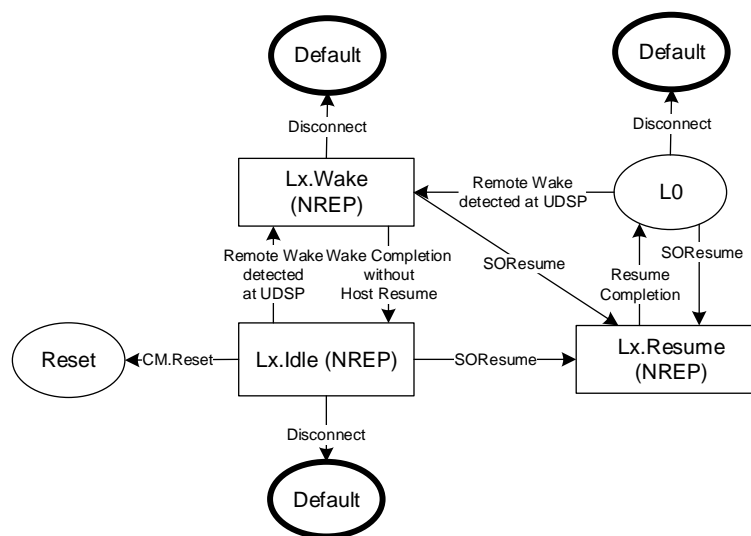
eDSPr shall perform the following tasks.

- It shall transition to L0.Idle if it has completed the transmission of the USB packet.
- In HS operation, it shall declare device disconnect as defined by  $T_{\text{HSDISC\_eSE1}}$  and transition to Default if a Device Disconnect Announcement is received from eUSPh. Note that eDSPr is not recommended to transmit Port Reset after receiving eUSPh Device Disconnect Announcement.

### 5.3.5 Lx

Lx is a state where the repeater is in power saving mode. It may be entered due to receiving CM.Lx or CM.FS. In FS/LS operation, it may also be entered as a transitional state from L0 upon detecting Remote Wake at UDSP, or SOResume at eUSPh. Only CM.Lx receipt would necessarily put it into a power saving mode. The repeater power management may be different between L1 and L2 depending on implementation. Sections 5.5.12 and 5.5.13 show the timing sequence of the FS L1 and L2 entries, while Section 5.5.18 shows the L2 entry of a HS link. Additionally, Sections 5.5.20, 5.5.21, and 5.5.22 illustrate device disconnect detection during Lx entry. The Lx substate machine is shown in Figure 5-10.

- The repeater shall be in NREP mode. Note: As described in Section 5.3.4.1.2 where the repeater in LS/FS operation may stay in L0 (although the link is in Lx), which is in REP mode.



**Figure 5-10: Lx Substate Machine**

#### 5.3.5.1 Lx.Idle

Lx.Idle is a substate where the repeater is in logical low power idle state.

##### 5.3.5.1.1 Lx.Idle Requirements

The repeater shall meet the following conditions.

- It shall be ready for eSE1 detection at eUSPh.
- It shall disable its high-speed transceivers.
- It's UDSP shall meet the requirements defined by USB 2.0.
- It shall not perform device disconnect detection. If SE0 at UDSP is detected, it shall perform SE0 mapping at eUSPh as defined in Table 3-1, and allow eDSPr to perform disconnect detect.

eDSPr shall meet the following conditions.

- It shall monitor the eUSB2 bus state for potential events of Remote Wake or device disconnect.
- It shall disable its high-speed transceivers.

- It shall perform device disconnect detection based on SE0 mapping in Table 3-1 for eUSB2 Bus state mapping.

#### 5.3.5.1.2 *Exit from Lx.Idle*

The repeater shall perform the following tasks.

- It shall transition to Lx.Resume if it has detected Resume at eUSPh.
- It shall enter Lx.Wake if it has detected Remote Wake at UDSP.
- It shall transition to Reset if it has received CM.Reset.
- It shall transition to Default if Port Reset (it could be triggered from eDSPr based on device disconnect or as directed) is detected. Note that eDSPr declares USB 2.0 device disconnect based on repeater mapping the eUSB2 bus state from UDSP to eUSPh.

eDSPr shall perform the following tasks.

- It shall transition to Lx.Resume if directed by its host on the UTMI+ to perform Resume.
- It shall enter Lx.Wake if it has detected Remote Wake from eUSPh.
- It shall transition to CM.Reset if directed by its host on the UTMI+ to perform USB 2.0 Bus Reset.
- It shall transmit Port Reset and transition to Default if it has declared device disconnect, or is directed. Note: Although implementation specific, given the likely window where role swap occurs during Lx, eDSPr shall transmit Port Reset and transition to Default in the event of role swapping where the UTMI+ interface changed from host to peripheral mode. This is then followed by a Repeater Configuration to reconfigure the repeater to peripheral mode operation.

#### 5.3.5.2 *Lx.Resume*

Lx.Resume is a substate where the host starts exiting from L1 or L2. Sections 5.5.125.5.13 show the timing sequence of the FS Resume from L1 and L2, while Section 5.5.17 shows Resume to back to HS.

##### 5.3.5.2.1 *Lx.Resume Requirements*

The repeater shall meet the following conditions.

- It shall monitor the eUSPh Resume until its completion.
- It shall drive the Resume signal at its UDSP defined by USB 2.0 while the eUSB2 Resume signal is asserted.
- It shall end Resume at its UDSP upon detecting EOResume at its eUSPh. Refer to Section 3.3.5 for EOP transmission.

eDSPr shall meet the following conditions.

- In FS/LS Lx, it shall drive Resume as defined in Section 3.3.5.1.2 to its eUSPh when directed by its controller.

##### 5.3.5.2.2 *Exit from Lx.Resume*

The repeater shall perform the following tasks.

- It shall transition to Default if it has detected Port Reset.
- It shall enter L0.Idle upon detecting EOResume from its eDSPr and complete Resume signaling on UDSP.

eDSPr shall perform the following tasks.

- Resuming to FS/LS, it shall transition to L0.Idle upon completing EOResume as defined in Section 3.3.5.1.2 to its repeater.
- Resuming to HS, it shall transition to L0.Idle upon completing EOResume as defined in Section 3.3.5.2.2 to its repeater.

### 5.3.5.3 *Lx.Wake*

Lx.Wake is a substate where a USB 2.0 device initiates Remote Wake to Resume the USB 2.0 operation. Sections 5.5.15 and 5.5.18 show the timing waveform of L2 wake to FS and HS respectively. Additionally, Sections 5.5.16 and 5.5.19 provide timing sequences of a FS and HS wake from L2 without the host Resume being triggered.

#### 5.3.5.3.1 *Lx.Wake Requirements*

The repeater shall meet the following conditions. Refer to Sections 5.5.15 and 5.5.18 for examples.

- It shall perform the Remote Wake from L2 as defined by USB 2.0.
  - Upon detecting Remote Wake at its UDSP, it shall drive Remote Wake at its eUSPh with the delay meeting related USB 2.0 hub timing parameters. If auto-resume is enabled, it shall propagate Remote Wake at eUSPh and Resume at UDSP simultaneously.
  - It shall drive or in the case of auto-resume, continue the Resume signal at its UDSP, upon detecting SOResume at eUSPh.
  - It shall conclude the eUSB2 Remote Wake signal upon detection of SOResume.
  - It shall implement a  $T_{\text{SE0\_FILTER}}$  SE0 filter timer to detect Remote wake without Resume. In case of Remote Wake conclusion without SOResume from eDSPr and auto-resume is not supported, it implies a non-K bus state is observed at UDSP. Under this scenario, it shall maintain Wake K at eD+/eD-, start the  $T_{\text{SE0\_FILTER}}$  SE0 filter timer and perform the bus state mapping from D+/D- to eD+/eD- as defined in Table 3-3. It shall continue the bus state mapping from D+/D- to eD+/eD- as defined in Table 3-3 upon expiration of the  $T_{\text{SE0\_FILTER}}$  SE0 filter timer.
- It shall perform Remote Wake from L1 as defined by USB 2.0 Link Power Management Addendum. The repeater shall do the following.
  - Upon detecting Remote Wake at its UDSP, it shall drive the eUSB2 Remote Wake at its eUSPh. If auto-resume is enabled, it shall propagate Remote Wake at eUSPh and Resume at UDSP simultaneously.
  - It shall drive or in the case of auto-resume, continue the the Resume signal at its UDSP upon detecting SOResume at eUSPh.
  - It shall conclude the eUSB2 Remote Wake signal upon detection of SOResume.

eDSPr shall meet the following conditions.

- It shall reflect Remote Wake received at eD+/eD- to its UTMI+ interface.
- It shall start driving Resume signal as defined in Section 3.3.5 when directed by its host through the UTMI+ interface.

#### 5.3.5.3.2 *Exit from Lx.Wake*

The repeater shall perform the following tasks.

- It shall transition to Lx.Resume upon detecting SOResume at its eUSPh before the End of Remote Wake at UDSP. Note that receiving SOResume implies the reception of eSE1 followed immediately by Resume K.
- It shall transition to Lx.Idle after the  $T_{\text{SE0\_FILTER}}$  SE0 filter timer timeout and the USB 2.0 bus state idle J is detected. Note this condition only applies to the scenario where auto-resume is not supported.
- It shall transition to Default if Port Reset is received on eUSPh.

eDSPr shall perform the following tasks.

- Resuming to FS/LS, it shall transition to Lx.Resume as directed as defined in Section 3.3.5.1.2. Note: A successful Remote Wake shall follow with Resume.

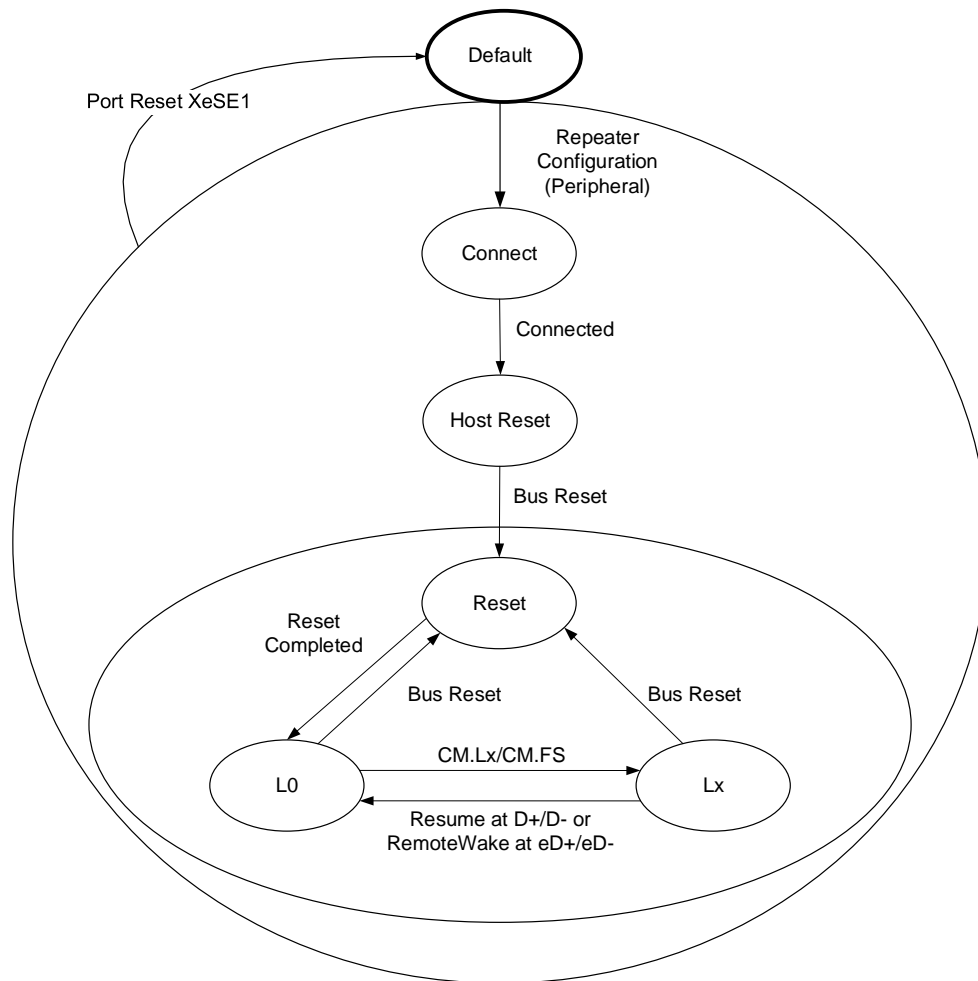


- Resuming to HS, it shall transition to Lx.Resume as directed as defined in Section 3.3.5.2.2. Note: A successful Remote Wake shall follow with Resume.
- It shall transition to Default and transmit Port Reset upon detecting a device disconnect during wake (i.e. a logic '1' on eD+ for FS Lx indicating a SE0 condition at UDSP) or as directed.

## 5.4 Peripheral Repeater Operation

This section describes basic operations of an eUSB2 peripheral repeater associated with eUSPr. The state machine of an eUSB2 repeater in peripheral mode is like host mode but with different transition conditions. The peripheral mode repeater state machine is shown in Figure 5-11.

Note: eUSPr implementation may not have the exact states or state transitions as the repeater. Below diagrams and description serve as an informative guide to eUSPr implementation.

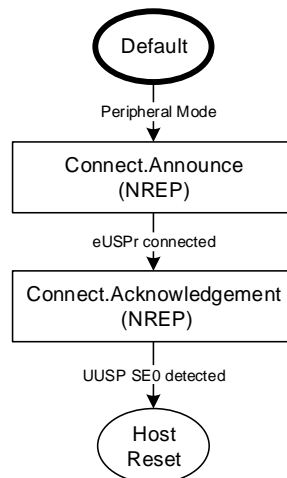


**Figure 5-11: Peripheral Mode eUSB2 State Machine**

### 5.4.1 Connect

Connect is a state where a peripheral repeater is ready for device connect directed by its eUSPr. Section 5.5.2 illustrates a peripheral repeater link initiating a FS connection upon POR. Section 5.5.4 show a peripheral repeater connecting to a host and establishing a HS link upon POR. Note that the repeater's bus state mapping defined in Table 3-1 does not apply in this state. It is applicable only after establishing a connection (exiting Connect.Acknowledge and entering Host Reset).

Connect contains two substates shown in Figure 5-12.



**Figure 5-12: Connect Substate Machine**

#### 5.4.1.1 *Connect.Announce*

Connect.Announce is a substate where eDSPp is expecting device connect from eUSPr.

##### 5.4.1.1.1 *Connect.Announce Requirements*

The repeater shall meet the following conditions.

- eDSPp shall meet the following conditions.
  - It shall enable its R<sub>PD</sub> to maintain eSE0 at eUSB2 bus.
  - It shall enable its SE receivers.
- UUSP shall have its transceivers disabled.

eUSPr shall meet the following conditions.

- It shall enable its R<sub>PD</sub> at both eD+ and eD-.
- It shall, when directed by its device controller, drive logic '1' at eD+ to instruct its repeater to pull-up at D+.
- It shall, when directed by its device controller, drive logic '1' at eD- to instruct its repeater to pull-up at D-.

##### 5.4.1.1.2 *Exit from Connect.Announce*

The repeater shall perform the following tasks.

- It shall transition to Default if it has detected Port Reset.
- It shall transition to Connect.Acknowledge if one of the following conditions is met.
  - It has enabled FS transceiver at UUSP with D+ pull-up upon detecting logic '1' at eD+ for FS/HS operation.
  - It has enabled LS transceiver at UUSP with D- pull-up upon detecting logic '1' at eD- for LS operation.

eUSPr shall perform following tasks.

- It shall send Port Reset and transition to Default as directed.
- It shall transition to Connect.Acknowledge if one of the following conditions is met.
  - It has detected logic '1' at eD- for FS/HS operation.
  - It has detected logic '1' at eD+ for LS operation.

#### **5.4.1.2 Connect.Acknowledge**

Connect.Acknowledge is a substate where the repeater is relaying device connect from its eDSPp to UUSP, and acknowledging the connect completion to eUSPr.

##### **5.4.1.2.1 Connect.Acknowledge Requirements**

The repeater shall meet the following conditions.

- It shall acknowledge the connect completion to eUSPr by performing the following.
  - It shall drive logic '1' at eD-, upon completing the FS transceiver configuration at UUSP with D+ pull-up and after observing logic '1' at D+ that is a result of the pull-up.
  - It shall drive logic '1' at eD+, upon completing the LS transceiver configuration at UUSP with D- pull-up and after observing logic '1' at D- that is a result of the pull-up.
- It is not required to perform debounce or de-glitching on the USB 2.0 bus. Note that this requirement shall apply to the peripheral repeater in any of the ensuing states.
- It shall complete the connect acknowledgement to eUSPr by performing the following.
  - It shall drive and maintain logic '0' at eD-, upon detecting logic '0' at eD+ indicating eUSPr concluding the connect announcement. Note that the repeater shall maintain the FS transceiver configuration at UUSP with D+ pull-up throughout this substate.
  - It shall drive and maintain logic '0' at eD+, upon detecting logic '0' at eD- indicating eUSPr concluding the connect announcement. Note that the repeater shall maintain the LS transceiver configuration at UUSP with D- pull-up throughout this substate.

eUSPr shall meet the following conditions.

- It shall conclude the connect announcement by performing the following.
  - It shall drive logic '0' at eD+ if it has detected the connect acknowledgment at eD- from the repeater and disable its SE transmitter.
  - It shall drive logic '0' at eD- if it has detected the connect acknowledgment at eD+ from the repeater and disable its SE transmitter.
- It shall monitor the conclusion of the connect acknowledgement from the repeater.

##### **5.4.1.2.2 Exit from Connect.Acknowledge**

- The repeater shall transition to Default if it has detected Port Reset.
- The repeater shall transition to Host Reset upon completing the connect acknowledgement. Refer to Section 5.5.2 timing diagram for details of the operation.
- eUSPr shall transition to Host Reset upon concluding the connect announcement. Refer to Section 5.5.2 timing diagram for details of the operation.

#### **5.4.2 Host Reset**

In the Host Reset state, the repeater monitors its UUSP for SE0 indicating USB 2.0 Bus Reset. Sections 5.5.2, 5.5.3, and 5.5.4 describe the reset flow for a LS, FS and HS connection respectively.

##### **5.4.2.1 Host Reset Requirements**

The repeater shall meet the following conditions.

- It shall monitor the bus state at UUSP and eDSPp.

In FS/LS operation, it shall perform the bus state mapping as defined in

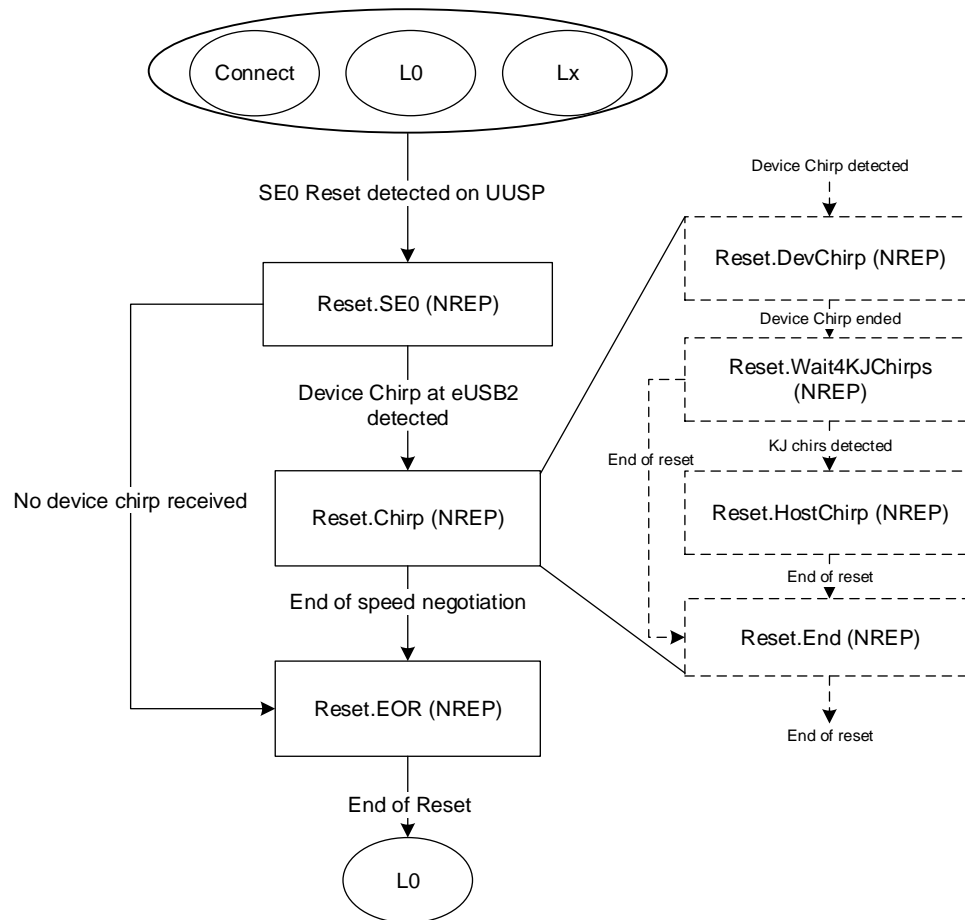
- Table 3-1. Refer to Section 5.5.8 for FS link reset timing diagram.

##### **5.4.2.2 Exit from Host Reset**

- The repeater shall transition to Default if it has detected Port Reset.
- The repeater shall transition to Reset upon SE0 detection at UUSP.
- eUSPr shall transition to Reset upon SE0 indication from repeater according to mapping in Table 3-1.

### 5.4.3 Reset

Reset is a state where host port performs the USB 2.0 Bus Reset and speed detection. Reset contains multiple substates as shown in Figure 5-13.



**Figure 5-13: Reset Substate Machine**

#### 5.4.3.1 Reset.SE0

Reset.SE0 is a substate where the repeater performs a USB 2.0 Bus Reset and prepares for speed negotiation.

##### 5.4.3.1.1 Reset.SE0 Requirements

The repeater shall meet the following conditions.

- If entry to Reset is from HS L0 idle, and the bus state at UUSP remains SE0 after the repeater has D+ pull-up enabled and HS termination disabled at UUSP in response to CM.FS, it shall maintain eSE0 (not pulse/acknowledge on eD+) at eD+/eD- with R<sub>PD</sub>, in preparation for Reset.Chirp or Reset.EOR (in the event that host or device decided to downgrade a previously established HS link, in which case either device chirp or host KJ chirp is not transmitted, eDSPp shall transmit EOReset upon observing a SE0 to J transition on UUSP). Refer to Sections 5.5.8, 5.5.9, 5.5.10, and 5.5.11 for detailed timing diagram.
- If entry to Reset is from FS/LS Connect, L0 or Lx, it shall continue the bus state mapping from UUSP to eDSPp based on LS/FS bus state mapping defined in
- Table 3-1. Note that a repeater may not receive CM.L1 or CM.L2 from eUSPr even when the link is in L1 or L2. Under this situation, a repeater will remain in L0. It may implement

a timer to differentiate and track SE0 of USB 2.0 Bus Reset from SE0 within a data packet including LS keep-alive, to stay in-sync with eUSPr. Refer to Section 5.5.8 for Bus Reset during FS Link.

eUSPr shall meet the following conditions.

- In a FS/LS link, it shall perform the bus state mapping as defined in Table 3-1
- In an established HS link, it shall expect eSE0 at eUSB2 bus (not observing a pulse/acknowledge on eD+) after transmitting CM.FS indicating USB 2.0 Bus Reset (Note: eDSPp shall transmit a pulse/acknowledge on eD+ within  $T_{PR\_RESET\_FROM\_HS}$  for Lx entry). Refer to Section 5.5.9 for timing diagram.

#### 5.4.3.1.2 *Exit from Reset.SE0*

The repeater shall perform the following tasks.

- It shall transition to Default if it has detected Port Reset.
- It shall transition to Reset.Chirp if device chirp is detected at its eDSPp.
- It shall transition to Reset.EOR if it has detected data J at its UUSP.

eUSPr shall perform the following tasks:

- It shall transition to Reset.Chirp and transmit a logic '1' on eD- when directed to start HS negotiation.
- It shall transition to Reset.EOR if it has detected EOReset from eDSPp for a FS/LS link.

### 5.4.3.2 **Reset.Chirp**

Reset.Chirp is a substate where a high-speed eUSB2 device is connected, and the speed negotiation is performed. Section 5.5.4 shows the timing waveform of the reset chirp sequence. There are multiple stages of operation within Reset.Chirp to complete the speed negotiation, as shown in Figure 5-13.

#### 5.4.3.2.1 *Reset.Chirp Requirements*

The repeater shall meet the following conditions.

- eDSPp of the repeater shall be ready for speed negotiation by having its SE receivers enabled.
- The USB 2.0 port shall enable its HS transceiver to forward device chirp K and host KJ chirp acknowledgment.
- It shall stop transmitting logic '1' on eD+ to conclude SE0 bus state mapping from UUSP to eDSPp upon detecting device chirp at eD-.
- It shall forward the eUSB2 device chirp based on the following:
  - It shall drive a chirp K at UUSP if eD- is logic '1'.
  - It shall conclude chirp K at UUSP if eD- is logic '0'.
- It shall perform the following to forward the K-J chirps from the host.
  - It shall drive logic '1' at eD- if it has detected a Chirp K at D+/D-.
  - It shall drive logic '0' at eD- if it has detected a Chirp J at D+/D-.
- In the event where the device started HS negotiation, but Host does not perform chirp KJ (e.g. a FS capable only or downgraded HS Host), the peripheral repeater shall differentiate them in an implementation specific way through the reset sequences and enter Reset.EOR accordingly. Refer to Section 5.5.10 for Bus Reset of a FS Host timing diagram.
- It shall enable its HS receiver termination at UUSP if it has detected a pulse at eD+. Note that this is a pulse sent by eUSPr to inform the peripheral repeater to turn on its HS device termination at UUSP. If HS termination is not enabled by the eUSPr, the repeater shall maintain FS terminations at the end of reset.
- When SE0 is detected after Host KJ chirps (not SE0 after Device chirp), it shall conclude speed negotiation by performing Reset.EOR as described in Section 3.3.4.

- Upon successful completion of high-speed negotiation, which is defined as having HS receiver termination enable from eUSPr during host KJ chirps, it shall be ready for HS operation.

eUSPr shall meet the following conditions.

- It shall transmit logic '1' on eD- as directed by its device controller for device chirp.
- It shall return the eUSB2 bus to eSE0 by driving logic '0' at eD- for  $T_{eSE0\_DR\_LSFS}$  before disabling its TX (eSE0 maintained by  $R_{PD}$ ) upon completion of device chirp.
- It shall map logic '1' and logic '0' toggling at eD- as the host K-J chirp respectively and reflect these to its UTMI+ interface to the device controller. Note: eUSPr may observe continuous eSE0 if the host doesn't transmit chirp. Refer to Section 5.5.10 for Bus Reset of a FS Host timing diagram.
- In the event where the device started HS negotiation, but Host does not perform chirp K-J (e.g. a FS capable only or downgraded HS Host), it shall transition to Reset.EOR upon detecting a logic '1' at eD+ as EOReset. Refer to Section 5.5.10 for Bus Reset of a FS Host timing diagram.
- It shall pulse eD+ as directed by its device controller to instruct the repeater to enable HS termination. Refer to Section 5.5.4 for timing diagram.

#### 5.4.3.2.2 *Exit from Reset.Chirp*

The repeater shall perform the following tasks.

- It shall transition to Default if it has detected Port Reset.
- It shall transition to Reset.EOR if either one of the following conditions is met.
  - SE0 after host KJ chirps is detected at UUSP.
  - FS J is detected at UUSP following SE0 after device chirp but without host KJ chirps.

eUSPr shall perform the following tasks.

- It shall transition to Reset.EOR if a logic '1' is observed at eD+ as EOReset.

#### 5.4.3.3 **Reset.EOR**

Reset.EOR is a substate where the USB 2.0 Bus Reset is concluded. Reset.EOR does not contain any substate.

##### 5.4.3.3.1 *Reset.EOR Requirement*

The repeater shall meet the following conditions.

- In LS/FS operations, it shall stop transmitting logic '1' at eD-/eD+ to end USB 2.0 Bus Reset.
- If a successful HS negotiation is achieved prior to entry of the sub-state, it shall perform the following actions.
  - It shall drive logic '1' at eD+ for  $T_{STROBE}$  to conclude speed negotiation and USB 2.0 Bus Reset, upon SE0 detection at UUSP.
  - It shall then enable its HS transceivers and squelch detectors at its eDSPp and UUSP at the falling edge of eD+.
- If a successful HS negotiation is not achieved prior to entry of the sub-state, it shall transmit FS Reset.EOR for  $T_{STROBE}$  accordingly. Refer to Section 5.5.10 for Bus Reset of a FS Host timing diagram.
- It shall enter L0 upon completion of EOReset transmission.
- It shall determine and keep the established HS, FS, or LS link state based on the Connect and Reset handshake for subsequent L0 HS or FS/LS operation, bus state mapping, and Lx entry.

eUSPr shall meet the following conditions.

- It shall reflect a logic '1' on eD+ to the UTMI+ as an EOReset and L0 entry for FS and HS.

- It shall reflect a logic '1' on eD- to the UTMI+ as an EOReset and L0 entry for LS.

#### 5.4.3.3.2 Exit from Reset.EOR

- The repeater shall transition to Default if it has detected Port Reset.
- The repeater and eUSPr shall transition to L0 upon completion of the EOReset transmission at eUSB2 port.

### 5.4.4 L0

L0 is a state where the repeater is forwarding the USB packets between eDSPp and UUSP. For a peripheral repeater, L0.Tx refers to packets forwarding from UUSP to eDSPp, and L0.Rx refers to packets forwarding from eDSPp to UUSP. Note that for eUSPr, L0.Tx refers to receiving a packet from host, and L0.Rx refers to transmitting a packet to host. L0 contains three substates as shown in Figure 5-14.

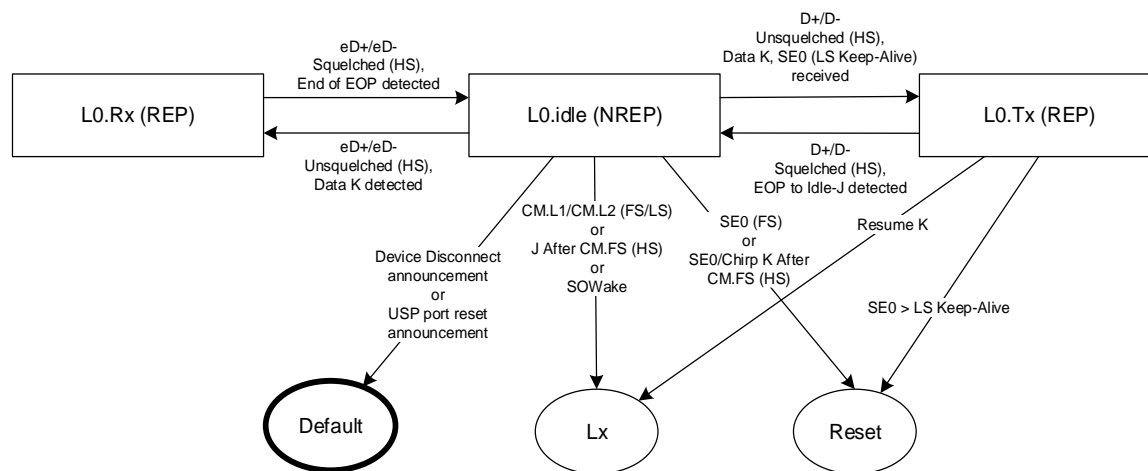


Figure 5-14: L0 Substate Machine

#### 5.4.4.1 L0.Idle

L0.Idle is a substate where the link is idle expecting upcoming events at UUSP and eDSPp.

##### 5.4.4.1.1 L0.Idle Requirements

The repeater shall perform the following tasks.

- Its UUSP shall meet the requirements defined by USB 2.0 specification and be ready to detect input activity for a data packet, SE0 for LS keep-alive or USB 2.0 Bus Reset, and additionally in FS/LS operations, potential Resume K.
- Its eDSPp shall ready to detect input activities such as a data packet, a CM, XeSE1, and additionally potential Remote Wake in FS/LS operations.
- If in HS operation, it shall enable its squelch detectors on both ports.
- Upon detecting SCM, it shall remove its HS termination on eDSPp to enable CM reception.
- Upon receiving CM.FS in high-speed operation, the repeater shall perform the following:
  - It shall switch to NREP mode.
  - It shall configure eDSPp to FS, and enable HS transceiver at UUSP with HS termination disabled. It shall also enable D+ pullup at UUSP.
  - It shall start a  $T_{PR\_RESET\_FROM\_HS}$  timer to differentiate L2 or USB 2.0 Bus Reset by monitoring the bus state at D+/D-. Refer to Sections 5.5.9 and 5.5.17 for timing diagram.
  - It shall continue mapping SE0 at UUSP to eDSPp with eSE0 maintained through Rpd and switch to FS Bus state mapping after idle J is observed at D+/D-.



eUSPr shall meet the following conditions.

- it shall monitor the input status for a data packet, SE0 mapping for LS keep-alive or USB 2.0 Bus reset, and additionally in FS/LS operations, potential Resume K.
- If in HS operation, it shall enable the squelch detector.

#### 5.4.4.1.2 *Exit from L0.Idle*

The repeater shall perform the following transitions.

- It shall transition to Default if it has detected Port Reset.
- It shall transition to L0.Rx if one of the following conditions is met.
  - A high-speed un-squelched condition is detected at eDSPp.
  - A LS/FS data K is detected at eDSPp.
- It shall transition to L0.Tx if one of the following conditions is met.
  - A high-speed un-squelched condition is detected at UUSP.
  - A LS/FS data K, or host Resume K is detected at UUSP.
- It shall transition to Lx if one of the following conditions is met.
  - In an established HS link upon receiving CM.FS and having completed the following actions.
    - It has reverted to FS termination, started a  $T_{PR\_RESET\_FROM\_HS}$  timer and observed idle J at its UUSP before timer expiration.
    - Upon idle J detection, it has reset the timer and transmitted a  $T_{STROBE}$  wide pulse.
  - In an established FS/LS link upon meeting any one of the following conditions.
    - It has received CM.L1/CM.L2 at eDSPp.
    - It has detected SOWake (transition to Lx.Wake) at eDSPp.
- In HS operation, it shall transition to Reset if either one of the following conditions is met. Refer to Section 5.4.3 for details.
  - CM.FS is received and SE0 at UUSP remains unchanged upon the  $T_{PR\_RESET\_FROM\_HS}$  timer expiration.
  - Device Chirp K is detected at eDSPp after switching to FS.
- In FS operation, it shall transition to Reset if it has detected SE0 at UUSP. Note: During a mechanical connect event where UUSP may experience toggling, repeater may be transitioning between Reset and L0.Idle.
- In LS operation, it shall transition to L0.Tx if it has detected SE0 (LS Keep-Alive or USB 2.0 Bus Reset) at UUSP.

eUSPr shall perform the following transitions.

- It shall transition to L0.Rx if directed by its device controller to transmit a data packet or device chirp.
- It shall transition to L0.Tx when an un-squelched (HS) or logic '1' on eD-/eD+ (FS/LS) condition is detected.
- In FS/LS operations, it shall transition to L1/L2 once completing CM.Lx to its repeater, if directed by its controller through UTMI+ interface to perform a Lx entry.
- In HS operation, when directed by its controller through UTMI+ interface to enter FS mode, it shall transition to FS after completing CM.FS to its repeater and having received a pulse as an indication of idle J at its repeater's UUSP.
- In HS operation, when directed by its controller through UTMI+ interface to enter FS mode, it shall transition to Reset once completing CM.FS to its repeater and having not received  $T_{STROBE}$  wide pulse indicating an idle J condition at its repeater's UUSP, upon  $T_{PR\_RESET\_FROM\_HS}$  timer expiration.

#### 5.4.4.2 *L0.Tx*

L0.Tx is a substate for a peripheral repeater where a USB 2.0 packet is received from UUSP and forwarded directly to eDSPp. It is also a substate for eUSPr, where a USB 2.0 packet is received.

#### 5.4.4.2.1 L0.Tx Requirements

The repeater shall meet the following conditions.

- It shall operate in REP mode.
- It shall forward the USB 2.0 packets until HS a high-speed squelch condition or a FS/LS EOP is detected at UUSP. Note: The repeater can consume 4 SYNC bits on the exit from Squelch. While forwarding USB packets from UUSP to eDSPp, the repeater may transmit the 1<sup>st</sup> bit (within the 4 allowable SYNC bits that a repeater can consume) of the SYNC pattern with random UI duration and add EOP dribble up to 5 random (SE0 or K or J) bit duration.
- In FS/LS operation, it shall implement a Resume timer that is capable of determining if the input signal from UUSP is the start of a packet or Resume. Note that scenarios exist where eUSPr may not transmit CM.Lx to the repeater after entering Lx. Under this situation, eUSPr is in Lx while the repeater still remains in L0.Idle. Although a non-ideal configuration with higher power consumption, the link shall remain operational and the repeater in L0.Tx shall be able to use this timer to distinguish between an incoming USB 2.0 packet and Resume K. The mechanism of the Resume timer operation is implementation specific. It may be based on, but not limited to one of the following two methods.
  - If the Resume timer is only enabled to distinguish Resume K from the first bit of SYNC K, the following operations shall be performed.
    - The Resume timer threshold shall be between 2 LS UI and 4 LS UI. Note that 2 LS UI minimum value is specified to be identical with the host mode Wake timer for ease of implementation. In FS operation, the minimum timer threshold could be 2 FS UI, since a peripheral repeater will always receive a FS Preamble packet before a LS packet.
    - The Resume timer shall start upon detecting data K at UUSP.
    - The Resume timer shall expire if the duration of data K exceeds the timer threshold.
    - The Resume timer shall reset if the duration of data K is less than the timer threshold.
  - If the Resume timer is always enabled when a data K is detected, the following operations shall be performed.
    - The Resume timer threshold shall be between 8 LS UI and 16 LS UI. Note that for both methods, LS UI is specified for both FS and LS operations to cover the scenario of a FS hub repeating a Preamble packet meant for a LS device. In this case, the hub DFP operates at FS edge rate and polarity, but with LS unit interval after the Preamble packet. Note also that minimum of 8 LS UI is specified to consider bit stuffing, where the maximum duration of data K is 7 FS/LS UI.
    - The Resume timer shall start upon detecting data K.
    - The Resume timer shall expire if the duration of data K exceeds the timer threshold.
    - The Resume timer shall be reset if the duration of data K is less than the timer threshold.

eUSPr (in Rx) shall meet the following conditions.

- In HS operation, it shall be receiving differential data packets from eDSPp.
- In HS operation, it shall filter squelch for up to 5 UI to ignore SE0 from the repeater during EOP dribble.
- In FS/LS operation, it shall be receiving SE data packets from eDSPp.

#### 5.4.4.2.2 Exit from L0.Tx

The repeater shall perform the following tasks.

- It shall transition to Default if it has detected Port Reset.

- It shall transition to L0.Idle upon detection of a squelch condition or detection of SE0 for EOP followed by idle J at UUSP and the USB 2.0 packet forwarding at eDSPp is completed.
- It shall transition to Reset if SE0 exceeded duration for LS Keep-Alive or link is FS.
- It shall transition to Lx (Lx.Resume) if the Resume timer expires.

eUSPr shall perform the following tasks.

- In HS operation, it shall transition to L0.Idle upon detecting a squelched condition at eUSPr and the last byte of the packet has been reported over UTMI+.
- In FS/LS operations, it shall transition to L0.Idle upon detecting the end of EOP at eUSPr.

#### **5.4.4.3 L0.Rx**

L0.Rx is a substate for a peripheral repeater, where a USB 2.0 packet is received from eDSPp and forwarded directly to UUSP. It is also a substate for eUSPr, where a USB 2.0 packet is transmitted.

##### **5.4.4.3.1 L0.Rx Requirements**

The repeater shall meet the following conditions.

- It shall operate at REP mode.
- It shall forward the HS USB 2.0 packets based on the following.
  - It shall start forwarding the packet upon detecting the un-squelched condition at eDSPp.
  - It may consume up to 4 SYNC bits for exit from squelch and the 1<sup>st</sup> bit (within the 4 allowable SYNC bits that a repeater can consume) of the SYNC pattern may be with random UI duration.
  - It may add up to 4 UI of random (K or J) EOP dribble with no SE0. Note that prohibiting SE0 within dribble is to ensure interoperability with legacy USB 2.0 devices.
- It shall forward the FS or LS USB 2.0 packets based on mapping defined in Table 3-1, including eUSB2 EOP.

eUSPr (in Tx) shall meet the following conditions.

- In HS operation, it shall be transmitting differential data packets to eDSPp.
- In FS/LS operations, it shall be transmitting data packets including EOP to eDSPp as described in Section 3.3.1.

##### **5.4.4.3.2 Exit from L0.Rx**

The repeater shall perform the following tasks.

- It shall transition to Default if it has detected Port Reset.
- It shall transition to L0.Idle if the following conditions are met.
  - It has completed the transmission of USB 2.0 packet including EOP at D+/D-.
  - It has detected a squelched condition or EOP at eD+/eD-.

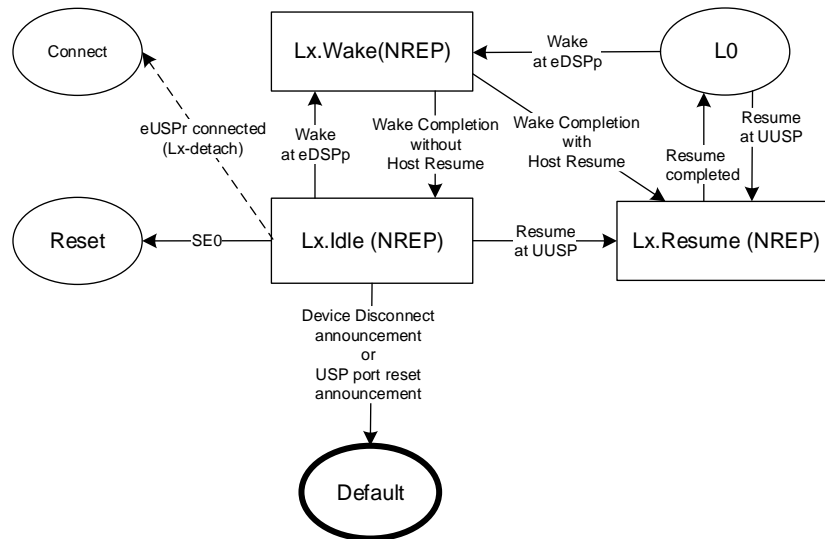
eUSPr (in Tx) shall perform the following tasks.

- eUSPr shall transition to L0.Idle if it has completed the transmission of the USB packet at its eUSB2 interface.

#### **5.4.5 Lx**

Lx is a state where the repeater is in power saving mode. The repeater power management maybe different between L1 and L2, but there is no difference with respect to the operation and mechanism of repeater state transition. Sections 5.5.12 and 5.5.13 show the timing sequence of the FS L1 and L2 entry, while Section 5.5.17 shows the L2 entry of a HS link. Lx substate machine is shown in Figure 5-15.

- The repeater shall be in NREP mode in all sub-states.



### Figure 5-15: Lx Substate Machine

#### 5.4.5.1 *Lx.Idle*

Lx.Idle is a substate where the repeater is in low power idle state.

#### 5.4.5.1.1 *Lx.Idle Requirements*

The repeater shall meet the following requirements.

- It shall maintain eSE0 at eDSPp by enabling its R<sub>PD</sub> at eD+/eD-.
- It shall disable its high-speed transceivers.
- The USB 2.0 port of the repeater shall meet the requirements defined by USB 2.0.

eUSPr shall meet the following conditions.

- It shall be ready for Resume from eDSPp and Remote Wake directed by its controller.
- It shall disable its high-speed transceivers.

#### 5.4.5.1.2 *Exit from Lx.Idle*

The repeater performs the following tasks.

- It shall transition to Lx.Resume if it has detected Resume at UUSP.
- It shall transition to Lx.Wake if it has detected Remote Wake at eDSPp.
- It shall transition to Default if Port Reset is received.
- It shall transition to Reset if SE0 is detected at UUSP.

eUSPr perform the following tasks.

- It shall transition to Lx.Wake when directed to transmit Remote Wake.
- It shall enter Lx.Resume if it has detected host Resume from the repeater, which it reports through UTMI+ LineState.
- It shall transition to Reset if it has detected SE0 mapping on eD+/eD- as USB 2.0 Bus Reset. Note: USB 2.0 Bus Reset is not permitted by USB 2.0 if Remote Wake is enabled. Hence, Wake and Bus Reset will not coincide.
- It shall transmit Port Reset if directed by its controller to perform a soft disconnect or role swap. Note: Although implementation specific, given the possible window where role swap occurs during Lx, eUSPr shall transmit Port Reset and transition to Default in the

event of role swapping where the UTMI+ interface changed from peripheral to host mode. This is then followed by Repeater Configuration to reconfigure the repeater to host mode operation.

#### **5.4.5.2 Lx.Resume**

Lx.Resume is a substate where the host starts exiting from L1 or L2.

##### **5.4.5.2.1 Lx.Resume Requirements**

The repeater shall meet the following conditions.

- It shall monitor the Resume at UUSP, and drive the eUSB2 Resume at eDSPp as defined in Sections 5.5.12 and 5.5.13 for FS Resume from L1 and L2 respectively, Section 5.5.17 for HS Resume from L2, until its completion.
- It shall end Resume at its eDSPp upon detecting EOResume at its UUSP. Refer to Section 3.3.5 for EOResume transmission.

eUSPr shall meet the following conditions.

- It shall reflect Resume to its UTMI+ interface indicating host Resume.
- Upon detecting EOResume, it shall reflect EOResume to its UTMI+ interface.

##### **5.4.5.2.2 Exit from Lx.Resume**

- The repeater and eUSPr shall transition to L0 upon completion of Resume.

#### **5.4.5.3 Lx.Wake**

Lx.Wake is a substate where an eUSB2 peripheral device initiates Remote Wake to Resume the USB traffic. Sections 5.5.12, 5.5.15, and 5.5.18 show the timing waveform of L2 wake to FS and HS respectively. Additionally, Sections 5.5.16 and 5.5.19 provide timing sequences of a FS and HS wake from L2 without the host Resume being triggered.

##### **5.4.5.3.1 Lx.Wake Requirements**

The repeater shall meet the following conditions.

- It shall follow the eUSB2 Remote Wake protocol as defined in Section 3.3.7 and illustrated in Sections 5.5.15 and 5.5.18.
- Its UUSP shall perform Remote Wake defined by USB 2.0 specification.
- It shall drive Remote Wake at UUSP until End of Wake is detected. Note that delay in repeater forwarding Remote Wake shall meet the related USB 2.0 hub timing requirement.
- While driving Remote Wake at UUSP, it shall reflect the bus state from UUSP onto eUSPr as defined in
- Table 3-1. Note that USB 2.0 Bus Reset will not be issued if Remote Wake is enabled. Refer to Section 10.5.4.5 of the USB 2.0 specification for details.
- Upon detecting EOWake (as defined in Section 3.3.6), the repeater shall perform the following.
  - It shall stop driving Remote Wake at UUSP and start the  $T_{\text{SE0\_FILTER}}$  SE0 filter timer.
  - It shall monitor the bus state at UUSP and map it from UUSP to eDSPp as defined in Table 3-3 before and after the expiration of the  $T_{\text{SE0\_FILTER}}$  SE0 filter timer.
  - With host Resume seen on UUSP, it shall continue to map Resume K on UUSP as defined in Section 3.3.5 until the end of host Resume.

eUSPr shall meet the following conditions.

- In FS/LS operations, it shall drive Remote Wake as defined in Section 3.3.6.1.2 at eD+/eD- when directed by its controller.
- It may continue to observe K on eD- beyond the completion of EOWake, even if host Resume is not returned after wake. In this scenario, it shall observe a K to Idle J transition which it shall not declare as host Resume. Host Resume shall be declared as K to SE0 for EOResume.

#### 5.4.5.3.2 *Exit from Lx.Wake*

The repeater shall perform the following tasks.

- It shall transition to Default if it has detected Port Reset.
- It shall transition to Lx.Resume upon completion of wake and having detected a Resume K at UUSP. Note: A successful Remote Wake shall be concluded with host Resume.
- It shall transition to Lx.Idle after the  $T_{SE0\_FILTER}$  SE0 filter timer timeout and the USB 2.0 bus state idle J is detected. Refer to Sections 5.5.16 and 5.5.19 for Remote Wake without Resume.

eUSPr shall perform the following tasks.

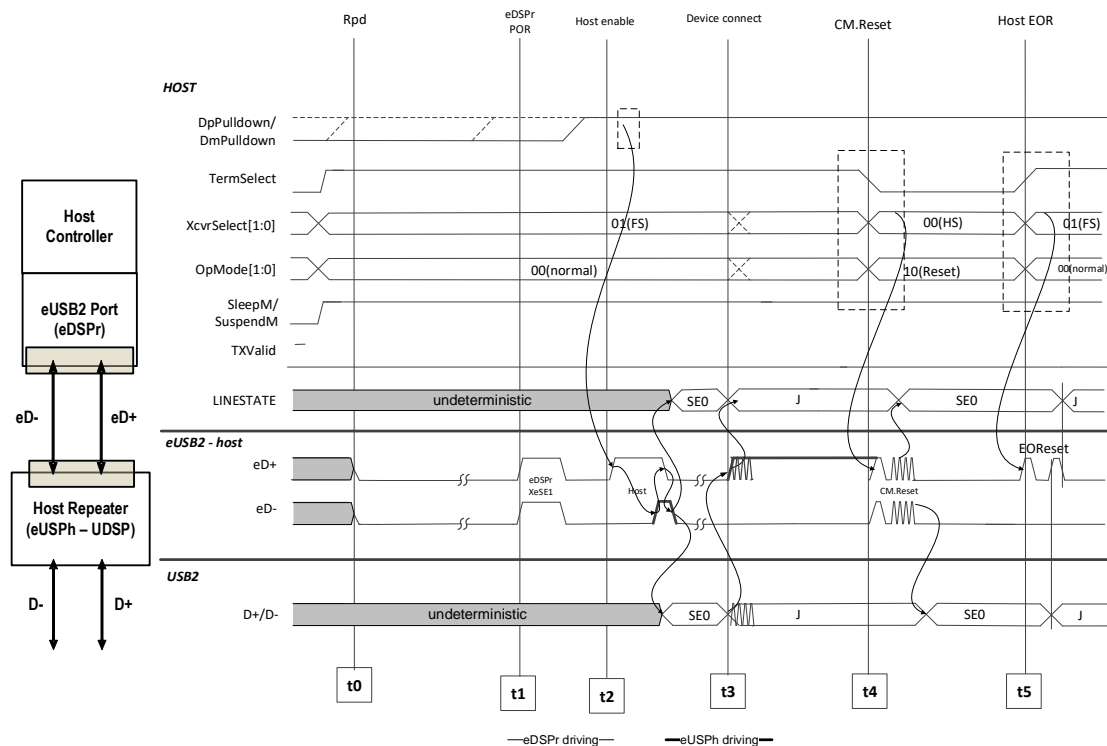
- It shall transition to Lx.Resume upon completion of wake and having detected a Resume K at eD+/eD-. Note: A successful Remote Wake shall be concluded with host Resume.

## 5.5 ***Host-Peripheral Repeater Mode Link Operation***

This section illustrates the various Host-Peripheral repeater mode link operation.

### 5.5.1 **Host Mode Repeater POR and Configuration**

Figure 5-16 shows the timing diagram of a host mode repeater sequencing through Port Reset, Default, Connect, Reset and L0.



**Figure 5-16: Host Mode Repeater Configuration**

- t0:
- eSE0 maintained with Rpd by both eDSPr and eUSPh.
- t1:
- eDSPr transmits XeSE1 as Port Reset. Note: the host repeater may not be powered up. Port Reset may be missed.
  - Note that, eDSPr shall ensure an idle (eSE0) time of  $T_{\text{CONFIG\_IDLE}}$  after transmitting XeSE1 and Repeater Configuration.
- t2:
- eDSPr transmits Repeater Configuration with logic '1' on eD+, to its associated repeater for host mode operation. Note: UTMI+ pulldown indicating host mode operation may have been stable or static at time zero. Transmission of Repeater Configuration shall not depend on a change on UTMI+ pulldown. This is implementation specific on when to transmit this announcement where eDSPr/eUSPr may sample the UTMI+ pulldown state upon completion of XeSE1. If UTMI+ pulldown indicator changes after or in the middle of transmitting Repeater Configuration, eDSPr and eUSPr shall transmit XeSE1 as Port Reset, follow by Repeater Configuration to re-configure its repeater.
  - eUSPh acknowledge eDSPr Repeater Configuration upon POR. Note: eUSPh POR is asynchronous to eDSPr. If eDSPr coming out from POR prior to eUSPh, eDSPr shall transmit Port Reset announcement follow by Repeater Configuration and monitor for eUSPh acknowledgement. On the other hand, if eUSPh comes out of POR first, it shall stay in default pending eDSPr Port Reset and Repeater Configuration.
  - Note that, depending on behavioral requirement of the host controller implementations, LineState mapping may or may not become valid until the repeater configuration is completed. Some host controller may require LineState to be default at SE0 before the repeater configuration.
- t3:

- Device connect with Pullup-J on D+/D-. Note that device may start connect much earlier with valid VBus.
- Host repeater transmits logic '1' on eD+ to eDSPr to announce device connect.
- Note that USB 2.0 D+/D- is shown experiencing a signaling bounce. These bounces are mapped to the eUSB2 bus as defined in Section 5.3.1.

t4:

- CM.Reset from eDSPr. Note: Depending on implementation, UTMI+ xcvrselect and opmode may not change together with UTMI+ termselect. UTMI+ termselect may be the sole trigger for CM.Reset.
- eUSPh drops logic '1' on eD+ and declare a FS (or HS depending on chirp handshake during USB 2.0 Bus Reset) connection.

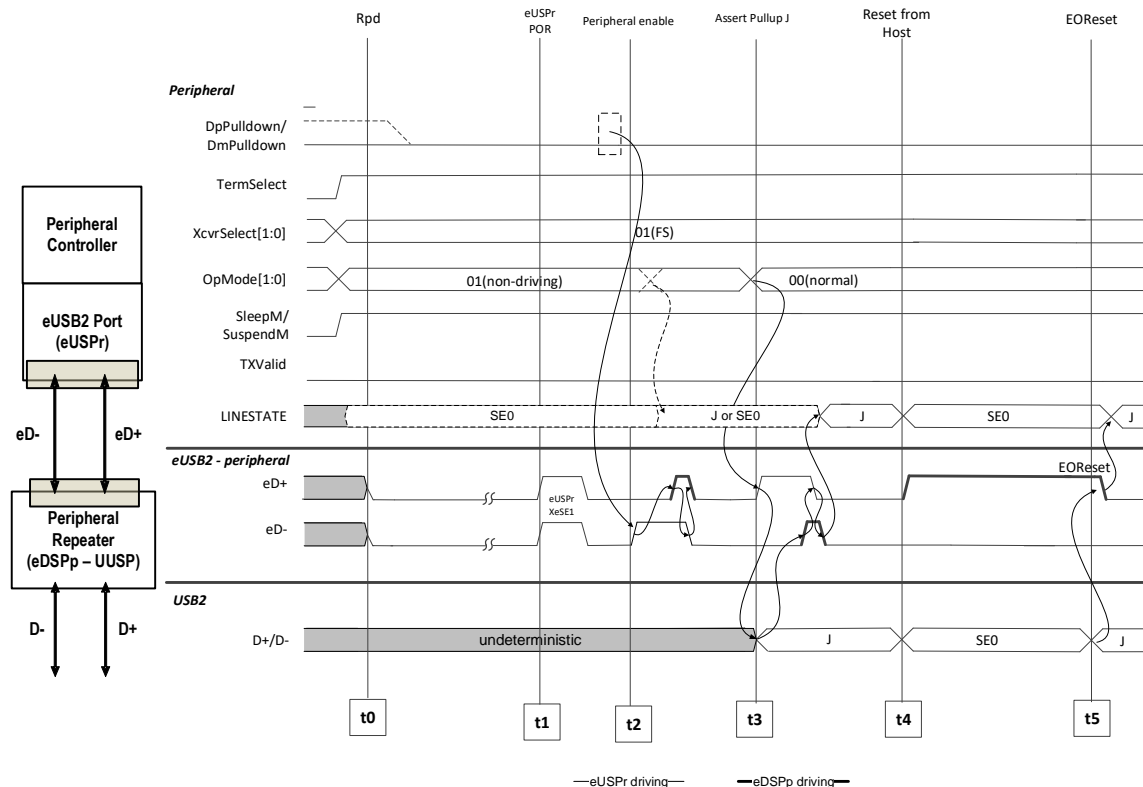
t5:

- EOReset (LS UI duration) from eDSPr. Note: Depending on implementation, UTMI+ xcvrselect and opmode may not change together with UTMI+ termselect. UTMI+ termselect may be the sole trigger for EOReset.
- Link enter FS L0 operation.



### 5.5.2 Peripheral Mode Repeater POR and Configuration

Figure 5-17 shows the timing diagram of a peripheral mode repeater sequencing through Port Reset, Default, Connect, Reset and L0.



**Figure 5-17: Peripheral Mode Repeater Configuration**

- t0:**
- Power-up with eSE0 maintained with Rpd. Note that depending on device controller requirement, Linestate may require to be at SE0 when opmode is non-driving.
- t1:**
- eUSPr transmits Port Reset upon POR. Note that, eUSPr shall ensure an idle (eSE0) time of  $T_{CONFIG\_IDLE}$  after transmitting Port Reset and Repeater Configuration.
- t2:**
- eUSPr transmits Repeater Configuration with logic '1' on eD-, to its associated repeater for peripheral mode operation. Note: UTMI+ pulldown indicating peripheral mode operation may have been stable or static at t0. Transmission of Repeater Configuration shall not depend on a change on UTMI+ pulldown. This is implementation specific on when to initiate this announcement where eDSPr/eUSPr may sample the UTMI+ pulldown state upon completion of XeSE1. If UTMI+ pulldown indicator changes after or during Repeater Configuration, eDSPr and eUSPr shall transmit XeSE1 as Port Reset, follow by Repeater Configuration to re-configure its repeater.
  - eDSPp acknowledges to eUSPr upon POR. Note: eDSPp POR is asynchronous to eUSPr. If eUSPr completes POR prior to eDSPp, eUSPr shall transmit Port Reset announcement follow by Repeater Configuration and monitor for eDSPp acknowledgement. If eDSPp completes POR first, it shall stay in Default pending eUSPr Port Reset and Repeater Configuration.
  - Note: as illustrated with the dotted arrow, UTMI+ opmode may have transition to "normal" earlier (or at t0). Some device controller may require LineState to be default at J (or SE0) before the repeater configuration, depending on OpMode. In this

scenario, eUSPr shall change its UTMI+ LineState to J (or remain as SE0) depending on behavioral requirement of the device controller implementations, but only transmit logic '1' on eD+ after it has received Repeater Configuration.

- Note: depending on behavioral requirement of the device controller implementations, LineState mapping may or may not become valid until the repeater configuration is completed.

t3:

- eUSPr transmits logic '1' on eD+ to its associated repeater to enable pullup J.
- Peripheral repeater asserts Pullup-J on D+/D-.
- eDSPp pulses eD-, eUSPr drops eD+ and eDSPp drops eD-.
- eUSPr LineState indicates J upon eDSPp acknowledgement.
- bus state on eUSPr change from SE0 to J.

t4:

- Reset from Host results in SE0 on D+/D-.
- eDSPp maps D+/D- SE0 to logic '1' on eD+.

t5:

- EOReset from host with J on D+/D-.
- eDSPp maps D+/D- J to eSE0 on eD+/eD-.
- Link enters FS L0 operation.

### 5.5.3 Establishing LS Link

In the scenario where a host and LS peripheral is connected, Figure 5-18 shows the sequence of a Host and Peripheral repeater with its associated eDSPr/eUSPr connecting, USB 2.0 Bus Reset and eventually entering L0.

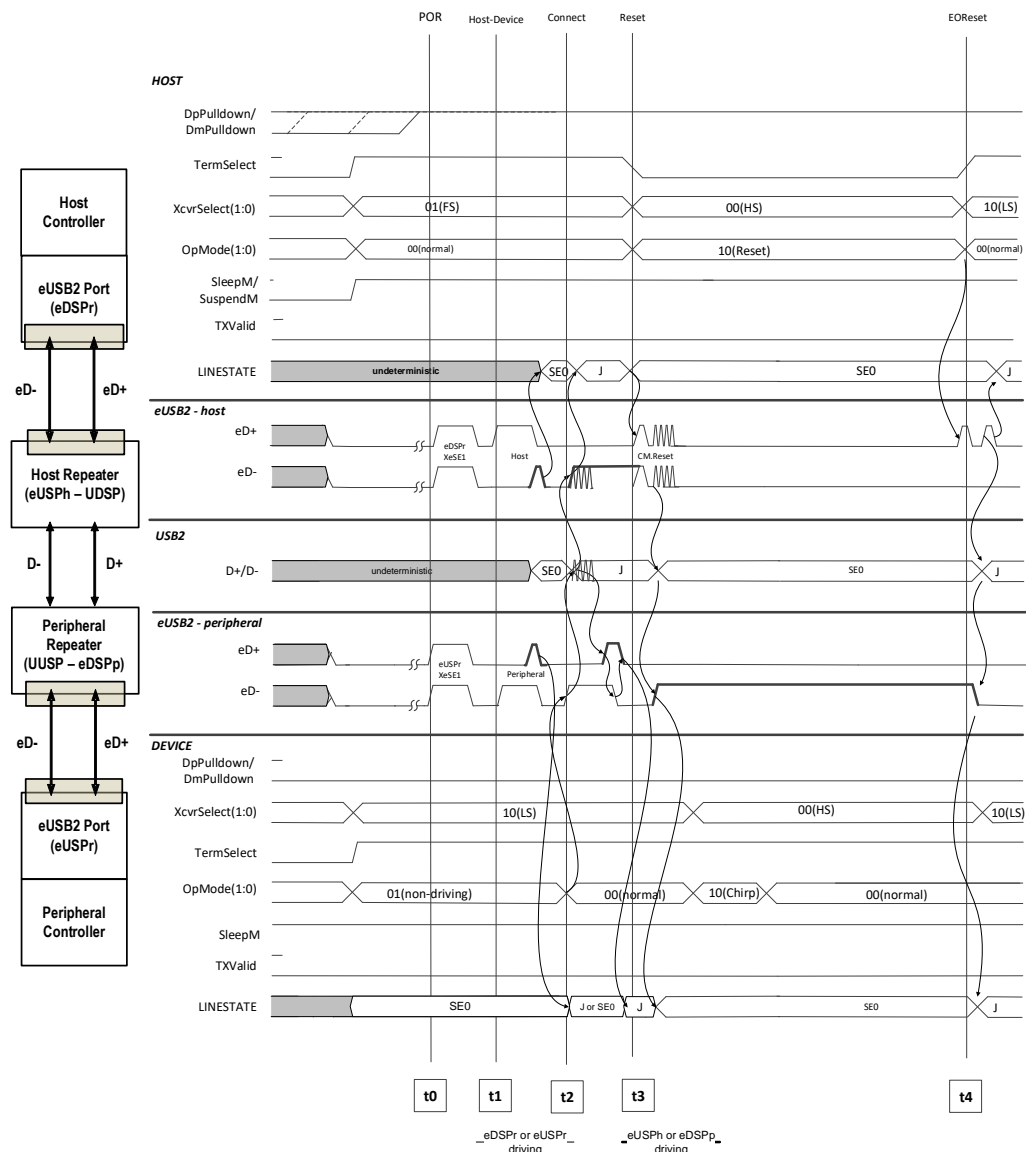


Figure 5-18: Establishing LS Link

- t0:
- eDSPr and eUSPr POR with Port Reset announcement.
  - Note that these PORs are asynchronous.
  - Note that depending on device controller requirement, Linestate may require to be at SE0 when opmode is non-driving.
- t1:
- eUSPr and eDSPr configuring peripheral and host mode operation respectively with Repeater Configuration.
  - eDSPp and eUSPh acknowledge.
  - Note that these events are aeUSPr synchronous.

t2:

- eUSPr asserts logic '1' on eD- to enable pull up J for device attach.
- Note that, device controller may require LineState to be J (or SE0) when OpMode become normal. In this scenario, eUSPr shall change its UTMI+ LineState to J (or remain as SE0) depending on behavioral requirement of the device controller implementations, but only transmit logic '1' on eD+ after it has received Repeater Configuration.
- Lineatate indicates J upon eDSPp acknowledgement.
- Device attach event propagates to eDSPr.
- Note that USB 2.0 D+/D- is shown experiencing a signaling bounce. These bounces are mapped to the eUSB2 bus as defined in Section 5.3.1.

t3:

- eDSPr transmits CM.Reset to eUSPh for USB 2.0 Bus Reset.
- eUSPh drops logic '1' on eD- and declare a LS connection.
- eDSPp maps SE0 on D+/D- to logic '1' on eD-.

t4:

- EOReset from eDSPr resulted with a LS J on D+/D-. Note: Depending on implementation, UTMI+ xcvrselect and opmode may not change together with UTMI+ termselect. UTMI+ termselect may be the sole trigger for EOReset.
- eDSPp maps D+/D- J to eSE0 on eD+/eD-.
- Link enters LS L0 operation.

### 5.5.4 Establishing HS Link

In the scenario where a HS capable host and peripheral is connected, Figure 5-19 shows the sequence of a Host and Peripheral repeater with its associated eDSPr/eUSPr connecting, chirping and eventually entering L0.

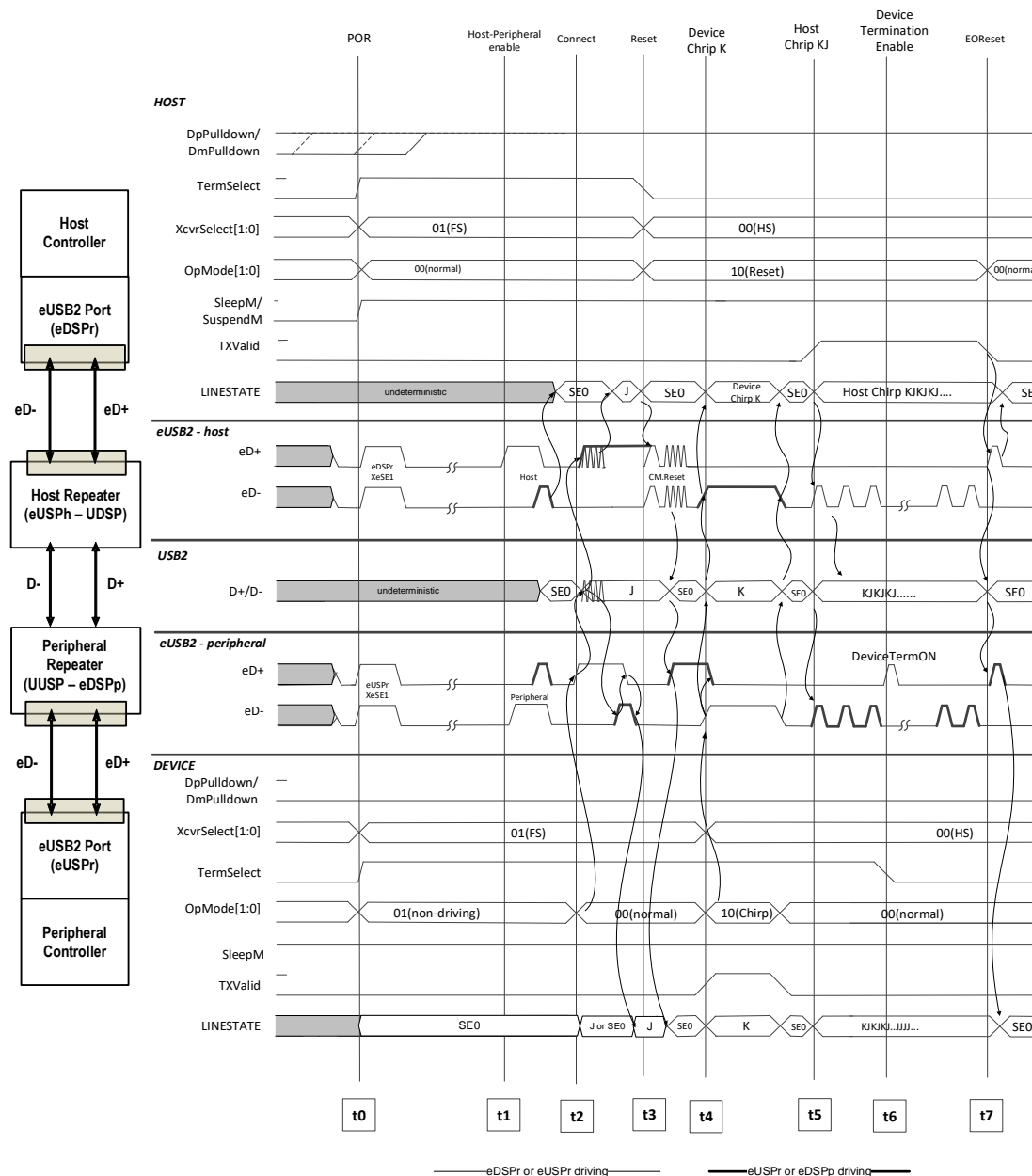


Figure 5-19: Establishing HS Link

t0:

- eDSPr and eUSPr POR with Port Reset announcement.
- Note that these PORs are asynchronous.

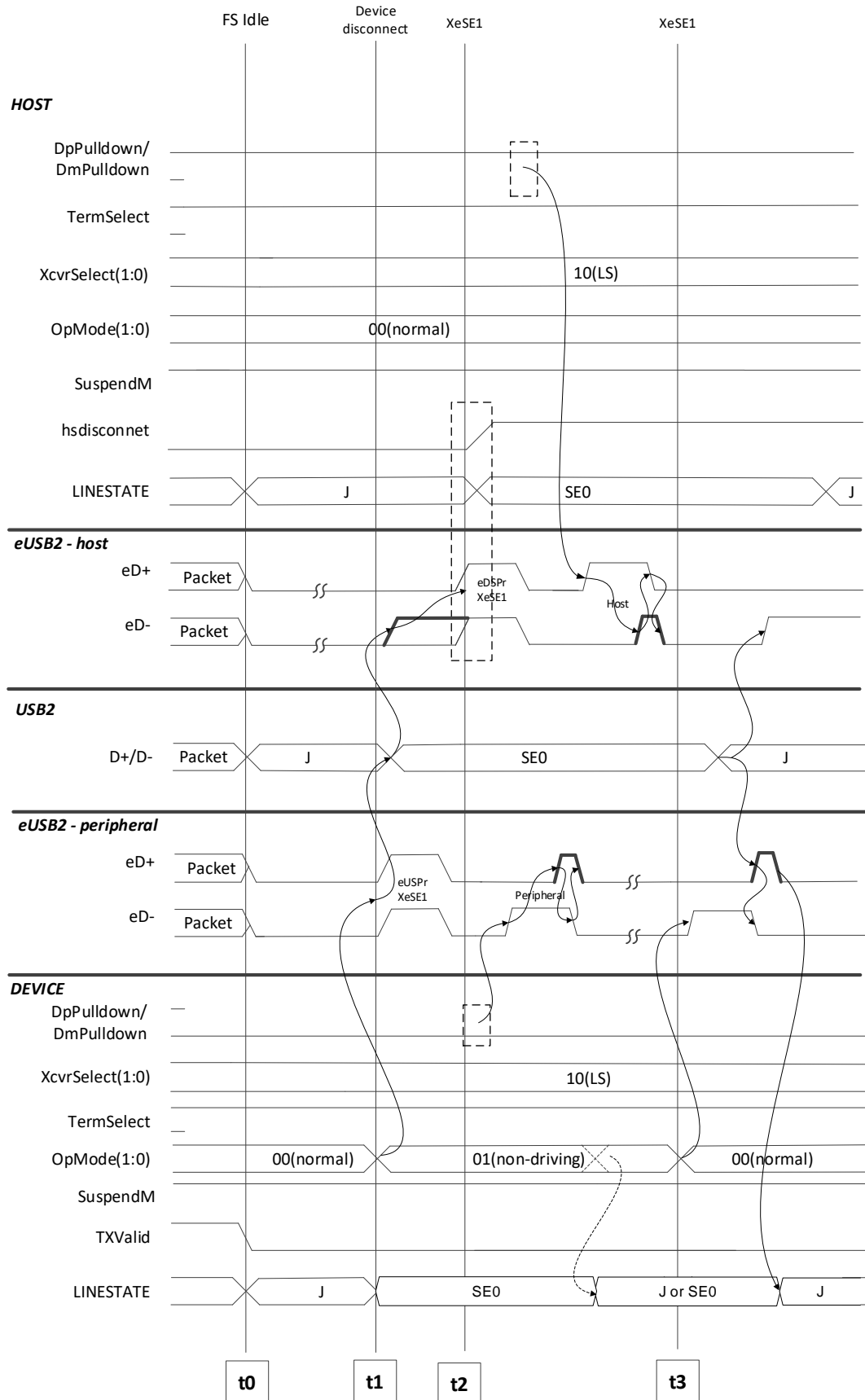
t1:

- eUSPr and eDSPr configuring peripheral and host mode operation respectively with Repeater Configuration.
- eDSPp and eUSPh acknowledge.

- Note that these events are asynchronous.
- t2:
- eUSPr asserts logic '1' on eD+ to enable pull up J for device attach.
  - eUSPr Lineatate indicates J upon eDSPp acknowledgement.
  - Device attach event propagates to eDSPr.
  - Note that USB 2.0 D+/D- is shown experiencing a signaling bounce. These bounces are mapped to the eUSB2 bus as defined in Section 5.3.1.
- t3:
- eDSPr transmits CM.Reset to eUSPh for USB 2.0 Bus Reset.
  - eUSPh drops logic '1' on eD+ and declare a FS (or HS depending on chirp handshake during USB 2.0 Bus Reset) connection.
  - eDSPp maps SE0 on D+/D- to logic '1' on eD+.
  - Note: This same flow of event is applicable for a FS idle link (where an idle J transition to SE0 on D+/D- is mapped to an eSE0 on eD+/eD- transition to logic '1' on eD+) being reset and eventual established as HS (in the case of FS upgrading to HS).
- t4:
- eUSPr transmits device chirp K.
  - eDSPp drops eD+ upon receiving device chirp K.
- t5:
- Host chirp K-J follows.
- t6:
- eUSPr pulses eD+ to eDSPp to indicate transition to HS.
  - UUSP enables HS termination.
  - eUSPr reports LineState change from Chirp to Squelch at UTMI+
- t7:
- EOReset and enter L0.

### 5.5.5 **LS Link Disconnect and Reconnect**

This flow, as shown in Figure 5-20, describes the process where Host and Peripheral disconnecting from an established a LS link, and finally reconnecting.



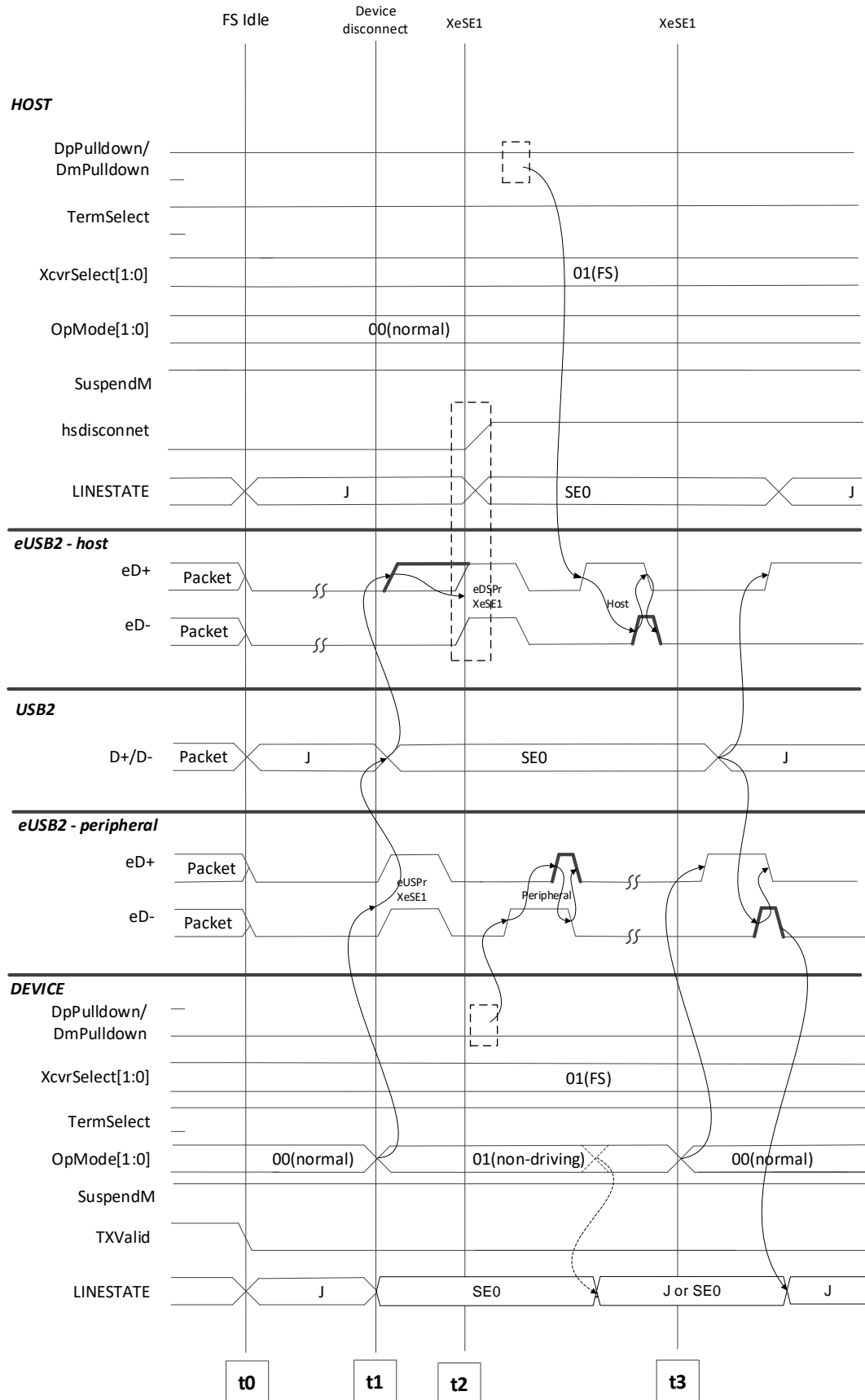


**Figure 5-20: LS Link Disconnect and Reconnect**

- t0:
- LS idle with pull-up J at D-.
  - LS idle with eSE0 on eD+/eD-.
- t1:
- eUSPr triggers soft disconnect with UTMI+ opmode changed. Note: physical device detach would behave similarly with D+/D- becoming SE0.
  - eUSPr transmit XeSE1 to eDSPp to remove pull-up J. Peripheral repeater removes pull-up J upon declaring xeSE1 detection.
  - D+/D- becomes SE0 and eUSPh maps this to logic '1' on eD-. Note: Host Repeater does not qualify this SE0 as device disconnect but rather mapping D+/D- SE0 to logic '1' on eD-. It is the responsibility of eDSPr to qualify logic '1' on eD- and declare device disconnect.
  - Note that depending on device controller requirement, LineState may be required to be SE0 when opmode is non-driving.
- t2:
- Upon detecting logic '1' on eD- and declaring device disconnect, eDSPr transmits XeSE1 to eUSPh to indicate device disconnect.
  - At the same time, eDSPr's UTMI+ interface reflecting device disconnect.
  - eUSPh stop driving logic '1' on eD- upon receiving XeSE1 from eDSPr.
  - Both eUSPh and eDSPp return to default mode, and Repeater Configuration follows to re-enable operation.
  - Note: UTMI+ pulldown may be static as indicated in Figure 5-20, hence transmitting Repeater Configuration shall not be triggered with the UTMI+ pulldown transition. This is implementation specific on when to transmit this announcement where eDSPr/eUSPr may sample the UTMI+ pulldown state upon completion of XeSE1. If UTMI+ pulldown indicator changes after or in the middle of transmitting Repeater Configuration, eDSPr and eUSPr shall transmit XeSE1 as Port Reset, follow by Repeater Configuration to re-configure its repeater.
- t3:
- eUSPr transmitting logic '1' on eD- as directed by its controller to initiate a new connection.
  - Note that, as illustrated with the dotted arrow, UTMI+ opmode may have transition to "normal" earlier. In this scenario, eUSPr shall change its UTMI+ LineState to J or remain as SE0 depending on behavioral requirement of the device controller implementations, but only transmit logic '1' on eD- after it has received Repeater Configuration.

### 5.5.6 FS Link Disconnect and Reconnect

This flow, as shown in Figure 5-21, describes the process where Host and Peripheral disconnecting from an established a FS link, and finally reconnecting



**Figure 5-21: FS Link Disconnect and Reconnect**

- t0:
- FS idle with pull-up J on D+/D-.
  - FS idle with eSE0 on eD+/eD-.
- t1:
- eUSPr triggers soft disconnect with UTMI+ opmode changed. Note: physical device detach would behave similarly with D+/D- becoming SE0.
  - eUSPr transmit XeSE1 to eDSPp to remove pullup J.
  - D+/D- becomes SE0 and eUSPh maps this to logic '1' on eD+. Note: Host Repeater does not qualify this SE0 as device disconnect but rather mapping D+/D- SE0 to logic '1' on eD+. It is the responsibility of eDSPr to qualify logic '1' on eD+ and declare device disconnect.
  - Note that depending on device controller requirement, LineState may be required to be SE0 when opmode is non-driving.
- t2:
- Upon detecting logic '1' on eD+ and declaring device disconnect, eDSPr transmits XeSE1 to eUSPh to indicate device disconnect.
  - At the same time, eDSPr's UTMI+ interface reflecting device disconnect.
  - eUSPh stop driving logic '1' on eD+ upon receiving XeSE1 from eDSPr.
  - Both eUSPh and eDSPp return to default mode, and Repeater Configuration follows to re-enable operation.
  - Note: UTMI+ pulldown may be static as indicated in Figure 5-21, hence transmitting Repeater Configuration shall not be triggered with the UTMI+ pulldown transition. This is implementation specific on when to transmit this announcement where eDSPr/eUSPr may sample the UTMI+ pulldown state upon completion of XeSE1. If UTMI+ pulldown indicator changes after or in the middle of transmitting Repeater Configuration, eDSPr and eUSPr shall transmit XeSE1 as Port Reset, follow by Repeater Configuration to re-configure its repeater.
- t3:
- eUSPr transmitting logic '1' on eD+ as directed by its controller to initiate a new connection.
  - Note that, as illustrated with the dotted arrow, UTMI+ opmode may have transition to "normal" earlier. In this scenario, eUSPr shall change it UTMI+ LineState to J or remain as SE0 depending on behavioral requirement of the device controller implementations, but only transmit logic '1' on eD+ after it has received Repeater Configuration.

### 5.5.7 Disconnecting from HS Link

As oppose to FS/LS where declaring disconnect (XeSE1) is the responsibility of eDSP, detecting and declaring HS disconnect is performed by the host repeater. Figure 5-22 shows the sequence of which the host repeater declaring a HS disconnect.

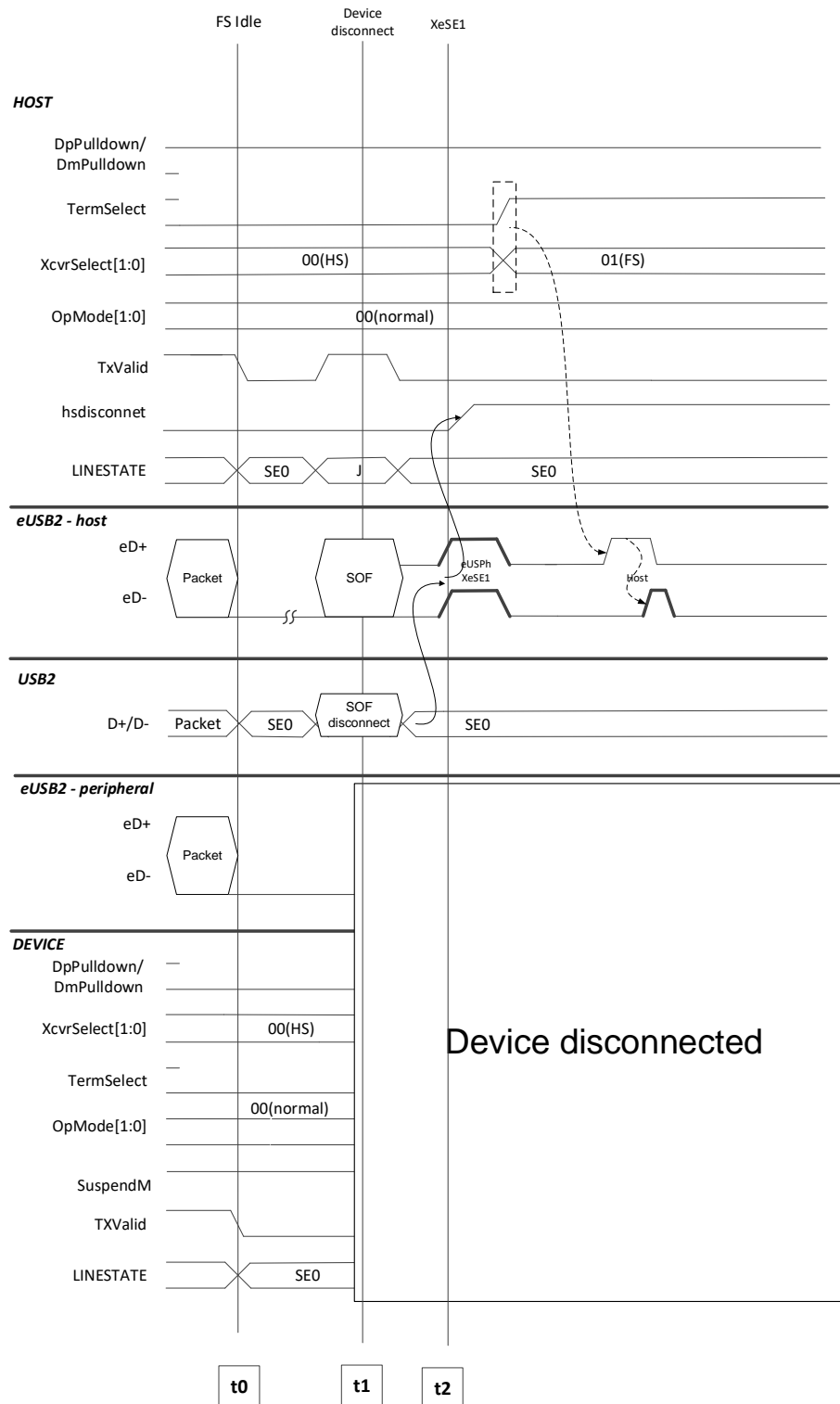


Figure 5-22: HS disconnect

- t0:
- HS idle with SE0 on D+/D- and eSE0 on eD+/eD-.
- t1:
- Device disconnected with SOF amplitude changed.
- t2:
- eUSPh transmits XeSE1 to indicate HS device disconnect.
  - eDSPr reflects disconnect to UTMI+ interface. Note that eDSPr shall not transmit Port Reset after receiving eUSPh XeSE1 device disconnect.
  - eUSPh returns to default mode of operation and Repeater Configuration follow to re-enable it.
  - Note: Implementation may utilize termselect and xcvrselect change to transmit Repeater Configuration.

### 5.5.8 Bus Reset during FS Link

Once a FS link is established and a USB 2.0 Bus Reset is triggered, Figure 5-23, shows the transition of the events and eventually re-establishing a link.

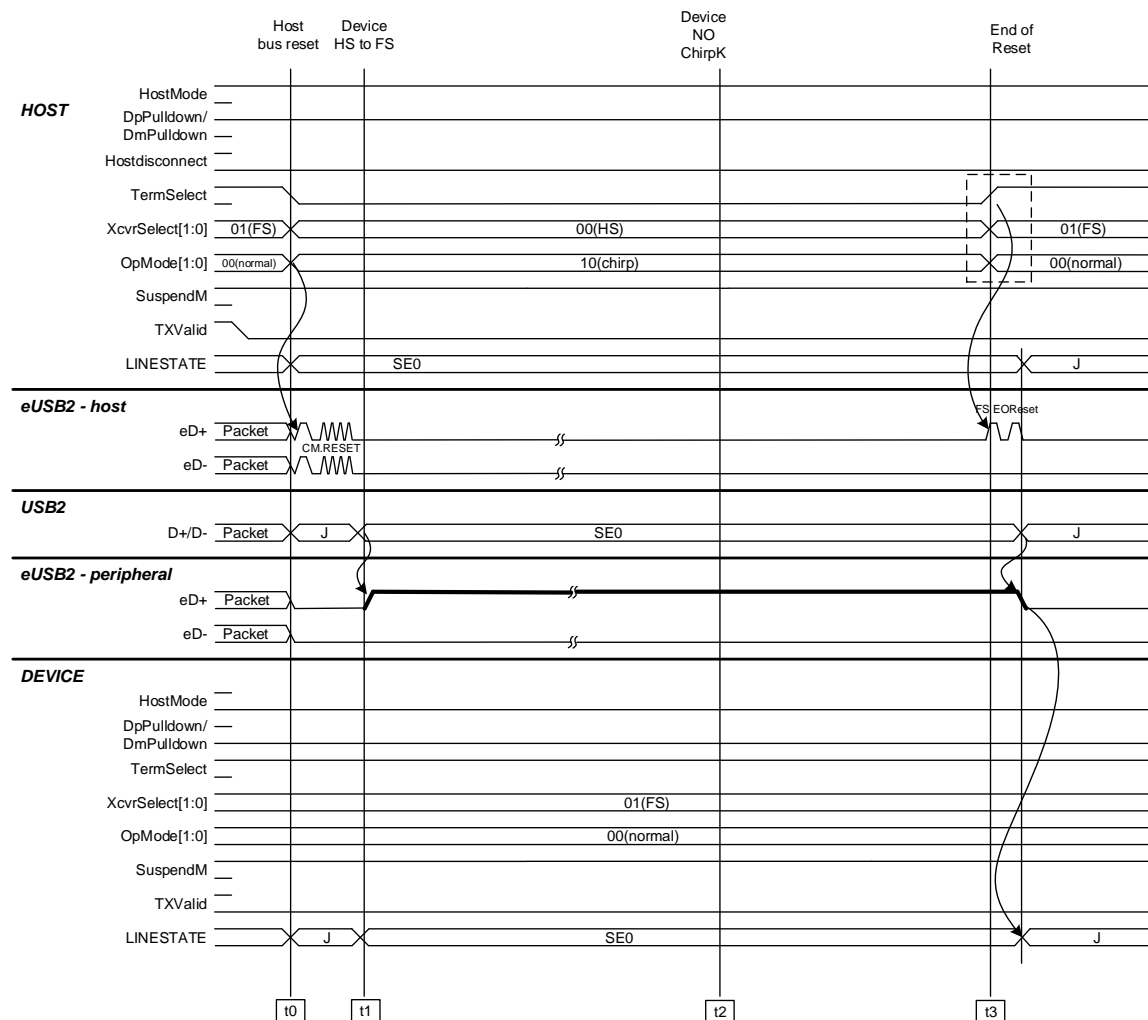
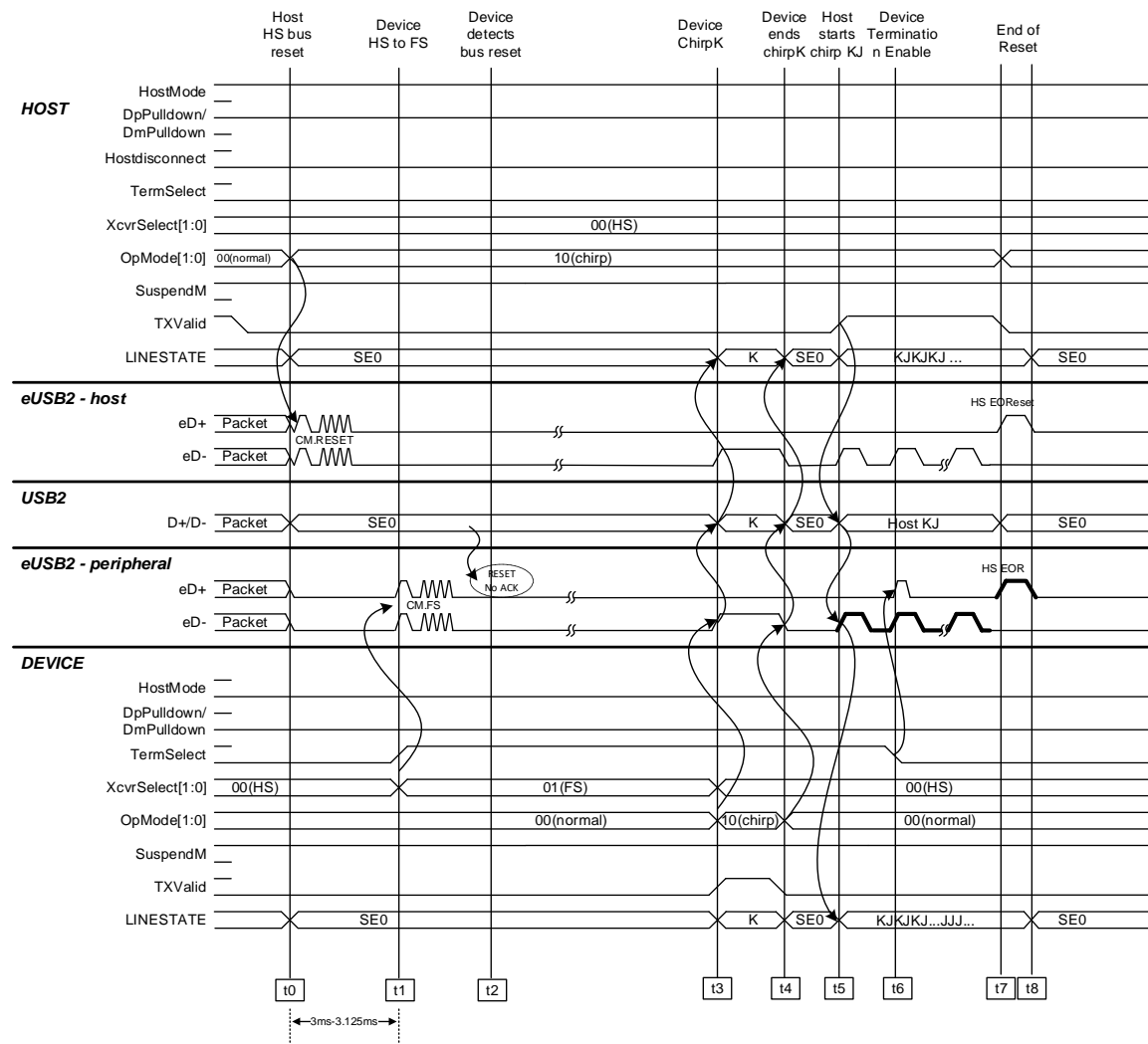


Figure 5-23: FS Link Bus Reset

- t0:
- eDSPr USB 2.0 Bus Reset with CM.Reset.
- t1:
- eUSPh receives CM.Reset; directs its UDSP to apply HS terminations and drive the USB 2.0 bus to SE0
  - UUSP observes J to SE0 transition on USB 2.0 bus; eDSPp performs FS mapping and drives eD+ high.
  - eUSPr reflects this condition as SE0 on LineState.
- t2:
- eUSPr does not transmit device chirp K.
- t3:
- eDSPr transmits FS EOReset.
  - UDSP removes the driven SE0 condition on USB 2.0 bus
  - UUSP after observing a J on USB 2.0 bus, directs its eDSPp to stop driving the eD+ line
  - eUSPr changes its LineState to J from SE0

### 5.5.9 Bus Reset during HS Link

Once a HS link is established and a USB 2.0 Bus Reset is triggered, Figure 5-24, shows the transition of the events and eventually re-establishing a link.



**Figure 5-24: HS Link Bus Reset**

- t0:
  - eDSPr USB 2.0 Bus Reset with CM.Reset.
- t1:
  - eUSPr sends CM.FS after 3ms to check for USB 2.0 Bus Reset or entry to Suspend
  - Peripheral repeater starts TPR\_RESET\_FROM\_HS timer and at its UUSP removes HS terminations and applies J pull-up. Before observing J at UUSP, the peripheral repeater remains in HS bus state mapping at eDSPp.
- t2:
  - TPR\_RESET\_FROM\_HS timer expires and the peripheral repeater continues to observe SE0 at UUSP indicating USB 2.0 Bus Reset. eDSPp sends no pulse/acknowledge on eD+.
- t3:
  - eUSPr transmits device chirp K.



- eUSPh forwards device chirp K to eDSPr at eD-
- t4:
- eUSPr ends device chirp K.
- t5:
- eDSPr transmits host chirp K.
- t6:
- eDSPr and eUSPr transmits HS termination acknowledgement.
- t7:
- eDSPr and eDSPp transmits EOReset.
- t8:
- eUSBr completes HS EOReset transmission or reception and switch to HS mode with receiver termination enabled and input in squelched condition.

### 5.5.10 Bus Reset to FS with HS capable device and FS capable host

Figure 5-25 shows the transition of the events of a USB 2.0 Bus Reset during with a HS capable device connecting to a FS capable host.

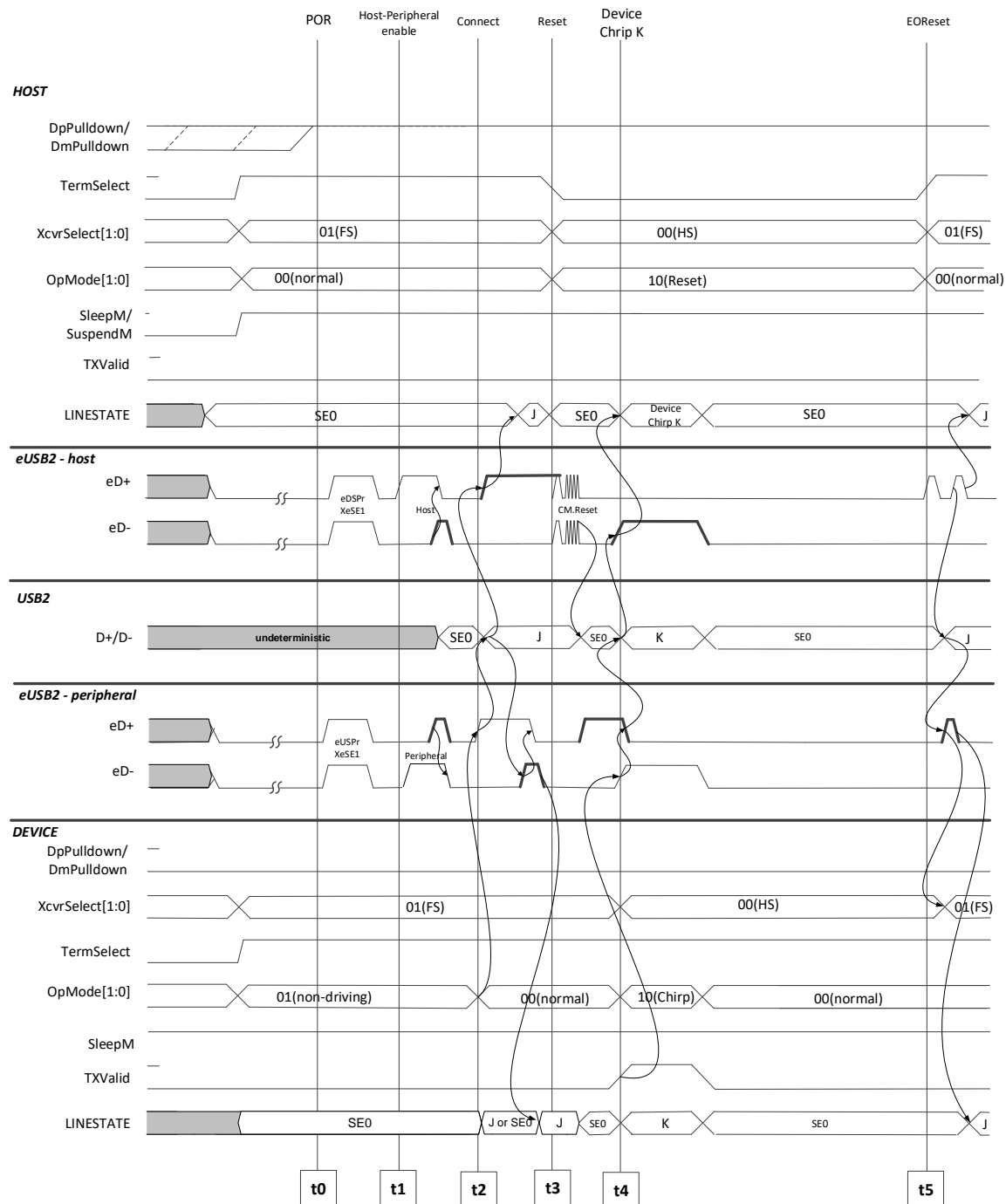
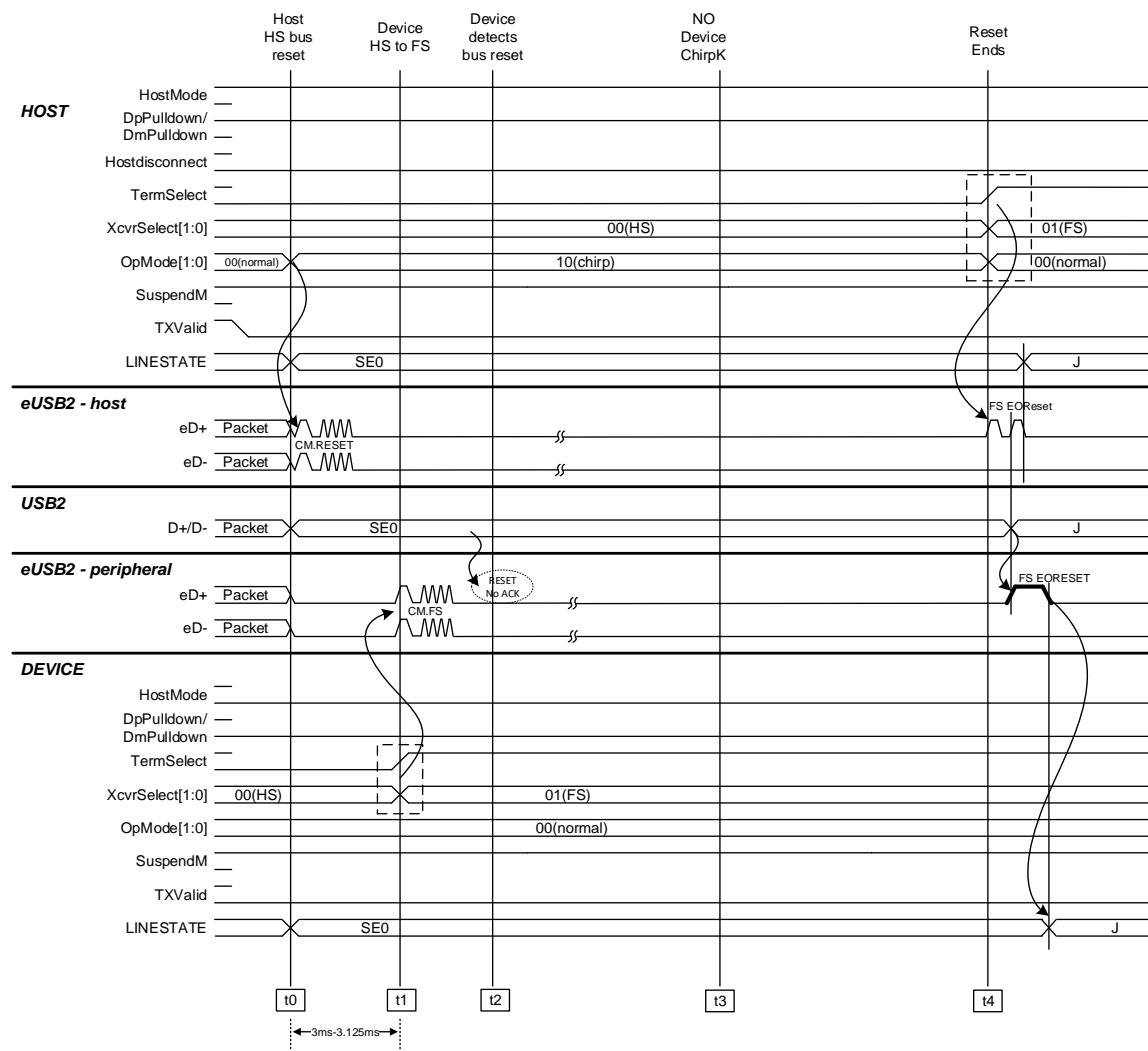


Figure 5-25: FS Link Bus Reset with FS host and HS device

- t0:
- eDSPr and eUSPr POR with Port Reset.
  - Note that these PORs are asynchronous.
- t1:
- eUSPr and eDSPr configuring peripheral and host mode operation respectively with Repeater Configuration.
  - eDSPp and eUSPh acknowledge upon POR.
  - Note that these events are asynchronous.
- t2:
- eUSPr asserts logic '1' on eD+ to enable pull up J for device attach.
  - Device attach event propagates to eDSPr.
- t3:
- eDSPr transmits CM.Reset to eUSPh for USB 2.0 Bus Reset.
  - eUSPh drops logic '1' on eD+ and declare a FS (or HS depending on chirp handshake during USB 2.0 Bus Reset) connection.
  - eDSPp maps SE0 on D+/D- to logic '1' on eD+.
  - Note: This same flow of event is applicable for a FS idle link (where an idle J transition to SE0 on D+/D- is mapped to an eSE0 on eD+/eD- transition to logic '1' on eD+) being reset and eventual established as HS (in the case of FS upgrading to HS).
- t4:
- eUSPr transmits device chirp K.
  - eDSPp drops eD+ upon receiving device chirp K.
  - Note: Observed not host K-J chirp.
- t5:
- eDSPr transmits EOReset (LS UI) and transition to FS L0.
  - eDSPp upon observing SE0 to J transition on UUSP, transmits EOReset to eUSPr to end USB 2.0 Bus Reset and enter FS L0.

### 5.5.11 Bus Reset to FS during HS Link

Figure 5-26 shows the transition of the events of a USB 2.0 Bus Reset during HS link with the eventual re-established to FS.



**Figure 5-26: HS Link Bus Reset to FS**

- t0:
- eDSPr HS USB 2.0 Bus Reset with CM.Reset.
- t1:
- eUSPr sends CM.FS after 3ms to check for reset or suspend.
  - Peripheral repeater starts  $T_{PR\_RESET\_FROM\_HS}$  timer and at its UUSP removes HS terminations and applies J pull-up. Before observing J at UUSP, the peripheral repeater remains in HS bus state mapping at eDSPP.
- t2:
- Peripheral repeater detected SE0 upon  $T_{PR\_RESET\_FROM\_HS}$  expiration at UUSP indicating USB 2.0 Bus Reset. Note: In this scenario where an established HS link is downgraded to FS, the peripheral repeater shall recognize this as USB 2.0 Bus Reset where in this case Idle J is only presented after  $T_{PR\_RESET\_FROM\_HS}$  expiration at UUSP as compared to Lx entry as illustrated in Section 5.5.17.
  - UUSP samples SE0 on D+/D-
  - eDSPP sends no pulse/acknowledge on eD+.

- t3:
- eUSPr does not transmit device chirp K. Note: Transition is applicable if device transmits chirp K but host doesn't not perform chirp K-J.
- t4:
- eDSPr transmits FS EOReset (LS UI).
  - UDSP removes the driven SE0 condition on USB line
  - UUSP after observing a J on USB 2.0 bus, directs its eDSPp to send T<sub>STROBE</sub> EOReset pulse
  - eUSPr updates its LineState to J from SE0

### 5.5.12 FS Link L1 entry and Resume

FS link L1 entry and Resume sequences are illustrated in Figure 5-27 below. Note that CM.FS (also CM.L1 or CM.L2) may or may not be issued by eDSPr or eUSPr in FS/LS operations, and it may lead to different state transitions of the host repeater and the peripheral repeater. However, this behavioral difference of the repeater operations does not change the exit sequence of the link and will not be described in this section and related sections.

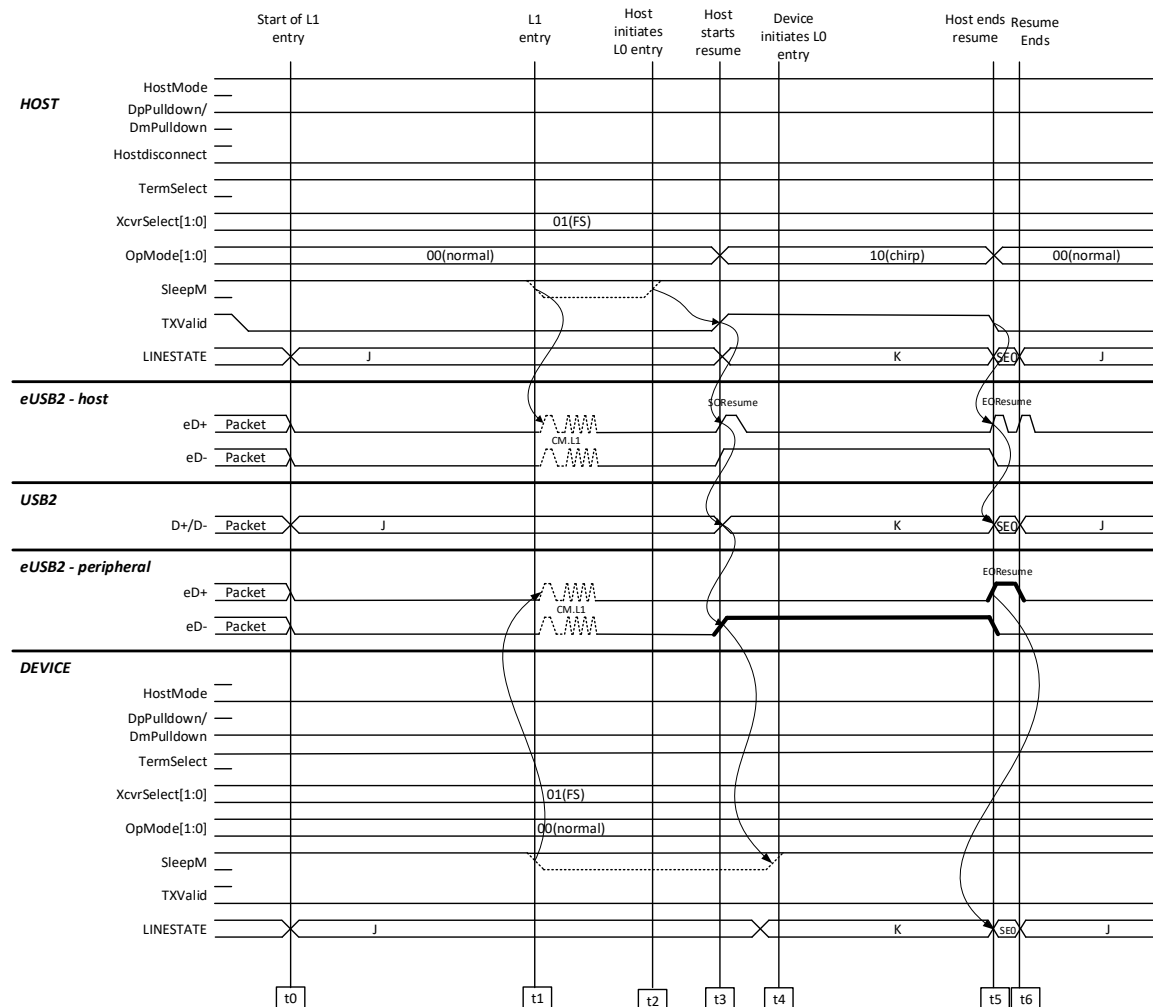


Figure 5-27: FS Link L1 entry and Resume

- t0:
  - eDSPr initiates suspend, stops driving anything on the USB 2.0 bus
- t1:
  - eDSPr and eUSPr declare bus L1 entry after L1 token exchange
  - Respective controllers may or may not assert SleepM
  - If SleepM asserted, eDSPr or eUSPr port sends CM.FS to its repeater
- t2:
  - eDSPr controller initiates L0 entry
- t3:
  - eDSPr starts sending Resume,
  - eUSPh detects eSE1 followed by logic '1' on eD-; eUSPh stops FS mapping mode
  - UDSP sends Resume at D+/D- after SOResume is declared.
  - eDSPp enters repeat mode after detecting K on USB 2.0 bus and drives eD- to logic '1'
  - eUSPr updates LineState to K
- t4:
  - eUSPr controller de-asserts suspend if required
- t5:
  - eDSPr ends Resume with EOResume
  - eDSPp exits repeat mode after observing EOP on USB 2.0 bus and sends EOResume to eUSPr
- t6:
  - Resume completes

#### 5.5.13 FS Link L2 entry and Resume

FS link L2 entry and Resume sequences are illustrated in Figure 5-28 below.

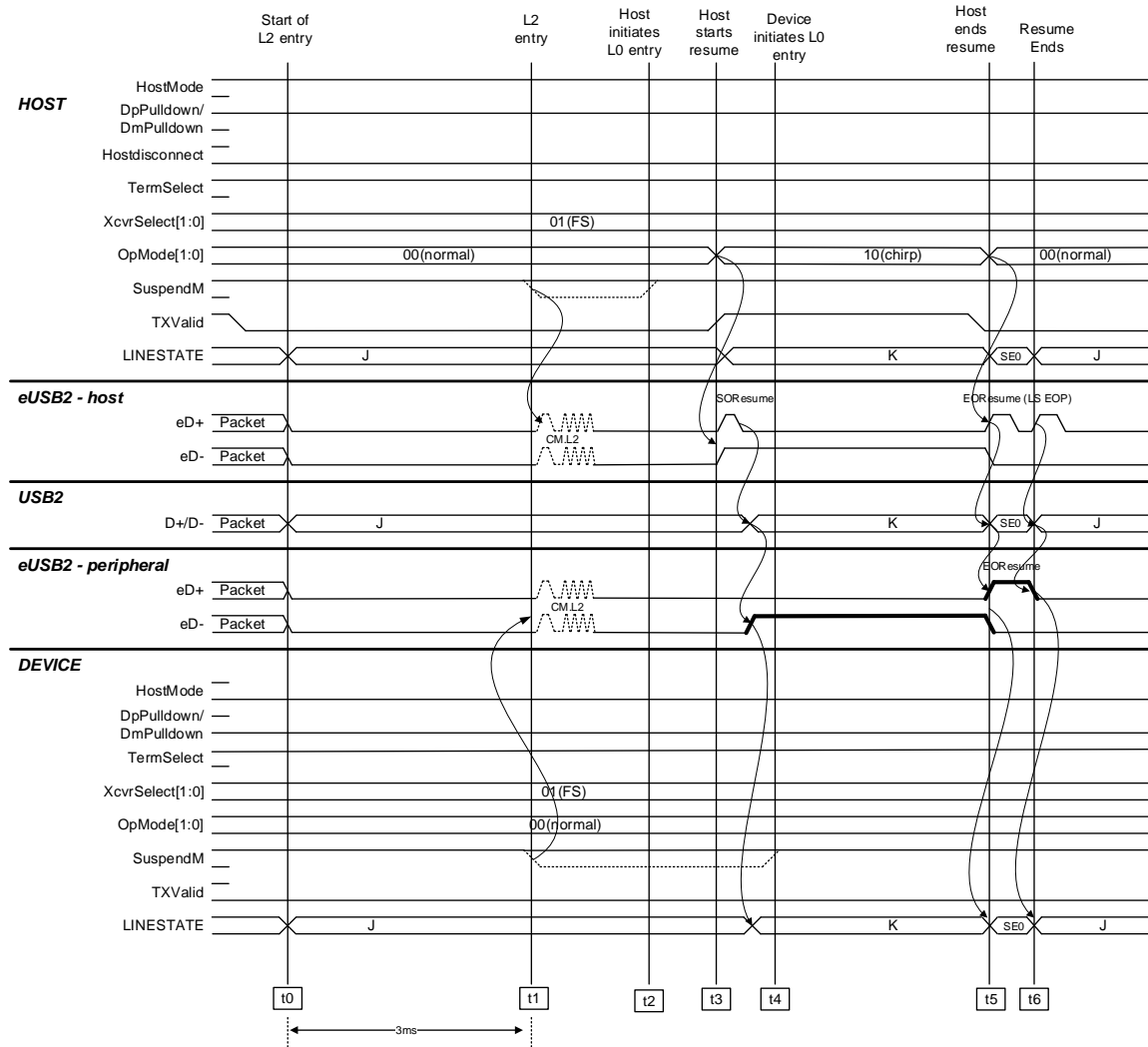


Figure 5-28: FS Link L2 entry and Resume

- t0:
- eDSPr initiates suspend, stops driving anything on the USB 2.0 bus
- t1:
- eDSPr and eUSPr declare bus suspend after 3ms
  - Respective controllers may or may not assert SuspendM
  - If suspend asserted, eUSB port sends CM.L2 to its repeater
- t2:
- eDSPr controller initiates L0 entry
- t3:
- eDSPr starts sending Resume,
  - eUSPh detects eSE1 followed by logic '1' on eD-; eUSPh stops FS mapping mode
  - UDSP sends Resume on USB 2.0 bus after eSE1 followed by logic '1' on eD- is detected.
  - eDSPp enters repeat mode after detecting K on USB 2.0 bus and drives eD- to logic '1'
  - eUSPr updates LineState to K
- t4:
- eUSPr controller de-asserts suspend if required

t5:

- eDSPr ends Resume with EOResume
- eDSPp exits repeat mode after observing EOP on USB 2.0 bus and sends EOP on eD+ line

t6:

- Resume completes



### 5.5.14 LS Remote Wake and Resume from L2

Link exiting L2 with a peripheral wake and host Resume is shown in Figure 5-29.

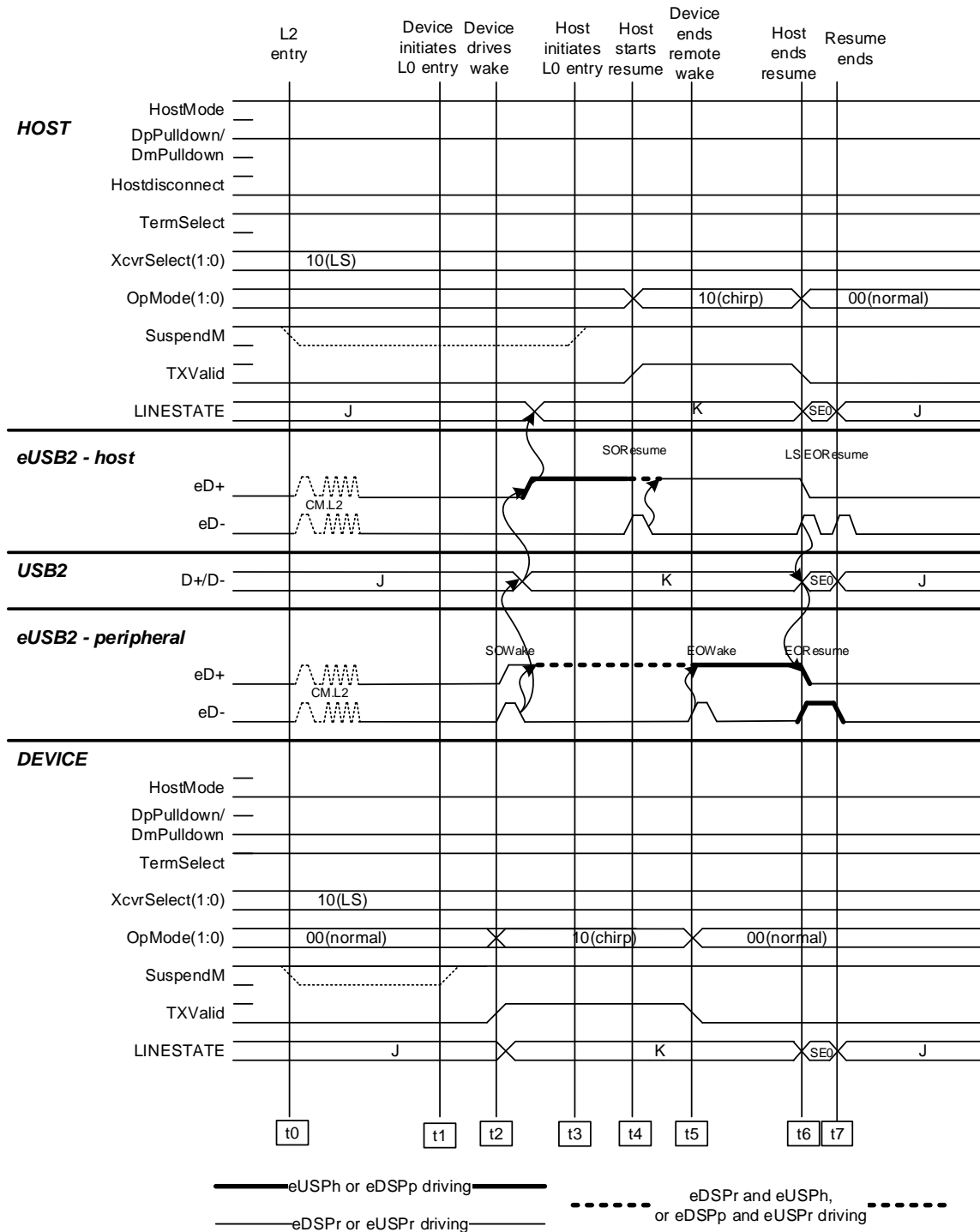


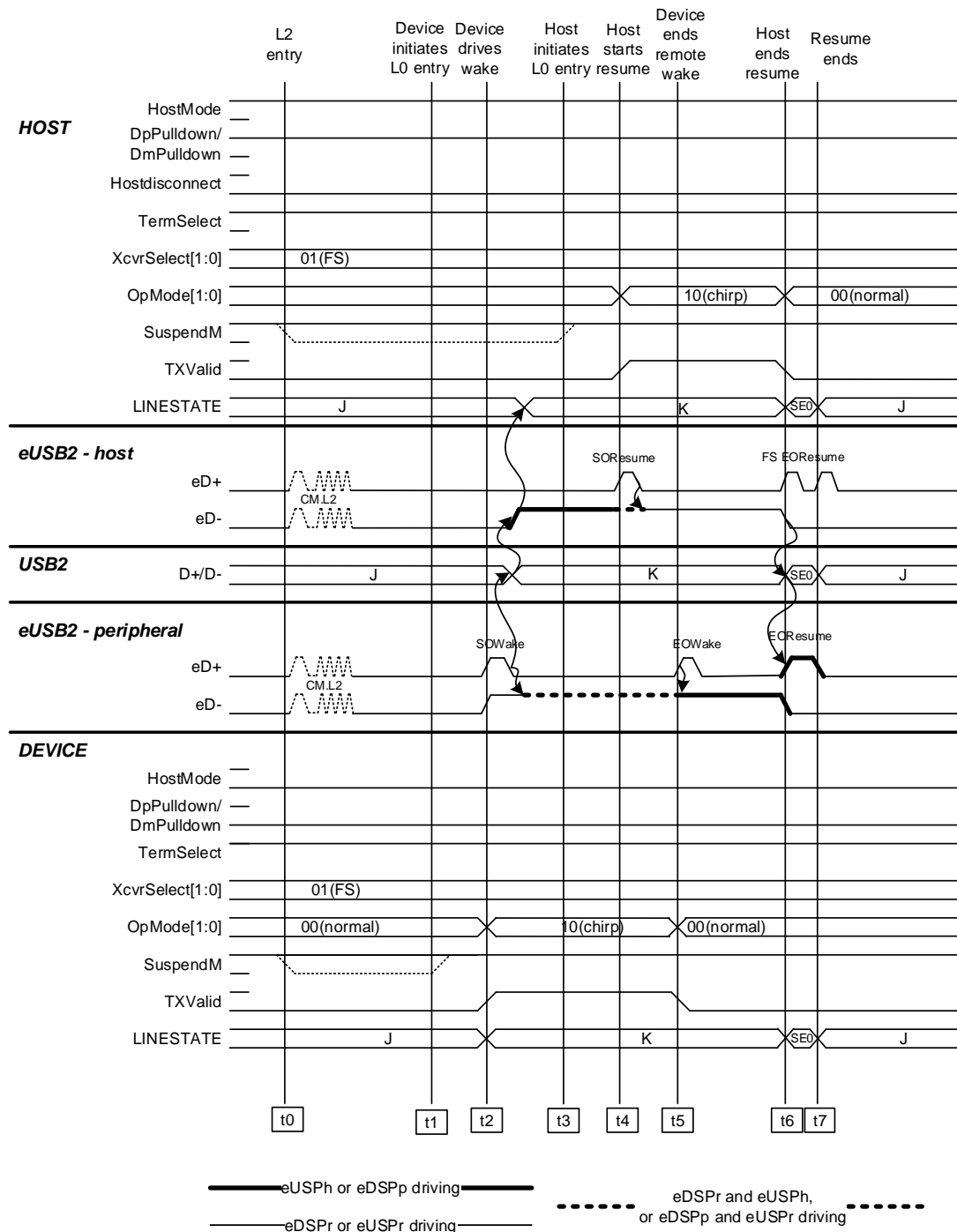
Figure 5-29: LS device Remote Wake and host Resume

- t0:
- Link in L2

- t1:
- eUSPr controller initiates L0 entry
- t2:
- eUSPr starts Remote Wake with SOWake
  - eDSPp detects eSE1 followed by a logic '1' on eD+, declares it as Remote Wake; UUSP starts Remote Wake on USB 2.0 bus
  - eDSPp reflects K on USB 2.0 bus driving logic '1' on eD+. Both eDSPp and eUSPr are driving eD+
  - UDSP detects Remote Wake K on USB 2.0 bus; eUSPh maps Remote Wake K at eUSB2 bus by driving logic '1' on eD+
  - eDSPr detects Remote Wake K on eD+ and updates LineState
- t3:
- eDSPr initiates L0 entry
- t4:
- eDSPr starts sending SOResume (Start of Resume). eD+ is driven by both eDSPr and eUSPh
  - eUSPh detects logic '1' at eD- and declares reception of SOResume after observing logic '1' to logic '0' transition at eD-; eUSPh stops driving Remote Wake K
  - UDSP continues driving Resume K at USB 2.0 bus
  - UUSP continues driving remote Wake K on USB 2.0 bus
- t5:
- eUSPr ends Remote Wake by sending EOWake (End of Wake)
  - eDSPp after detecting a logic '0' to logic '1' on eD-, declares the reception of EoWake
  - UUSP stops driving Remote Wake K on USB 2.0 bus
  - eDSPp continues to map USB 2.0 bus state at UUSP (Resume K) onto the eUSB2 bus to eUSPr
- t6:
- eDSPr ends Resume with EOResume
  - eDSPp ends Resume K after observing EOP on USB 2.0 bus and sends EOP on eUSB2 bus
- t7:
- Resume completes

### 5.5.15 FS Remote Wake and Resume from L2

Link exiting L2 with a peripheral wake and host Resume is shown in Figure 5-30.



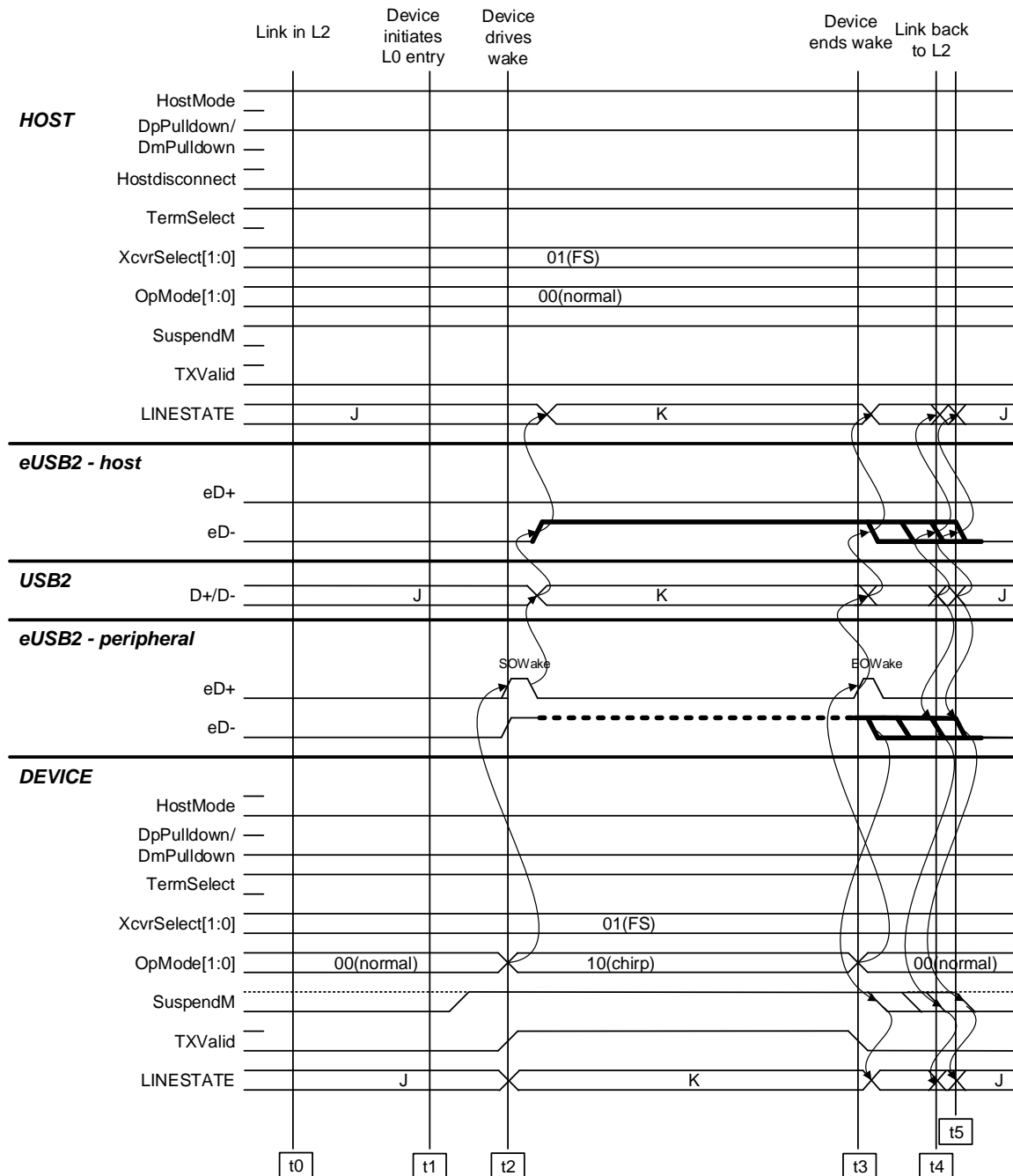
**Figure 5-30: FS device Remote Wake and host Resume**

- t0:
- Link in L2
- t1:
- eUSPr controller initiates L0 entry
- t2:

- eUSPr starts Remote Wake with SOWake
  - eDSPp detects eSE1 followed by a logic '1' on eD-, declares it as a remote-wake signal; UUSP sends Remote Wake on USB 2.0 bus
  - eDSPp maps K on USB 2.0 bus and drive logic '1' on eD-
  - UDSP detects Remote Wake K on the USB 2.0 bus; eUSPh drives logic '1' on eD-
  - eDSPr detects logic '1' on eD-, declares it as Remote Wake K and updates LineState
- t3:
- eDSPr initiates L0 entry
- t4:
- eDSPr starts sending Resume; both eDSPr and eSPh drive eD-
  - eUSPh detects eSE1 and stops driving Remote Wake K on eD- after declaring SoResume (eSE1 followed by logic '1' on eD-)
  - UDSP drives Resume K on USB 2.0 bus after declaring SoResume
- t5:
- eUSPr stops sending Remote Wake
  - eDSPp after detecting a logic '0' to logic '1' transition on eD+, declares the reception of EOWake
  - UUSP stops driving K on USB 2.0 bus; eDSPp assumes that the host Resume has happened and continues driving Resume K momentarily in order to maintain the continuity between Remote Wake and Resume
  - eDSPp maps the USB 2.0 bus state from UUSP to eUSB2 bus state towards eUSPr after observing Resume K
- t6:
- eDSPr ends Resume with EOResume
  - eDSPp exits repeat mode after observing EOP on USB 2.0 bus and sends EOP on eD+ line
- t7:
- Resume completes

### 5.5.16 FS Remote Wake without Resume from L2

Figure 5-31 illustrates the scenario where a device initiates a wake from L2, however, host Resume is not triggered.



**Figure 5-31: FS Link device wake without host Resume**

t0-t2:

- Link in L2 with eUSPr initiates L0 entry with Remote Wake.

t3:

- eUSPr ends Remote Wakeup with EOWake; UUSP stops driving K on USB 2.0 bus
- eDSPp maps USB 2.0 bus state observed onto eUSB2 bus. Note: K may continue to be presented on eD- after the completion EOWake before transition to J. In this case, the K to J transition shall not be declared as a host Resume instead it shall be a K to SE0 (EOResume).
- The peripheral repeater starts the  $T_{SE0\_FILTER}$  SE0 filter timer upon detecting start of EOWake. Possible SE0/SE1 at D+/D- is mapped as K/J at eD+/eD- as defined in Table 3-3.
- The host repeater starts the  $T_{SE0\_FILTER}$  SE0 filter timer upon detecting non-K bus state. Possible SE0/SE1 at D+/D- may be mapped as K or J as eD+/eD- as defined in Table 3-3. Note that the  $T_{SE0\_FILTER}$  SE0 filter timer starts asynchronously after the  $T_{SE0\_FILTER}$  SE0 filter timer of the peripheral repeater.

t4:

- The  $T_{SE0\_FILTER}$  SE0 filter timers expire independently.
- The host and peripheral repeaters map the bus state at D+/D- to eD+/eD- independently as defined in Table 3-3. SE1 may still be observed, driven J is mapped at eD+/eD-.

t5:

- The bus state at D+/D- finally reached idle J (if it did not at t4), the host and peripheral repeater map idle J (eSE0) at eD+/eD- and transition to L2.Idle.

#### 5.5.17 HS Link L2 entry and Resume

HS link L2 entry and Resume sequences are illustrated in Figure 5-32 below.

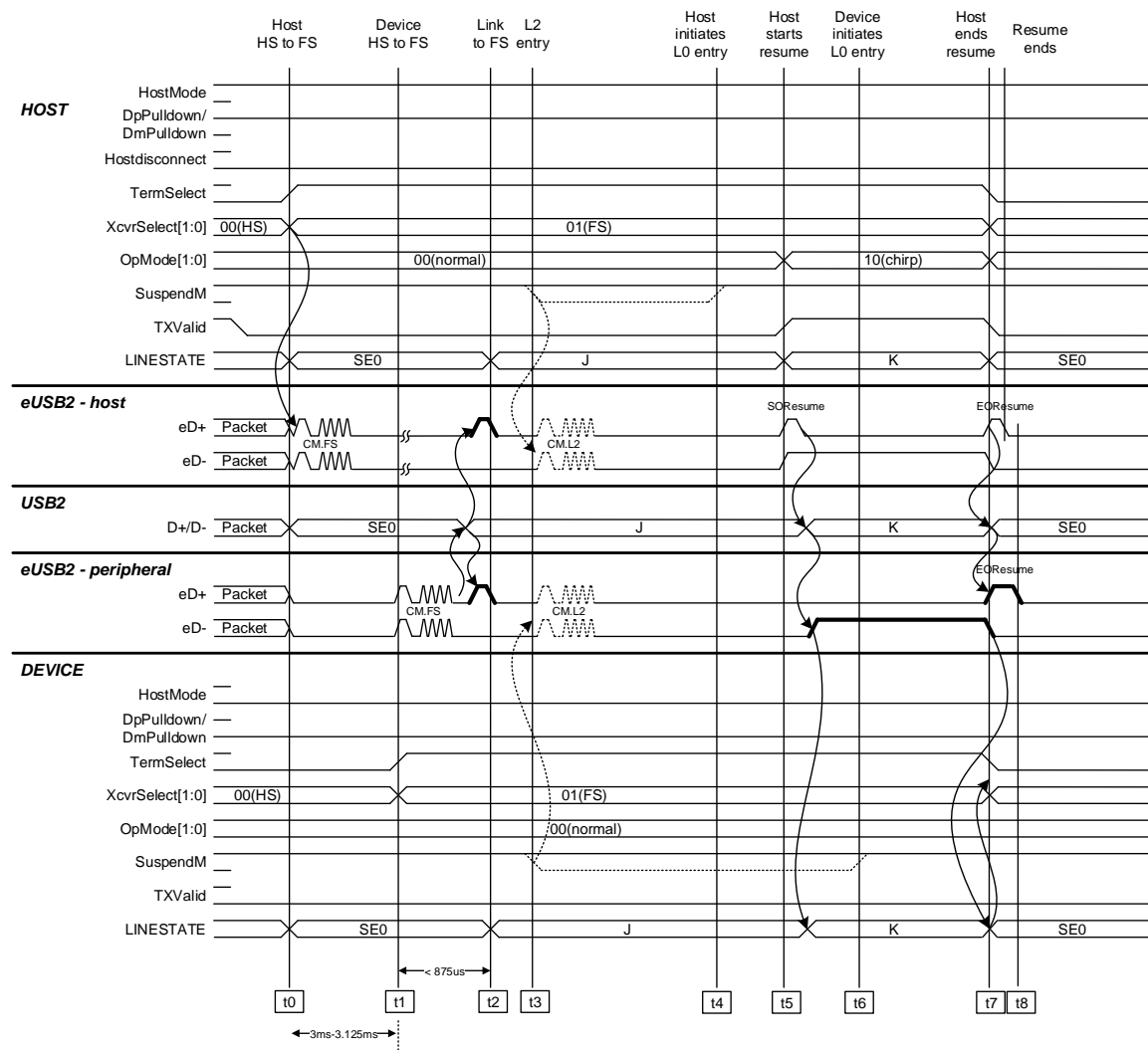


Figure 5-32: HS Link L2 entry and Resume

- t0:
- eDSPr initiates suspend, sends CM.FS, starts 4ms timer
  - Host repeater at its UDSP removes HS terminations
- t1:
- eUSPr sends CM.FS after 3ms to check for reset or suspend
  - Peripheral repeater starts  $T_{PR\_RESET\_FROM\_HS}$  timer and at its UUSP removes HS terminations and applies J pull-up. Before observing J at UUSP, the peripheral repeater remains in HS bus state mapping at eDSPp.
- t2:
- Peripheral repeater detected Idle J at UUSP before  $T_{PR\_RESET\_FROM\_HS}$  expired indicating suspend entry and sends a pulse to eUSPr and enter FS mapping.
  - eUSPr updates LineState to J
  - eUSPh also sends a pulse to eDSPr in case it observes J pull up; eUSPh enters FS mapping mode
  - eDSPr updates LineState to J, eDSPr stops 4ms timer
- t3:
- eDSPr controller may or may not assert suspend; eDSPr sends CM.L2 if SuspendM asserted

- eUSPr controller may or may not assert suspend; eUSPr sends CM.L2 if SuspendM asserted
- t4:
- eDSPr controller initiates L0 entry
- t5:
- eDSPr starts sending Resume,
  - eUSPh detects eSE1 followed by logic '1' on eD-; eUSPh stops FS mapping mode
  - UDSP sends Resume on USB 2.0 bus after eSE1 followed by logic '1' on eD- is detected.
  - eDSPp enters repeat mode after detecting K on USB 2.0 bus and drives eD- to logic '1'
  - eUSPr updates LineState to K
- t6:
- eUSPr controller de-asserts suspend if required
- t7:
- eDSPr ends Resume with EOResume
  - eDSPp exits repeat mode after observing EOP on USB 2.0 bus and sends T<sub>STROBE</sub> on eD+ line
  - eDSPp and eUSPh both enter HS mode within 2LS bit times
- t8:
- Resume completes. eUSBr configures itself to HS mode upon eSE0 with receiver termination enabled and input in squelched condition.



### 5.5.18 HS Remote Wake and Resume from L2

Link exiting L2 with a peripheral wake and host Resume is shown in Figure 5-33.

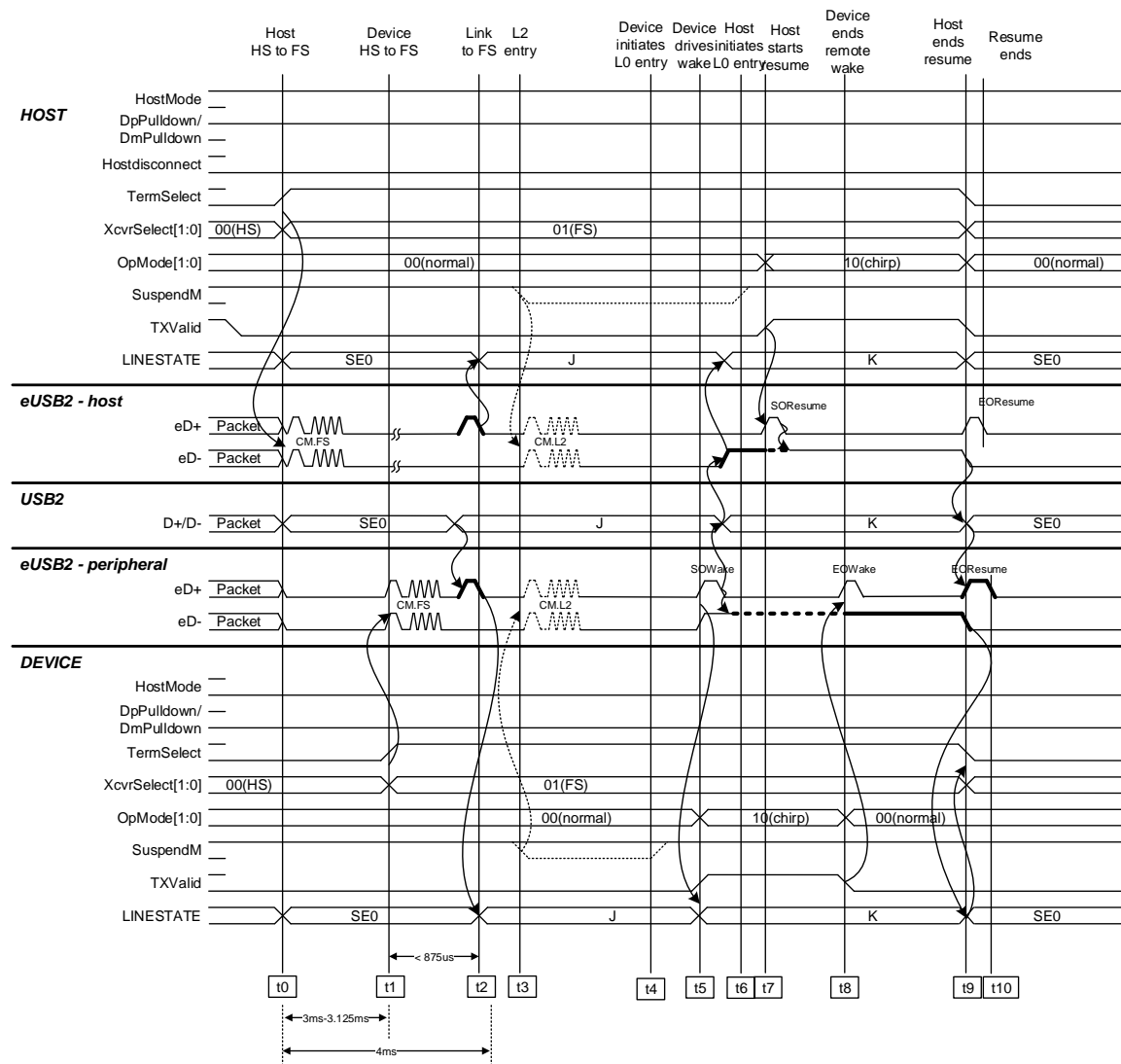


Figure 5-33: HS Link device wake and host Resume

t0-t3:

- HS Link L2 entry.

t4:

- eUSPr controller initiates L0 entry

t5:

- eUSPr starts Remote Wake with SOWake
- eDSPp detects eSE1 followed by a logic '1' on eD-, detects it as a remote-wake signal; UDSP sends remote-wake on USB 2.0 bus
- eDSPp remains in FS mapping mode and maps K on USB 2.0 bus as a driven logic '1' on eD-
- eUSPh enters repeat mode after detecting a K on the USB 2.0 bus and drives eD- to logic '1'

- eDSPr reflects it as Resume K and updates LineState; after observing USB 2.0 bus state change from J to K
- t6:
- eDSPr initiates L0 entry
- t7:
- eDSPr starts sending Resume
  - eUSPh detects eSE1 followed by logic '1' on eD-; eUSPh stops repeating mode
  - UDSP sends Resume on USB lines after eSE1 followed by logic '1' on eD- is detected.
- t8:
- eUSPr stops sending remote-wakeup
  - eDSPp after detecting a logic '0' to logic '1' on eD+, stops FS mapping mode and enters repeating mode
  - UDSP stops driving K on USB 2.0 bus
  - eDSPp sends K on USB 2.0 bus in repeating mode on eD-
- t9:
- eDSPr ends Resume with EOResume
  - eDSPp exits repeat mode after observing EOP on USB 2.0 bus and sends T<sub>STROBE</sub> on eD+
  - eDSPp and eUSPh both enter HS mode within 2LS bit times
- t10:
- Resume completes. eUSBr configures itself to HS mode upon eSE0 with receiver termination enabled and input in squelched condition.

### 5.5.19 HS Link wake and without Resume from L2

Figure 5-34 illustrates the scenario where a device initiates a wake from L2, however, host Resume is not triggered

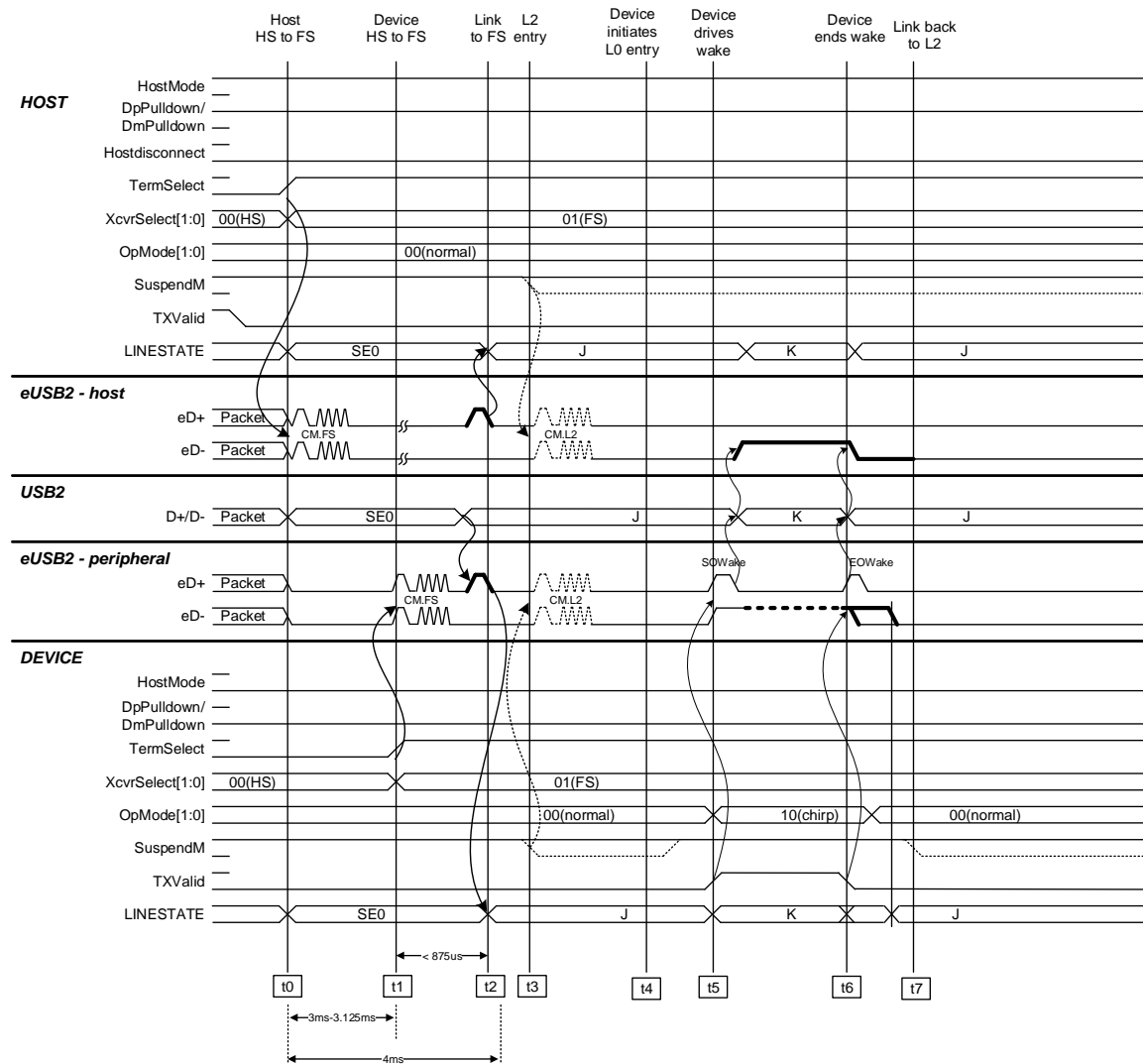


Figure 5-34: HS Link device wake without host Resume

t0-t4:

- HS Link L2 entry.

t5:

- eUSPr initiates remote-wakeup.

t6:

- eUSPr stops sending remote-wakeup
- UUSP stops driving K on USB 2.0 bus
- eDSPp enters FS mapping mode, and maps USB J as undriven eSE0 on eUSB2 bus. Note: K may continue to be presented on eD- after the completion EOWake before transiting to Idle J. In this case, the K to J transition shall not be declared as a host Resume (host Resume shall be a K to SE0 EOResume).
- eUSPh keeps forwarding J on USB 2.0 Bus as a data J. It starts the  $T_{SE0\_FILTER}$  SE0 filter timer.

t7:

- The  $T_{\text{SE0\_FILTER}}$  SE0 filter timer expires; it stops driving eD- line and moves back to FS mapping mode.
- Link is back to L2.

### 5.5.20 HS Link disconnect during L2 entry

Figure 5-35 illustrates the scenario where a device is disconnected during L2 entry.

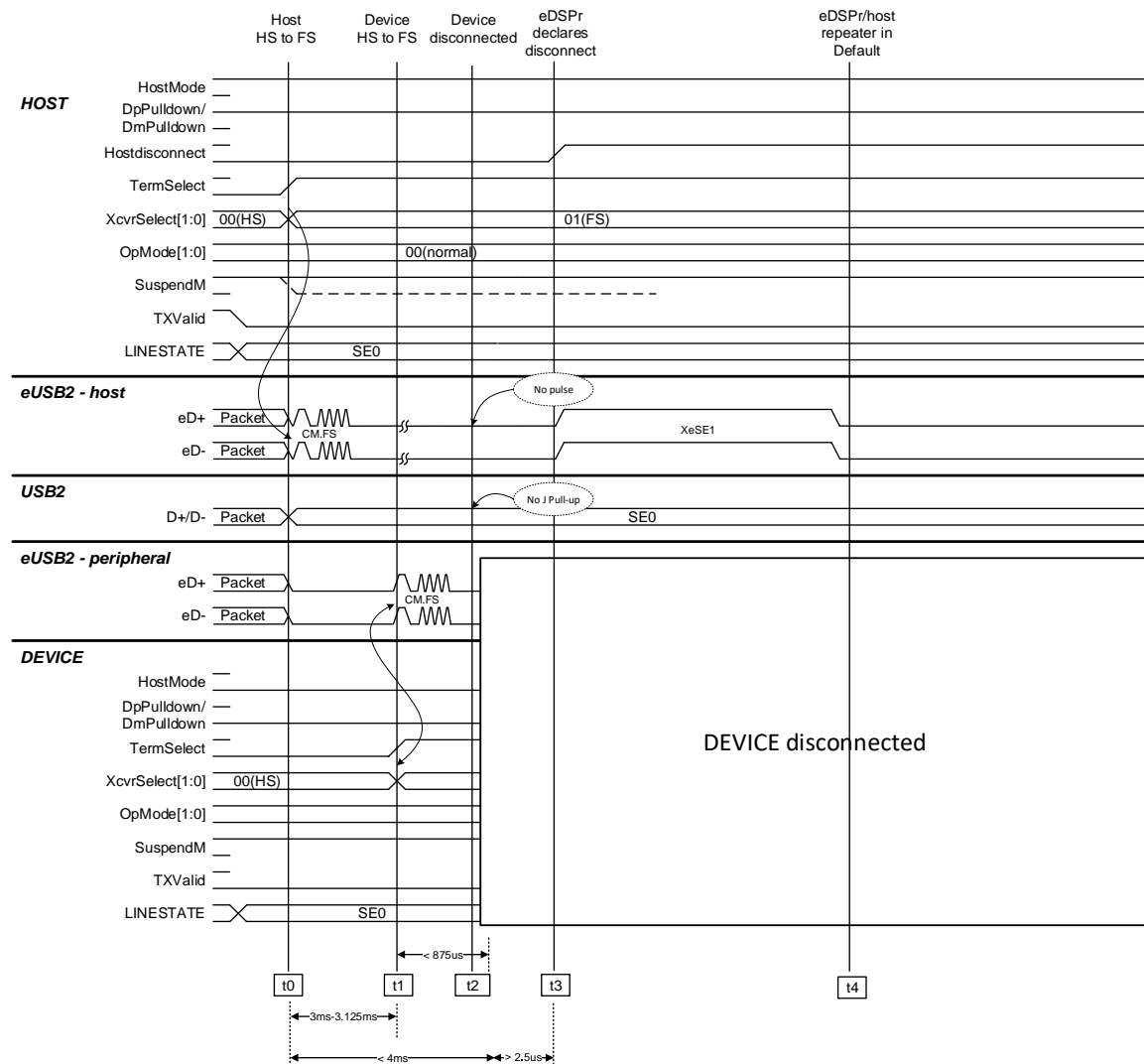
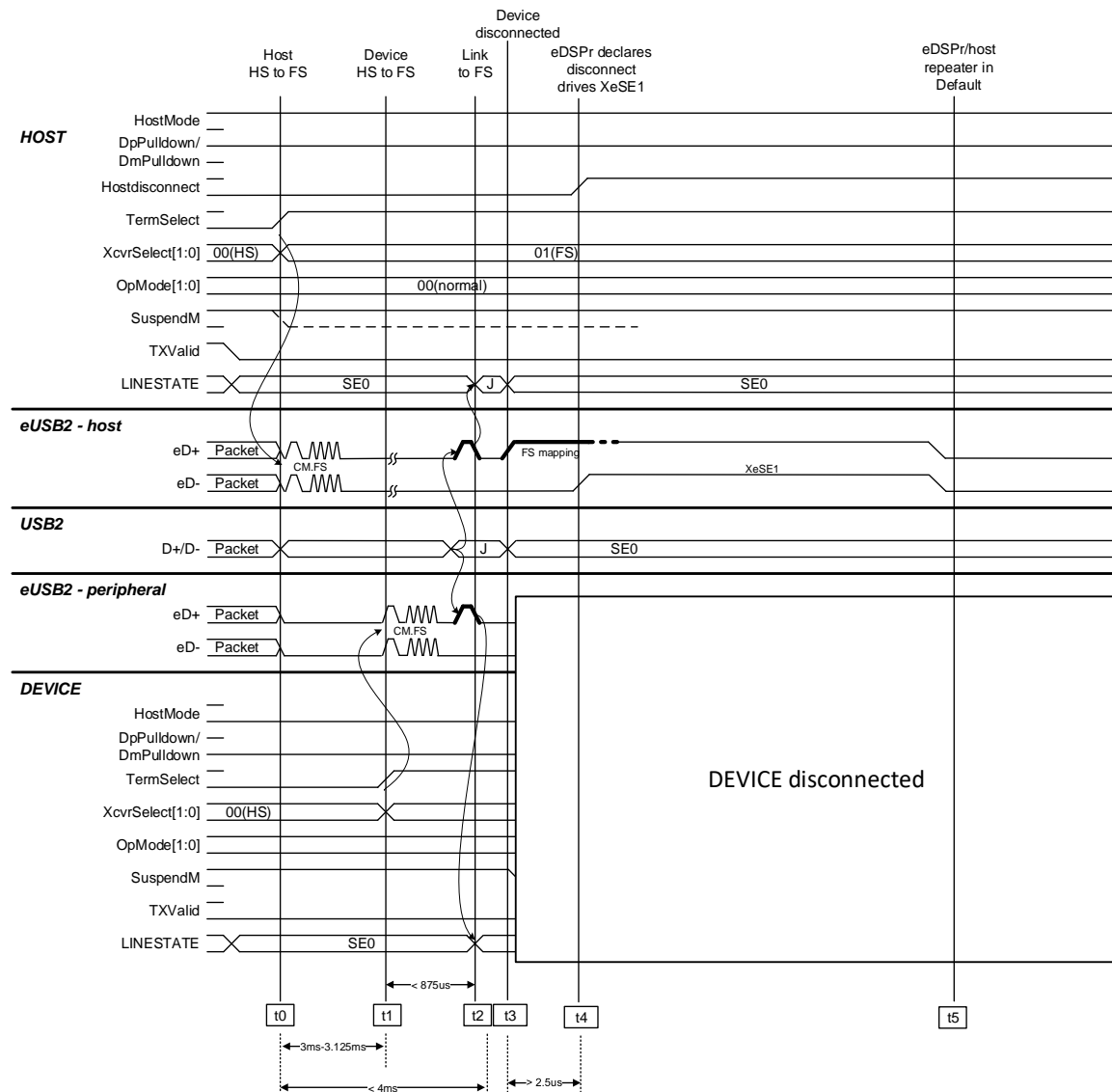


Figure 5-35: HS Link disconnect during L2 entry

- t0:
- eDSPr initiates suspend, sends CM.FS, starts 4ms timer.
  - eUSPh directs its UDSP to remove HS terminations.
- t1:
- eUSPr sends CM.FS after 3ms to check for reset or suspend.
  - eDSPp directs its UUSP to remove HS terminations and applies J pull up.
- t2:
- Peripheral disconnected on USB 2.0 bus before a J pull up could be applied.
- t3:
- UDSP never sees a J, thus eUSPh never sends a pulse; eUSPh is not completely in FS mode, thus it is not performing any disconnect detection.
  - After 4ms, disconnect recovery timer expires. eDSPr observes the eUSB2 bus state remain as eSE0 for more than 2.5us with no acknowledgement pulse received; eDSPr declares disconnect and sends Port Reset to eUSPh.
- t4:
- Link transition to Default for reconfiguration.

### 5.5.21 HS Link disconnect in L2 (before CM.L2)

Figure 5-36 illustrates the scenario where a device is disconnected in L2 entry before the CM.L2.



**Figure 5-36: HS Link disconnect in L2 entry (before CM.L2)**

- t0:
- eDSPr initiates suspend, sends CM.FS, starts 4ms timer.
  - eUSPh directs its UDSP to remove HS terminations.
- t1:
- eUSPr sends CM.FS after 3ms to check for reset or suspend.
  - eDSPp directs its UUSP to remove HS terminations and apply J pull up.
- t2:
- UDSP sees a J, thus eUSPh sends a pulse; eUSPh enters FS mode, enables its FS mapping.
  - eDSPr receives the pulse, before the 4ms timer expires, updates LineState to J.
- t3:

- Peripheral disconnected on USB 2.0 bus; eUSPh drives eD+ to '1' based on FS mapping.
- t4:
- eDSPr receives a '1' on eD+, updates LineState to SE0, asserts hostdisconnect, and issues Port Reset.
- t5:
- Link transition to Default for reconfiguration.

### 5.5.22 HS Link disconnect in L2 (during CM.L2)

Figure 5-37 illustrates the scenario where a device is disconnected in L2 entry after the CM.L2.

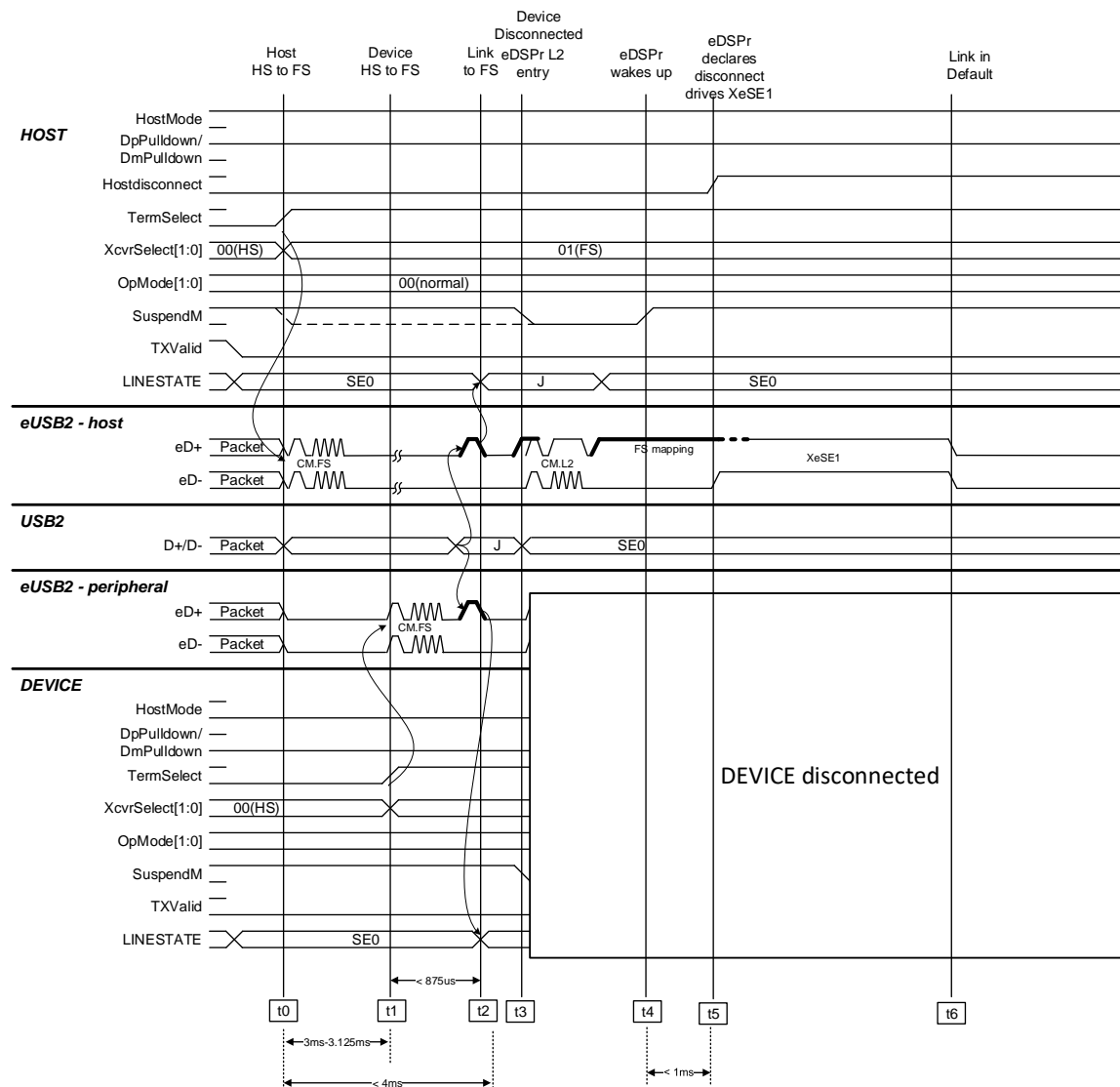


Figure 5-37: HS Link disconnect in L2 entry (during CM.L2)

- t0:
- eDSPr initiates suspend, sends CM.FS, starts 4ms timer
  - eUSPh directs its UDSP to remove HS terminations
- t1:
- eUSPr sends CM.FS after 3ms to check for reset or suspend.
  - eDSPp directs its UUSP to remove HS terminations and apply J pull up.

- t2:
- UDSP sees a J, thus eUSPh sends a pulse; eUSPh enters FS mode, enables its FS mapping.
  - eDSPr receives the pulse, before the 4ms timer expires, updates LineState to J.
- t3:
- eDSPr controller observes J and asserts suspend.
  - eDSPr sends CM.L2.
  - Device disconnect occurs the same time as CM.L2. Hence, CM.L2 coincide with logic '1' on eD+ (indicating SE0 on D+/D-).
  - eUSPh stops driving logic '1' on eD+ to service CM.L2 (observes eSE1 SCM of CM.L2).
  - eUSPh redrives logic '1' on eD+ indicating device disconnect.
- t4:
- eDSPr exits L2 as directed by its controller to service device disconnect.
- t5:
- eDSPr transmits XeSE1 to its associated repeater as Port Reset.
- t6:
- Link transition to Default for reconfiguration.



## 6 Register Access Protocol

The register access protocol (RAP) is optional. It consists of CM.RAP followed by any of four different register operations described in this chapter. The transmission of CM.RAP adheres to the rules defined in Section 3.3.8. CM.RAP is defined with the assumption of an error free link. Any error recovery of RAP operations is implementation specific. The data integrity of the register operation may be facilitated through register read back. RAP supports control and configuration in the following two operation modes.

- In repeater mode, for an eUSB2 port to access the register space in its associated repeater in Default.
- In native mode, for an eDSPn to access the register space in an eUSB2 peripheral port.

Register access protocol (RAP) is optional, it is system implementation's responsibility to determine if RAP is required.

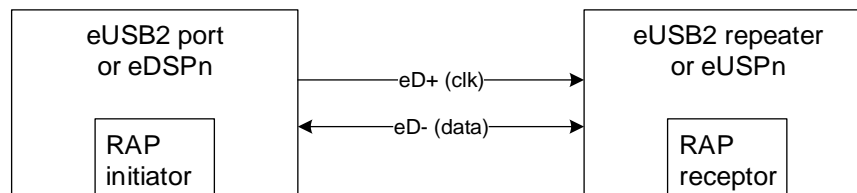
The RAP bus is a point to point interconnect based on eD+ and eD-. The RAP clocking architecture is forwarded clock. The electrical requirement of the RAP is compatible with LS/FS operation defined in Section 7.2.

The RAP supports 6-bit addressing with 2-bit command for following byte operations.

- Read: single-byte read.
- Write: single byte write.
- Set: to perform bit-wise logic "OR" with the registered data.
- Clear: to perform bit-wise reset to the registered data with the mask.

### 6.1 RAP Bus Definition and Operation

An example RAP configuration is shown in Figure 6-1. A RAP initiator is a port initiating the register access, and it is always implemented in an eUSB2 port. A RAP receptor is a port that has its register space implemented, and it is either implemented in an eUSB2 device, or in an eUSB2 repeater.



**Figure 6-1: RAP Block Diagram**

The RAP bus shares the eUSB2 bus. It can only be initiated in Default before Port/Repeater Configuration. Note that it is the responsibility of the RAP initiator to make sure that the RAP receptor is ready for RAP operations after power up.

As shown in Figure 6-1, RAP bus is constructed based on eD+/eD-. eD+ is repurposed to carry the forwarded clock. eD- is repurposed to carry half-duplex bi-directional data. The bus clocking and operation shall meet the following requirements.

- A RAP initiator shall supply a forwarded clock to a RAP receptor for data sampling, command decoding and its associated data processing.
- The RAP bus clocking shall be based on single data rate with the data transmitted on the rising edge of the clock and received and sampled on the falling edge of the clock. This shall apply to both the RAP initiator and receptor. (Refer to Section 5.3 for timing requirements).
- The timing requirements of RAP operations shall be identical to control message as defined in Section 3.3.8.

- The RAP command shall follow immediately after the end of CM.RAP.
- The data bus turnaround time for data read shall be between three to sixty-four clock cycles. A RAP receptor shall first drive one cycle of logic '1' and follow with the data.
- The transmission of the RAP shall start with CM.RAP and follow with the RAP command, the register address, and if the command is read, write, clear or set the data. The bit order shall be least significant bit first. Shown in Figure 6-2 is a general RAP format. Note that there is no burst RAP operation. Each RAP operation shall start with CM.RAP.
- For write operation, the RAP initiator shall drive logic '0' at eD- for two clock cycles after the last bit of data (d7).
- For read operation, the RAP initiator shall drive logic '0' at eD- for the first cycle of the 3~64 turnaround clock cycle and switch to pull-down starting from the second cycle. The turnaround begins immediately after the last bit of address (a5). The RAP receptor shall drive logic '0' at eD- for one clock cycle after the last bit of data (d7) is transmitted before disabling its transmitter with the second clock cycle.
- The RAP initiator shall wait for  $T_{CMB2B}$  (end to start) between consecutive RAP operations.
- If ACK is not received, the RAP initiator shall not proceed with RAP command and shall wait for  $T_{CMRETRY}$  to retry CM.RAP. There is no limit in how many times an initiator may retry. It is implementation specific.

CM_CLK	0	1	...	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
CM.RAP					Operand		Address					Data								idle		
CM.15					c0	c1	a0	a1	a2	a3	a4	a5	d0	d1	d2	d3	d4	d5	d6	d7	0	0

(a). Write/Set/Clear

CM_CLK	0	1	...	9	10	11	12	13	14	15	16	17	N = 3~64 cycles	N +	N +	N +	N +	N +	N +	N +	N +	N +	N +	N +	N +	N +	N +
CM.RAP					Read		Address						Turn around	S	Data								idle				
CM.15					1	0	a0	a1	a2	a3	a4	a5	000...0	1	d0	d1	d2	d3	d4	d5	d6	d7	0	0			

(b). Read

Figure 6-2: RAP Format

## 6.2 RAP Command and Features

The RAP supports four register operands defined in Table 6-1.

Table 6-1: The RAP Command Definition

CMD (b1~0)	Operand	Description
00	Write	Data is written to the register address
01	Read	Data is read from the register address
10	Clear	Active high bit-wise clear with the data on the register address.
11	Set	Bit-wise OR with the data on the register address

Example of register operations are shown in Figure 6-3 to Figure 6-6. Note: the time scales between CM.RAP and the rest of the register operation are not drawn in proportion.

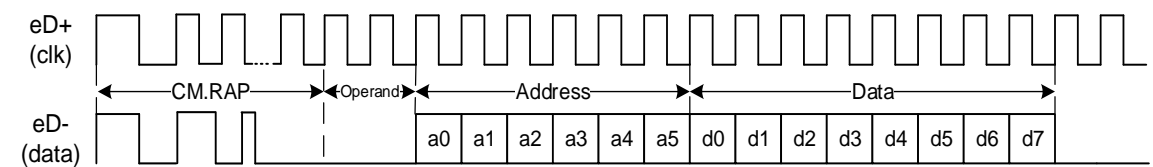


Figure 6-3: RAP Format: Write

An example of a read operation is shown in Figure 6-4.

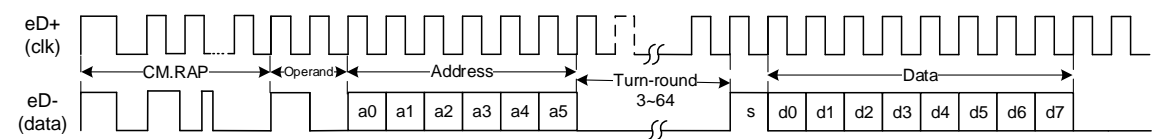


Figure 6-4: RAP Format: Read

An example of a clear operation is shown in Figure 6-5.

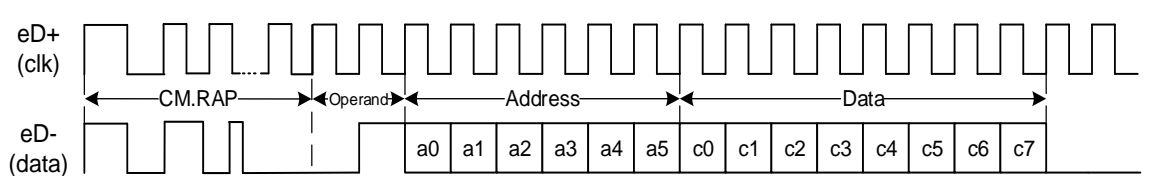


Figure 6-5: RAP Format: Clear

An example of a set operation is shown in Figure 6-6.

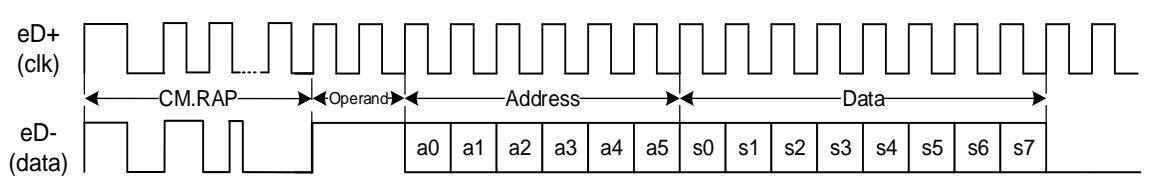


Figure 6-6: RAP Format: Set

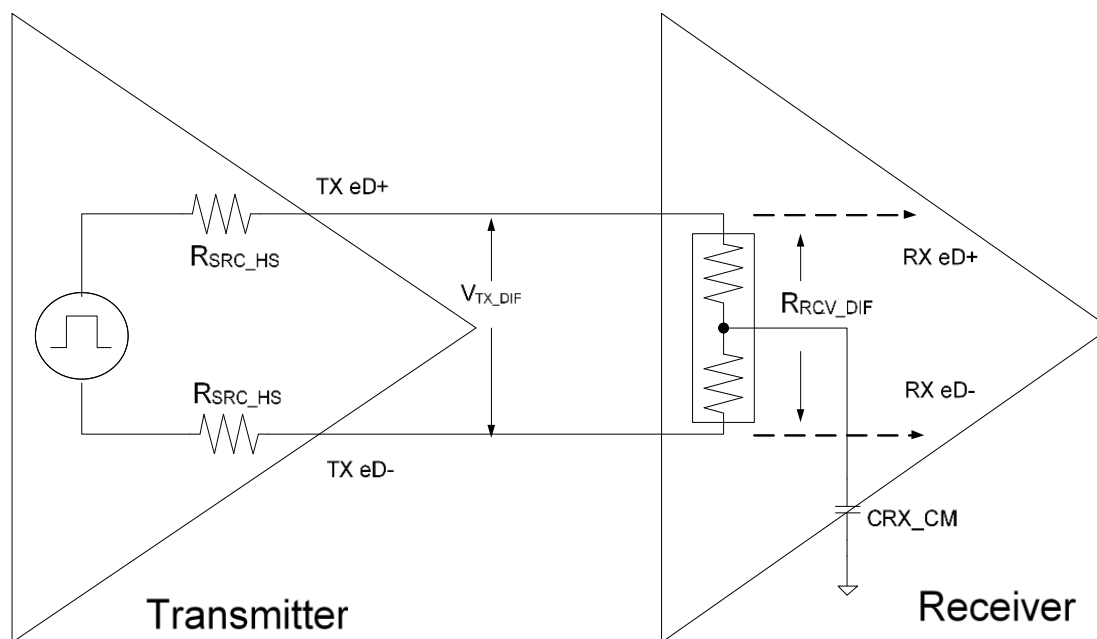
## 7 Electrical Specifications

This chapter describes the electrical specification of eUSB2.

### 7.1 High-Speed

Figure 7-1 shows an example of an eUSB2 transceiver circuit.  $R_{SRC\_HS}$  is the transmitter source termination.  $V_{TX\_DIF}$  is the peak differential swing across the Tx eD+ and eD- pads.  $R_{RCV\_DIF}$  represents the optional receiver differential termination.  $C_{RX\_CM}$  is an on-die capacitor, which is recommended to suppress AC common mode fluctuation seen by the receiver. The fact that eUSB2 is a half-duplex interconnect where transmitter and receiver share the pad are omitted from the drawing in Figure 7-1.

The high-speed transceiver implements low swing differential signaling. The transmitter is required to be source terminated to deliver good signal integrity. The receiver could be differentially terminated or un-terminated. The requirement for receiver termination depends on the use case and channel characteristics. Receiver termination is a requirement for repeater mode of operation but optional for native mode.



**Figure 7-1: Example eUSB2 Transmitter and Receiver Circuit Structure**

It is important to constrain the source impedance mismatch,  $\Delta R_{SRC}$ , between Tx eD+ and eD-. The mismatch will manifest itself into common mode voltage variation which impacts both receiver functionality and system EMI performance.

The eUSB2 receiver circuit is required to extract the clock information from the incoming data stream and perform data recovery. There is no requirement to implement common clocking architecture for 2 eUSB2 devices. The clock source inaccuracy shall be less than +/- 500 ppm as defined in USB 2.0. Spread spectrum clocking is not allowed.

The squelch circuit is implemented as an amplitude envelope detection circuit to differentiate between valid signal and wire noise. It is also used by the repeater to perform data traffic flow control. Therefore, a robust squelch circuit design is critical to guarantee correct functionality.

### 7.1.1 High-Speed Tx Electrical Specification

This section describes values at the TX pad.

**Table 7-1: High-Speed Transmitter DC Specifications**

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmit differential (terminated)	$V_{TX\_DIF\_TERM}$	165		245	mV	1,5
Transmit differential (un-terminated)	$V_{TX\_DIF\_UNTERM}$	360		440	mV	2,5
Transmit common mode	$V_{TX\_CM}$	170		230	mV	3,6
Transmit source termination impedance	$R_{SRC\_HS}$	32	40	48	$\Omega$	6
Source impedance mismatch	$\Delta R_{SRC\_HS}$			4	$\Omega$	4,5

Notes:

- 1) The transmitter must maintain the specified differential swing after accounting for the transmit voltage supply and source termination variation at both eD+ and eD-. An ideal 80 $\Omega$  Rx differential termination is used as the test load.
- 2) The transmitter must maintain the specified differential swing after accounting for the transmit voltage supply and source termination variation at both eD+ and eD-, an 80k $\Omega$  differential termination is used as the test load.
- 3) The specified number does not include AC noise component.
- 4) The source impedance mismatch between eD+ and eD- shall not vary more than the specified max value. This impedance mismatch could result from process random variation, systematic layout offset and other sources of error.
- 5) The specified numbers are Informative.
- 6) The specified numbers are Normative.

**Table 7-2: High-Speed Transmitter AC Specifications**

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmit CM AC (50MHz-480MHz)	$V_{TX\_CM\_AC}$			30	+/- mV <sub>PEAK</sub>	1,3
Transit rise and fall time (20%-80%)	$T_{RISE\_FALL\_TRM\_HS}$	100			ps	1,3
Transmit rise/fall mismatch				25	%	1,2

Notes:

- 1) Defined under an ideal 80 $\Omega$  Rx differential termination with maximum supply voltage variation.
- 2) Rise/fall mismatch = absolute delta of (rise – fall time) / (average of rise and fall time).
- 3) This parameter is informative, not normative.

### 7.1.2 High-Speed Rx Electrical Specification

**Table 7-3: High-Speed Receiver DC Specifications**

Parameter	Symbol	Min	Typ	Max	Units	Notes
Receive common mode range	$V_{RX\_CM}$	120		280	mV	1,4
Receive center-tapped capacitance	$C_{RX\_CM}$	15		50	pF	informative
Differential receiver termination	$R_{RCV\_DIF}$	64	80	96	$\Omega$	2,4
Differential receiver termination (repeater)		72	80	88	$\Omega$	3,4
Squelch detect threshold (peak differential)	$V_{SQUELCH\_DIF}$	60		110	mV	4

Notes:

- 1) The number includes common mode variation due to Tx source impedance mismatch and GND shall be within 4% of VCC of each other at all times on both receive and transmit sites. However, it does not account for receiver AC common mode variation.
- 2) High-Speed differential receiver termination for native mode operation only
- 3) A tighter termination tolerance is defined for repeater mode operation to minimize accumulated jitter when propagating downstream through the repeater.
- 4) This parameter is normative.

**Table 7-4: High-Speed Receiver AC Specifications**

Parameter	Symbol	Min	Typ	Max	Units	Notes
Receiver AC common mode (50MHz-480MHz)	$V_{CM\_RX\_AC}$			60	+/-mVpk	informative

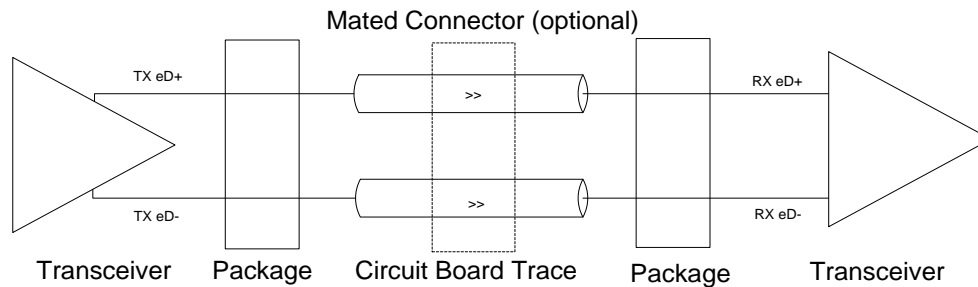
### 7.1.3 High-Speed Signal Pad Capacitance Recommendation

**Table 7-5: Capacitance (Informative)**

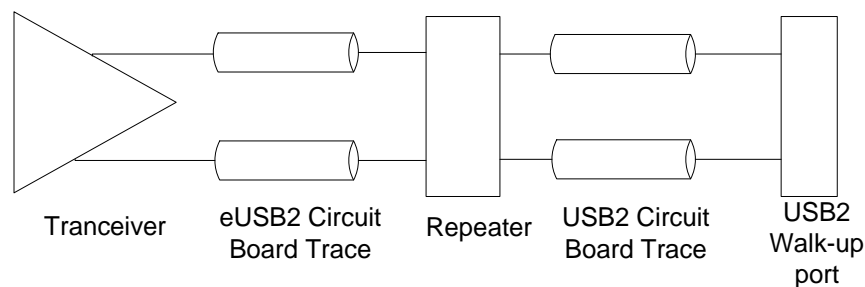
Parameter	Symbol	Min	Typ	Max	Units	Note
Tx Pad Capacitance	$C_{TX}$			2.5	pF	
Rx Pad Capacitance	$C_{RX}$			2.5	pF	

### 7.1.4 High-Speed Channel Requirement

Native mode and repeater mode channel topologies are shown in Figure 7-2 and Figure 7-3. The informative specifications are summarized in Table 7-6.



**Figure 7-2: Native Mode Channel Topology**



**Figure 7-3: Repeater Mode Channel Topology**

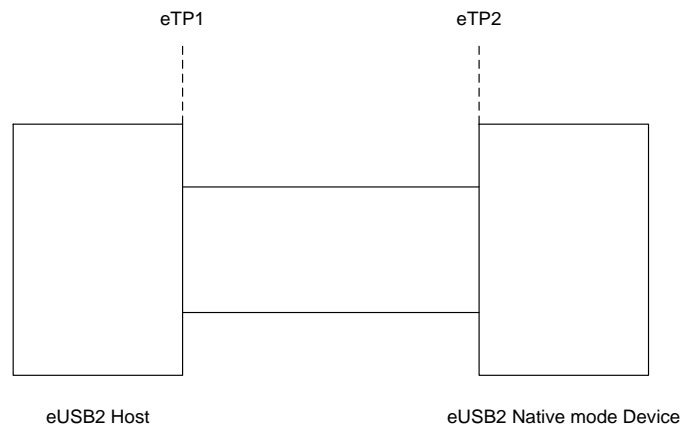
**Table 7-6: Channel Specification (normative)**

Parameter	Symbol	Min	Typ	Max	Units	Note
Trace Differential Impedance	$Z_{DIFF}$		85		$\Omega$	
Trace Differential Impedance Tolerance	$\Delta Z_{DIFF}$			15	%	
Host-to-device insertion loss, Native Mode	$IL_{NATIVE}$			-1.7	dB	1,2
Host-to-repeater insertion loss, Repeater Mode	$IL_{H2RPT}$			-1.2	dB	1,3
Repeater-to-connector insertion loss, Repeater Mode	$IL_{RPT2CON}$			-2	dB	1,3

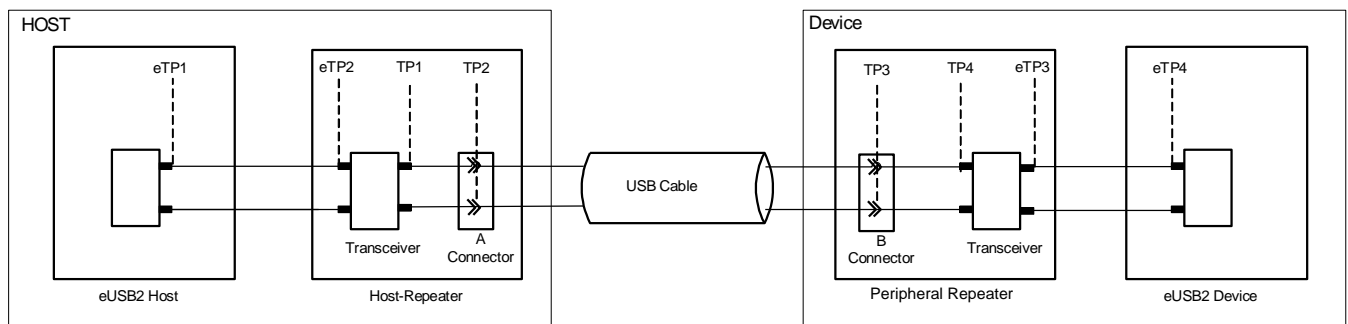
Notes:

- 1) The number is specified at 240MHz frequency.
- 2) Refer to Figure 7-2 for the topology setup.
- 3) Refer to Figure 7-3 for the topology setup.

### 7.1.5 High-Speed Eye Diagram and Jitter Allocation



**Figure 7-4: Measurement Plane for Native Mode**



**Figure 7-5: Measurement Plane for Repeater Mode**

Figure 7-6 defines 4 additional test planes<sup>1</sup> eTP1, eTP2, eTP3 & eTP4. Definition of TP2 and TP3 remains the same as specified by USB 2.0, Section 7.1.2.2.

- eTP1 and eTP2 are the points where the IC pins of the eUSB2 Host and eUSB2 host repeater are respectively soldered to the circuit board.
- eTP3 and eTP4 are the points where the IC pins of eUSB2 Repeater and eUSB2 Device are respectively soldered to the circuit board.

Two additional templates have been defined by the eUSB2 specification. eUSB2 jitter budgeting assumes jitter at TP2 & TP3 remain the same as defined in USB 2.0. USB 2.0 Template1 & Template 4 are normative specifications. eUSB2 Template 1 & eUSB2 Template 2 are informative specifications only during repeater mode. Conformance to eUSB2 Template 1 and 2 is required for eUSB2 Host and eUSB2 device in native mode.

**eUSB2 Template 1:** Transmit waveform requirement for an eUSB2 host measured at eTP1.

**eUSB2 Template 2:** Receiver sensitivity requirements for an eUSB2 device when signal is applied at eTP2 (native mode) or eTP4 (repeater mode).

*Note1: eUSB2 templates have been defined assuming signal flow where eUSB2 Host in transmit mode is transmitting to eUSB2 device in receive mode. Host repeater's eUSPh is in receiving*

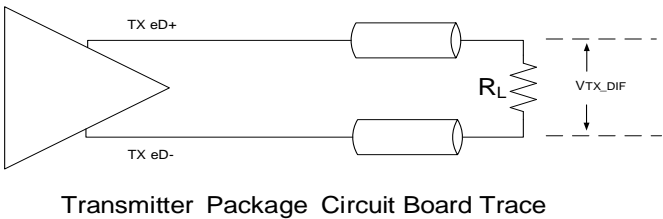


*mode & D+/D- side in transmit mode while Peripheral repeater's eDSPp is in transmit mode & D+/D- side is in receiving mode. Jitter allocation for a repeater is 50ps.*

**7.1.5.1 eUSB2 Template 1**

Figure 7-6 defines the setup for the simulation/measurement. The circuit board trace should be kept less than one inch, and  $R_L$  differential termination resistor should be  $80k\Omega \pm 1\%$  for unterminated mode and  $80\Omega \pm 1\%$  for terminated mode.

Figure 7-7 shows the transmit waveform requirement for an eUSB2 host measured at eTP1. It should be read together with Table 7-7 or Table 7-11 depending on the application. Table 7-8 and Table 7-9 define V-T limits for un-terminated and terminated load respectively.

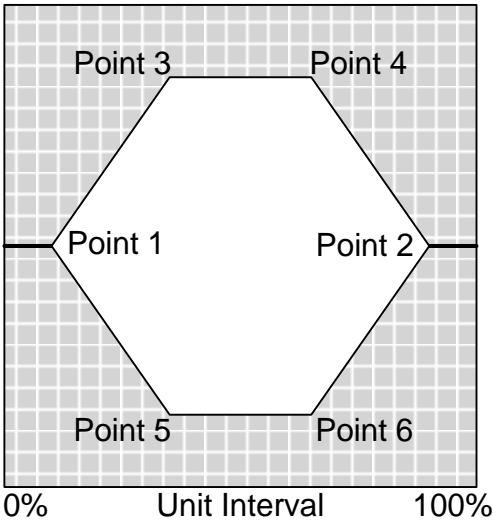


**Figure 7-6: High-Speed Transmit Eye Diagram Test Setup**

**Table 7-7: High-Speed Transmit Eye Test Load Definition**

Termination	$R_L$
Terminated	$80\Omega$
Unterminated	$80k\Omega$

Note: for measurement at pin.



**Figure 7-7: eUSB2 Template 1 Eye Mask**

**Table 7-8: eUSB2 Template 1 V-T Table (Un-terminated)**

	<b>80k<math>\Omega</math> test load</b>	
	Voltage Level (eD+ - eD-)	Time (% of UI)
Point 1	0V	10
Point 2	0V	90
Point 3	180mV	35
Point 4	180mV	65
Point 5	-180mV	35
Point 6	-180mV	65

**Table 7-9: eUSB2 Template 1 V-T Table (Terminated)**

	<b>80<math>\Omega</math> test load</b>	
	Voltage Level (eD+ - eD-)	Time (% of UI)
Point 1	0V	4
Point 2	0V	96
Point 3	150mV	35
Point 4	150mV	65
Point 5	-150mV	35
Point 6	-150mV	65

### 7.1.5.2 eUSB2 Template 2

Receiver eye patterns specify the minimum and maximum limits, as well as limits on timing jitter, measured at the  $80\Omega$  differential test load at the end of the channel. Figure 7-8 shows the Receiver sensitivity requirements for an eUSB2 device when signal is applied at eTP2 (Native mode), and for an eUSB2 device with repeater when signal is applied at eTP4 defines the V-T limits of the eye mask.

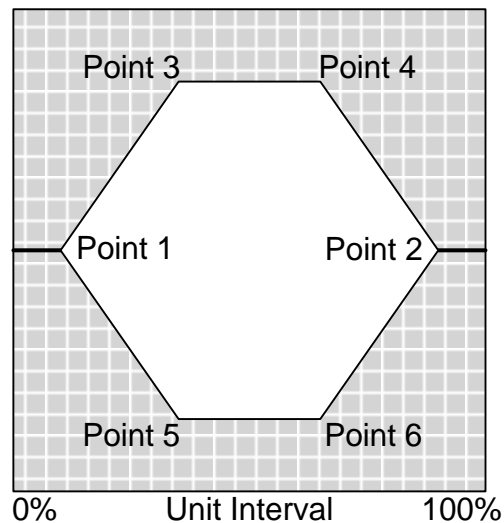


Figure 7-8: eUSB2 Template 2 Eye Mask

Table 7-10: eUSB2 Template 2 V-T Table

	Voltage Level (eD+ - eD-)	Time (% of UI)
Point 1	0V	21.2
Point 2	0V	79.8
Point 3	110mV	41.2
Point 4	110mV	58.8
Point 5	-110mV	41.2
Point 6	-110mV	58.8

### 7.1.5.3 High-Speed Repeater Mode Jitter Allocation

USB 2.0 Tx and Rx Eye Diagram compliance requirements dictate the total jitter allocation available to the transmitter, repeater and the channel.

A redriver is recommended if the channel topology between the SoC and walk-up port is meeting the specification outlined in Section 6.1.4. For applications that require channel route beyond the specification, a retimer is required.

A redriver is required to comply with Template 1 (in the case of host repeater) & Template 4 (in the case of peripheral repeater) as defined in USB 2.0, Section 6.1.2.2, when repeater signals

either to upstream or downstream. A detailed system level Jitter Budget is given in Table 7-11. The baseline for this jitter budget is maintaining the same jitter budget as TP2 & TP4 as defined in USB 2.0 Template 1 & Template 4. Note that this requirement does not apply to a retimer. A retimer should be treated like a typical USB 2.0 hub from jitter budgeting perspective.

**Table 7-11: System Level Jitter Budgeting with Host & Peripheral Redriver**

Jitter Source	Tj (ps)	UI (%)	Note
eUSB2 Tx	166.5	8	1
Host Channel	96	4.6	2
Host-Redriver	50	2.4	3
USB Cable	312.5	15	
Device Channel	208.3	10	2
Peripheral Redriver	50	2.4	3
Total	883.3	42.4	4,6

Notes:

1. Silicon TX jitter budget is informative.
2. Channel jitter is informative.
3. Repeater jitter is normative and measured during test mode using Test Packet.
4. Total jitter at eTP4 is informative.
5. Total jitter at TP2 & TP3 is normative and complies with USB 2.0 Template 1 & Template 3 as defined in USB 2.0.
6. Receiver must tolerate an additional 2.4% jitter.

## 7.2 Low-Speed/Full-Speed

Low-Speed/Full-Speed used single-ended CMOS signaling to communicate between the link partners. A relatively loose source termination is required if compared to High-Speed. The receiver is un-terminated. Limits are defined for rise and fall time to avoid excessive overshoot and undershoot observed at both the transmitter and receiver end.

### 7.2.1 Full-Speed/Low-Speed Electrical Specification

**Table 7-12: Low-Speed /Full-Speed DC Specifications for 1.0V +/- 10%**

Parameter	Symbol	Min	Typ	Max	Units	Notes
Supply Voltage for eD+/eD-	VCC	0.9	1.0	1.1	V	1, 2
Transmit single-ended output low	V <sub>OL</sub>			0.15 x VCC	V	
Transmit single-ended output high	V <sub>OH</sub>	0.85 x VCC		VCC	V	
Transmit output impedance	R <sub>SRC_LSFS</sub>	28		60	Ω	3
Input low voltage	V <sub>IL</sub>	-0.1		0.35* VCC	V	
Input high voltage	V <sub>IH</sub>	0.65 x VCC		1.05 x VCC	V	
Receive single-ended hysteresis voltage	V <sub>HYS</sub>	0.04 x VCC			V	

Notes:

- 1) VCC shall be within 150 mV (15%) of each other at all times on both receive and transmit sites
- 2) GND shall be within 40 mV (4%) of each other at all times on both receive and transmit sites
- 3) Shall be met up to V<sub>OL</sub> when driving low and above V<sub>OH</sub> when driving high

**Table 7-13: Low-Speed /Full-Speed DC Specifications for 1.2V +/- 10%**

Parameter	Symbol	Min	Typ	Max	Units	Notes
Supply Voltage for eD+/eD-	VCC	1.08	1.2	1.32	V	1, 2
Transmit single-ended output low	V <sub>OL</sub>			0.15 x VCC	V	
Transmit single-ended output high	V <sub>OH</sub>	0.85 x VCC		VCC	V	
Transmit output impedance	R <sub>SRC_LSFS</sub>	28		60	Ω	3
Input low voltage	V <sub>IL</sub>	-0.1		0.35* VCC	V	
Input high voltage	V <sub>IH</sub>	0.65 x VCC		1.05 x VCC	V	
Receive single-ended hysteresis voltage	V <sub>HYS</sub>	0.04 x VCC			V	

Notes:

- 1) VCC shall be within 180 mV (15%) of each other at all times on both receive and transmit sites
- 2) GND shall be within 48 mV (4%) of each other at all times on both receive and transmit sites  
Shall be met up to V<sub>OL</sub> when driving low and above V<sub>OH</sub> when driving high
- 3) To get better system performance try to match termination impedance as close as possible

**Table 7-14: Low-Speed /Full-Speed AC Specifications**

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmit rise and fall time (10%-90%)	T <sub>RISE_FALL_TRM</sub>	2		6	ns	1
Transmit rise/fall mismatch				25	%	2
eUSB2 to USB 2.0 repeater FS jitter to next transition	T <sub>e_to_U_DJ1</sub>	-6.0		+6.0	ns	3
repeater FS paired transition jitter in both directions	T <sub>DJ2</sub>	-1.5		+1.5	ns	4
eUSB receiver FS jitter tolerance	T <sub>RJR1</sub>	-15.5		+15.5	ns	5

Notes:

- 1) Measured with 2.5pF test load at eUSB2 device/eUSB2 repeater end and assuming 10-inch channel trace in between eUSB2 Host and eUSB2 repeater/eUSB2 device.
- 2) Rise/fall mismatch = absolute delta of (rise – fall time) / (average of rise and fall time).
- 3) USB 2.0 to eUSB2 repeater jitter to next transition follows USB 2.0 parameter T<sub>HDJ1</sub>
- 4) Relaxed relative to T<sub>HDJ2</sub> defined by USB 2.0
- 5) = abs(T<sub>JR1</sub>) – abs(T<sub>HDJ1</sub>) where T<sub>JR1</sub> and T<sub>HDJ1</sub> are defined by USB 2.0

### 7.3 Pull-down

A much stronger pull-down is defined for eUSB2 than USB 2.0. Pull-downs are used during device connect detect. It is also used to hold the line to ground when the link is idle.

**Table 7-15: Host and Device Pull-up and Pull-down Specification**

Parameter	Symbol	Min	Typ	Max	Units	Notes
Pull-down	$R_{PD}$	4		10	k $\Omega$	

### 7.4 Timing Specification

**Table 7-16: Timing Specification**

Parameter	Symbol	Tx Min	Tx Max	Rx Min	Rx Max	Units	Notes
The amount of time that an active driver shall remain idle for Back to back CM.	$T_{CMB2B}$	2				$T_{CM\_CLK}$	a) This is measured from end to start. b) CM.RAP included
The minimum duration eDSPr shall wait for CM retry if ACK is not received.	$T_{CMRETRY}$	10				us	Measured from the end of the previous CM to start of the retried CM
The amount of time that an active driver shall drive the wire to transition from non-SE0 to SE0, before letting the weak pull-down to hold the wire in SE0 idle, for low-speed and full-speed mode.	$T_{eSE0\_DR\_LSFS}$	20	70			ns	
The amount of time that an active driver shall drive the wire to transition from non-SE0 to SE0, before letting the weak pull-down to hold the wire in SE0 idle, for high-speed mode.	$T_{eSE0\_DR\_HS}$	1	4			HS UI	a) Shall be less than $T_{HSIPDOD}$ USB 2.0. b) Equal to USB 2.0 squelch delay to naturally drive back to SE0 while repeating. c) May be driven by SE TX or HS TX.

Parameter	Symbol	Tx Min	Tx Max	Rx Min	Rx Max	Units	Notes
1X Start of Control Message	$T_{CM\_eSE1\_1X}$	4	6			FS UI	For CM.FS, CM.L2 and CM.RAP
8X Start of Control Message	$T_{CM\_eSE1\_8X}$	32	48			FS UI	Only for CM.Test and CM.Reset.
Control message SE0 interval	$T_{CM\_eSE0}$	4	6			FS UI	
Control Message Internal Clock Period	$T_{CM\_CLK}$	2	3			FS UI	50+/-5% duty cycle
Control Message clock to data delay	$T_D$	0	25			ns	
Control Message setup time	$T_{SETUP}$	25				ns	
Control Message hold time	$T_{HOLD}$	25				ns	
Start of message to drive K for wake or Resume if CM.L2 was not issued to repeater	$T_{DR\_K\_eSE1\_1X}$	4	6			FS UI	Link could be in L0 during wake or Resume.
Start of message to drive K for wake or Resume if CM.L2 was issued to repeater	$T_{DR\_K\_eSE1\_8X}$	32	48			FS UI	If UTMI+ suspend is asserted and CM.L2 is send to repeater.
SE0 filter timer for USB 2.0 to eUSB2 bus state mapiing at the end of Remote Wake	$T_{SE0\_FILTER}$	3	8			us	
Time duration to end Port/Repeater Configuration upon detecting ACK	$T_{CONFIG\_CMPL}$				1	LS UI	
Time duration for transmitting XeSE1 and declaring reception of XeSE1	$T_{XeSE1}$	2	4	0.45		ms	2 ms needed for native device to announce graceful disconnect while host is in low power state with clocks off.

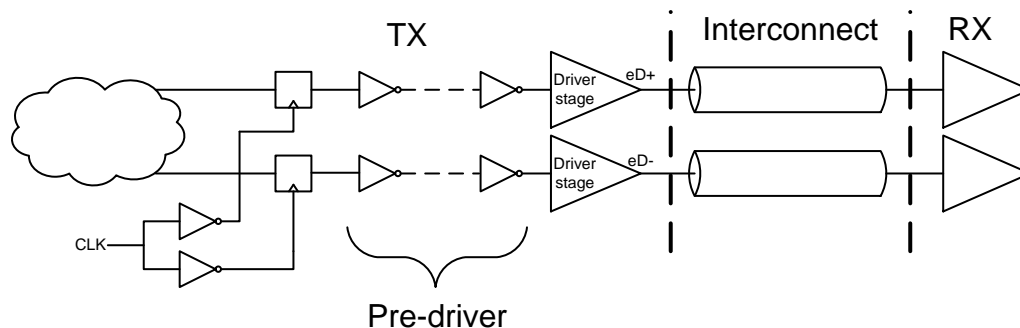


Parameter	Symbol	Tx Min	Tx Max	Rx Min	Rx Max	Units	Notes
Idle (eSE0) time after transmitting XeSE1 or Port/Repeater Configuration	T <sub>CONFIG_IDLE</sub>	1				LS UI	This is measured from the end of ACK
Time duration to declare reception of eSE1 for Native mode	T <sub>NATIVE_eSE1</sub>			1		FS UI	A short duration to allow declaring eSE1 reception and subsequently to block any signal transmission to allow a clean detection of eUSB2 protocol (i.e. XeSE1, CM message)
Time duration for declaring reception of XeSE1 for Native mode	T <sub>NATIVE_XeSE1</sub>			8		LS UI	
Time to detect HS disconnect by eDSPr/eDSPn in L0	T <sub>HSDISC_eSE1</sub>	NA	NA	16	50	HS UI	The reason for a short receive timing is to ensure disconnect detection within HS IPG (88UIs)
Delay for eUSPh to start signaling HS disconnect to eDSPr after end of $\mu$ SOF	T <sub>DISC_DLY</sub>		32			HS UI	Together with T <sub>HSDISC_eSE1</sub> , ensure disconnect detection within HS IPG (88UIs)
Duration of all strobes. End of Reset and Resume when going to HS, end of Wake from eUSPr, enable HS term during chirp from eUSPr and reporting DP pull up detection by repeater.	T <sub>STROBE</sub>	0.5	1.5	0.01		$\mu$ s	Roughly 1-2 LS UI
A setup time to sample Digital Ping	T <sub>DPING_SU</sub>			0.75		FS UI	

Parameter	Symbol	Tx Min	Tx Max	Rx Min	Rx Max	Units	Notes
Bus turnaround before analog ping	T <sub>TURNAROUND</sub>	12	24		10	HS UI	
Width of analog ping	T <sub>ANALOGPING</sub>	8	8	2	7	HS UI	RX timing is meant as a possible received width at the output of squelch receiver (Not as the input to eDSPn receivers)
Differential Skew	T <sub>eSE1_SKEW</sub>		500	600		ps	a) Measured at 50% cross-over point b) Receiver should be tolerant to differential skew up to the Rx min value at least. Guideline, not a requirement
Timer value for peripheral repeater to recognize USB 2.0 Bus Reset from Suspend entry	T <sub>PR_RESET_FROM_HS</sub>	NA	NA	64	128	µs	After the end of CM.FS, if a peripheral repeater detects its D+ pullup before timeout of this timer, it will enter L1 or L2 instead of USB 2.0 Bus Reset from HS.

## Appendix A. Skew and Rise/Fall time Break-ups

The skew and rise/fall time break-up for  $T_{SE\_SKEW}$  can be found below. Refer to Figure A-1 for skew sources in the communication channel.



**Figure A-1: eUSB2 Driver and Interconnect**

- Total skew: 340ps
  - Total driver induced skew=270ps.
    - Main driver induced skew=50ps + 60ps due to mismatch (+/- 3 sigma) = 110ps.
    - Pre-driver + Clock path skew + mismatch = 100ps + 60ps = 160ps.
  - Interconnect skew = 70ps (176 ps/inch FR4; or 70 ps/cm); Assuming 1cm mismatch in the trace for 20cm trace width.
- The rise and fall times must be between the min and max of  $T_{RISE\_FALL\_TRM}$  (2ns and 6ns) and matched to within max 25%. The following two cases show a 25% max matching for rise and fall times that are at the min and the max of  $T_{RISE\_FALL\_TRM}$ .
  - Case 1: eD+ rise @4.8ns & eD- rise @6ns.
  - Case 2: eD+ rise @2.5ns & eD- rise @2ns.
- Additional 160ps guard band assumed in current specification

## Appendix B. Hybrid Repeater

### B.1. Introduction

This specification introduces the definition of a repeater. A repeater is a mode that translates between eUSB2 signaling and USB 2.0 signaling and contains an eUSB2 port and a USB 2.0 port. Section 2.5 refers to the combination of the two repeaters allowing two eUSB2 ports to communicate with each other, with typically USB 2.0 receptacles in the middle. Figure B.1-1 and Figure B.1-2 illustrate such configurations.

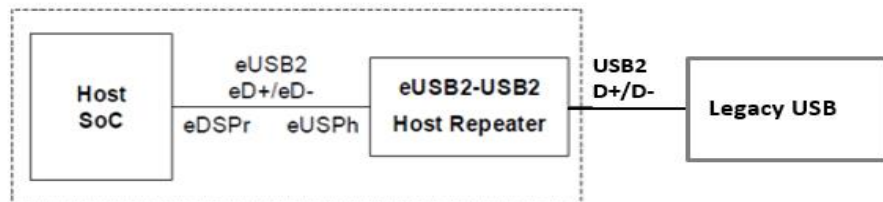


Figure B.1-1. Single Repeater Configuration

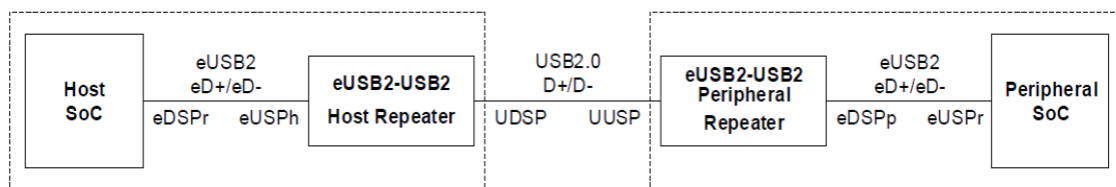


Figure B.1-2. Two Repeater Configuration

This appendix addresses applications requiring two eUSB2 ports to communicate with each other but not necessarily having traditional USB 2.0/eUSB2 wired systems (like USB 2.0 cables) between the two eUSB2 interfaces. This could be active logic, optical, wireless, or other connections. The configuration introduced here is called a Hybrid Repeater.

A Hybrid Repeater refers to a device hosting an upstream eUSB2 interface and a downstream eUSB2 interface. The link between these two interfaces is implementation specific and beyond the scope of this appendix. A Hybrid Repeater can be seamlessly connected to eUSB2 repeaters or ports configured in repeater mode. A simplified block diagram of eUSB2 Hybrid Repeater is shown in Figure B.1-3.

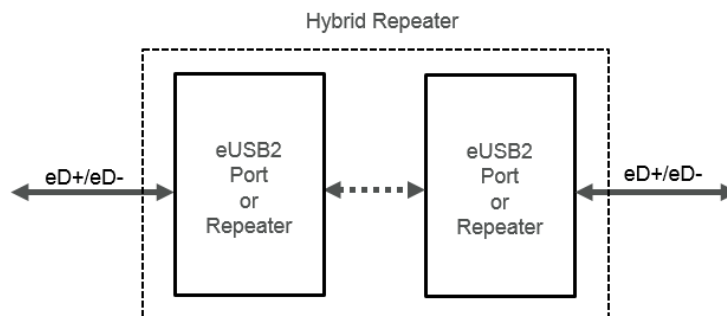


Figure B.1-3. eUSB2 Hybrid Repeater Block Diagram

## B.2. Hybrid Repeater Architecture

A Hybrid Repeater is comprised of two eUSBr ports connected back to back through two re-drivers and/or re-timers, as shown in the simplified block diagram in Figure B.2-1. Both the re-drivers/re-timers translate eUSB2 control commands /packets to implementation specific signaling. A Hybrid Repeater shall support all three data rates defined by USB 2.0:

- Low Speed (LS) at 1.5 Mb/s
- Full Speed (FS) at 12 Mb/s
- High Speed (HS) at 480 Mb/s

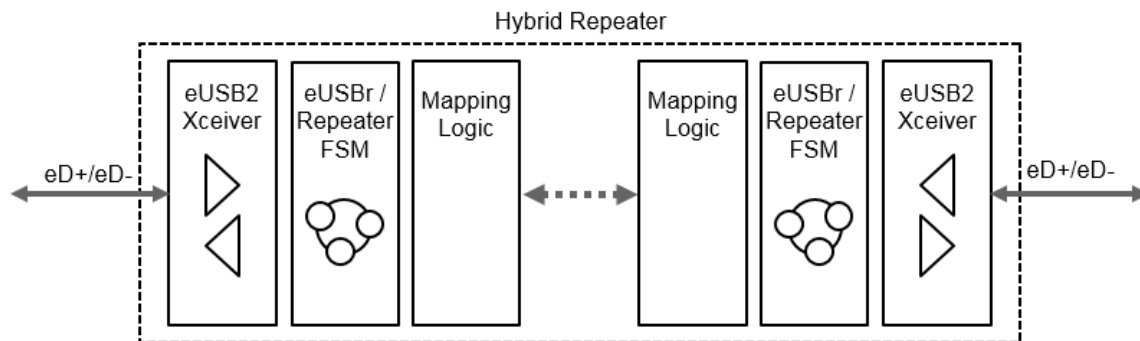


Figure B.2-1. Hybrid Repeater Architecture

## B.3. Modes of Configuration

### B.3.1. Configuration Definition

The eUSB2 Hybrid Repeater supports four different downstream and upstream port modes of the configurations as shown in Figure B.3.1-1 through Figure B.3.1-4. Each port of a Hybrid Repeater can be configured either as Upstream or as Downstream Port, or as a repeater enabling any mix between eUSB2-capable and USB 2.0-legacy Host and Devices.

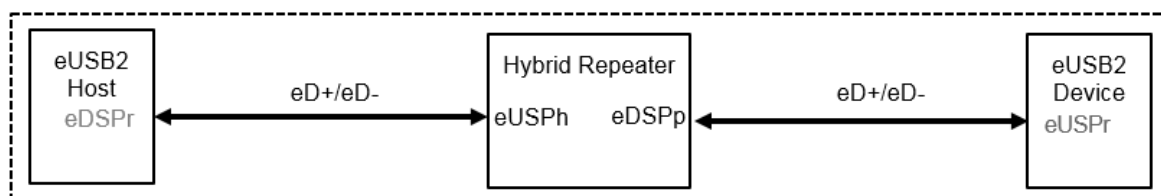
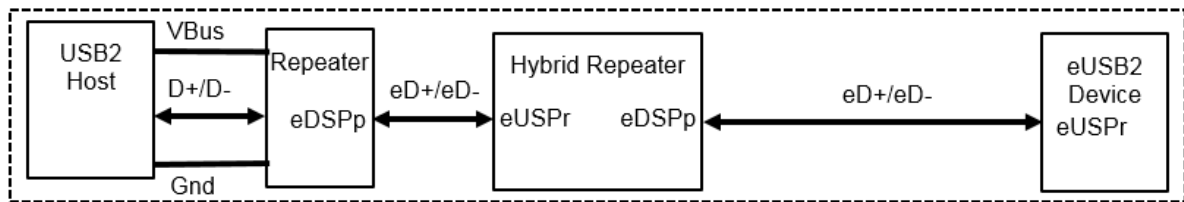
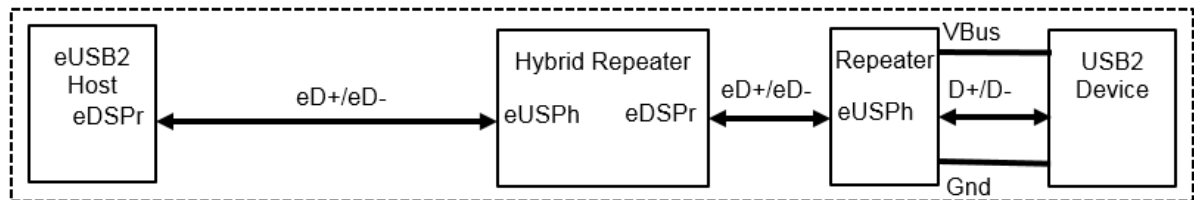


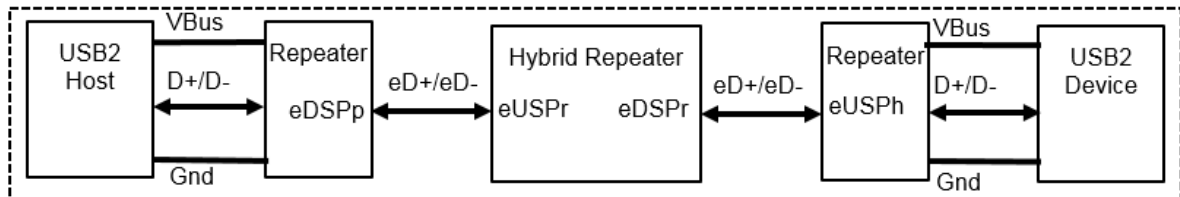
Figure B.3.1-1. Hybrid Repeater Configuration 1



**Figure B.3.1-2. Hybrid Repeater Configuration 2**



**Figure B.3.1-3. Hybrid Repeater Configuration 3**



**Figure B.3.1-4. Hybrid Repeater Configuration 4**

## B.3.2. Hybrid Repeater operations

In each configuration, Hybrid Repeater port (eUSPh/eDSPp, eUSPr/eDSPp, eUSBh/eDSPr, eUSBp/eDSPr) operation shall comply with the definitions in this specification. In HS mode, a Hybrid Repeater is allowed to consume up to 8 SYNC bits on the exit from Squelch and add EOP dribble up to 8 random (SE0 or K or J) bit durations when repeating packets.

### B.3.2.1. Control Messages

Control Messages are processed differently in Hybrid Repeaters depending on the Hybrid Repeater configurations defined in Section B.3.1.

In configuration 1, the Hybrid Repeater consumes Control Messages (CM) generated by the Host and the Device. CM handling shall be the same as a Repeater.

In configuration 2, the Hybrid Repeater functions as eUSPr to interact with a peripheral repeater connected to a USB host port. In Configuration 3, the Hybrid Repeater functions as eDSPr to interact with a host repeater connected to a USB device. In either configuration, the Hybrid Repeater is either forwarding or regenerating Control Messages issued respectively by the USB Device and the Host. Whether a Control Message is forwarded or regenerated is an implementation choice.

- A Hybrid Repeater shall constrain the delay to less than 3.5us when forwarding or regenerating a Control Message. Note that this additional latency has no impact when CM.L2 or CM.Reset is transmitted. When CM.FS is transmitted, this latency is borrowed from the 875 us allocated for checking for SE0. Refer to Section 7.1.7.5 of the USB 2.0

specification for details. When CM.L1 is transmitted, this additional latency is borrowed from part of the L1 residence time. Refer to USB 2.0 Link Power Management Addendum for details.

In configuration 4, the Hybrid Repeater serves as eDSPr and eUSPr interacting with the host repeater and the peripheral repeater. It is the source of Control Messages to both Repeaters, and therefore, needs to be protocol aware of the USB operation in order to issue Control Messages. Relaxed CM timings are allowed for the Hybrid Repeater in this configuration to generate CM.

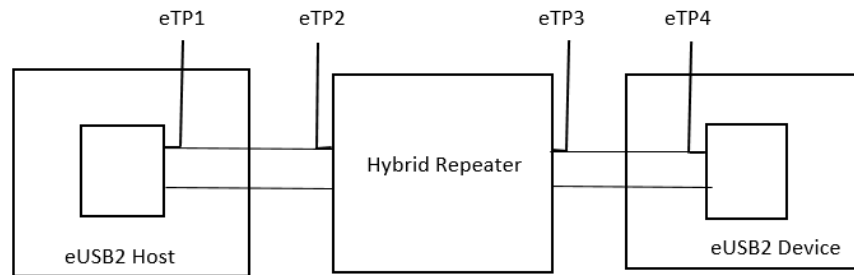
CM.RAP is optional for the Hybrid Repeater and is implementation specific.

## B.4. Electrical specification

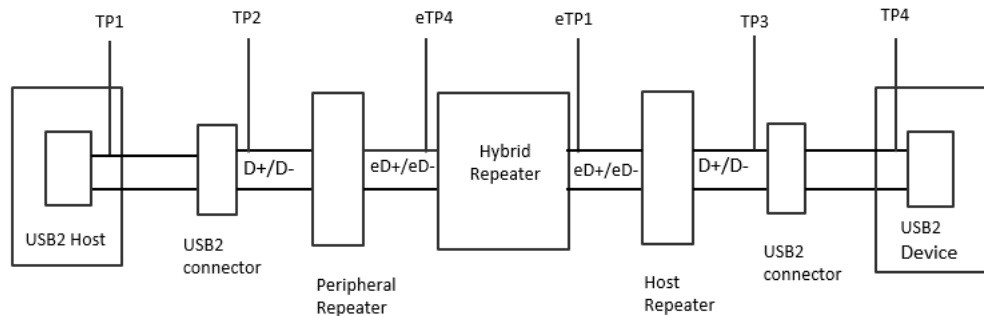
The eUSB2 repeater electrical specifications apply to the Hybrid Repeater in LS/FS and HS modes with a precision for LS/FS AC specifications given in Section B.4.3. The measurement planes and jitter allocation for a Hybrid Repeater are explained in this section.

### B.4.1. Hybrid Repeater Measurement planes and Jitter Allocation

Figure B.4.1-1 and Figure B.4.1-2 define the measurement planes for a Hybrid Repeater in configuration 1 and configurations 2, 3, 4 respectively.



**Figure B.4.1-1. Measurement Plane for a Hybrid Repeater (Configuration 1)**



**Figure B.4.1-2. Measurement Plane for a Hybrid Repeater (configuration 2, 3, 4)**

Note, the placement of peripheral repeater and host repeater in Figure B.4.1-2 is in line with the peripheral repeater and host repeater definition proposed in this specification (refer to Figure B.3.1-4 for the port naming convention).

The definitions of TP2 and TP3 remain the same as specified by USB 2.0 Section 7.1.2.2 - High-Speed Signaling Eye Patterns and Rise and Fall Time. eTP2 and eTP3 in Figure B.4.1-1 as well as eTP1 and eTP4 in Figure B.4.1-2 are the points where the IC pins of the Hybrid Repeater ports are soldered to the circuit board.



### B.4.2. High-Speed Hybrid Repeater Jitter Allocation

A detailed system level Jitter budget for the case when the Hybrid Repeater is a re-driver and used in configuration 1 is given in Table B.4.2-1.

**Table B.4.2-1: System Level Jitter Budgeting for Hybrid Repeater**

Jitter source	Tj (ps)	UI (%)
eUSB2Tx	166.5	8
Host Channel	96	4.6
Hybrid Repeater (re-driver)	412.5	19.8
Device channel	208.3	10
Total	883.3	42.4

Notes:

1. Hybrid Repeater jitter is informative and measured during test mode using a Test Packet.
2. The other modes of Hybrid Repeater configurations (configuration 2, 3 and 4), where additional eUSB2 repeaters are connected to the Hybrid Repeater, shall conform to jitter allocation defined in Section 7.1.5.3. When a retimer is used, it should also meet the USB 2.0 hub jitter budget described in Section 7.1.5.3.
3. When the Hybrid Repeater is implemented as a re-timer, it shall be treated as a typical USB 2.0 hub from a jitter budgeting perspective.

### B.4.3. Low-Speed / Full-Speed AC Specifications

When applicable to a Hybrid Repeater, the Low-Speed /Full-Speed AC specifications defined in earlier in this specification remain the same, with the following precision for the FS paired transition jitter in both directions.

**Table B.4.3-1: Hybrid Repeater Low-Speed / Full-Speed AC Specifications**

Parameter	Symbol	Min	Typ	Max	Units	Notes
Hybrid Repeater FS paired transition jitter in both directions	T <sub>DJ2_HR</sub>	-3		+3	ns	1

Notes:

1. In case of Hybrid Repeater, T<sub>DJ2</sub> defined in the base Specification for repeater is replaced by T<sub>DJ2\_HR</sub>