USB 3.0 SuperSpeed Equalizer Design Guidelines

Contents

1. Introduction

1.1 Purpose

This document describes the trade-offs involved in defining and designing the equalization circuits for USB 3.0 SuperSpeed transceivers. The descriptions include the range of interconnect channels and their electrical characteristics, key features of the USB 3.0 specification for enabling equalizer optimization, parameters describing equalizer behavior and recommended operating ranges for each, and considerations for implementation of the equalizer training.

The physical layer section (chapter 6) of the USB 3.0 specification [1] defines informative and normative specifications for SuperSpeed transceivers. This document is intended to supplement the specification and to provide guidance to transceiver designers.

1.2 Overview

Historically, Universal Serial Bus usage has spanned a wide range of interconnection environments. Examples of the range are shown in Figure 1. The short channel in the figure represents a device that plugs directly into the host connector (such as a memory stick) with a host controller that is as close as possible to the host port connector ("A" connector). The printed circuit board routing for such devices tends to be very short as well, perhaps as small as 10mm. Due to the short transmission lines, this configuration will have a relatively low differential insertion loss, perhaps as little as -4dB at the fundamental frequency for the signal (2.5GHz).

At the other extreme, the long channel connects the USB device to the controller through a 3 meter long cable. In addition, the traces on the printed circuit board are routed at the maximum length (approximately 10") and may contain multiple layer-layer transitions using through-hole vias. In addition, the routed length on the device may be up to 50mm (2") in length. In this case the differential insertion loss for the channel is expected to be in the range of -17dB to -18dB at 2.5GHz.

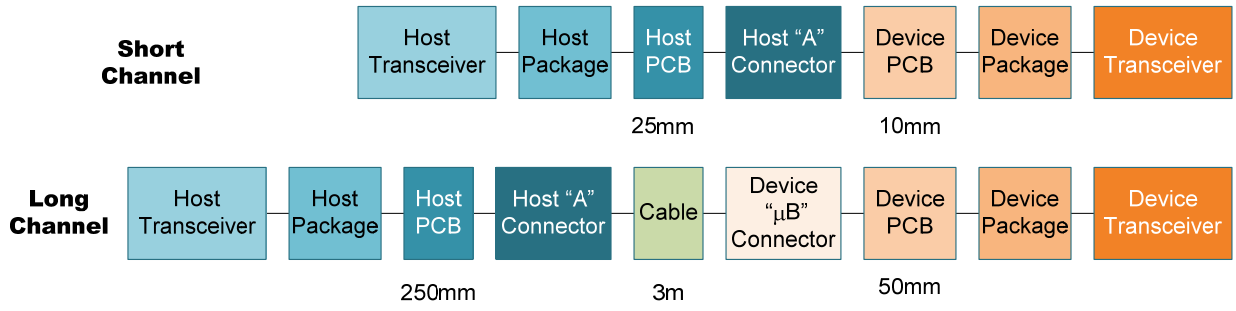
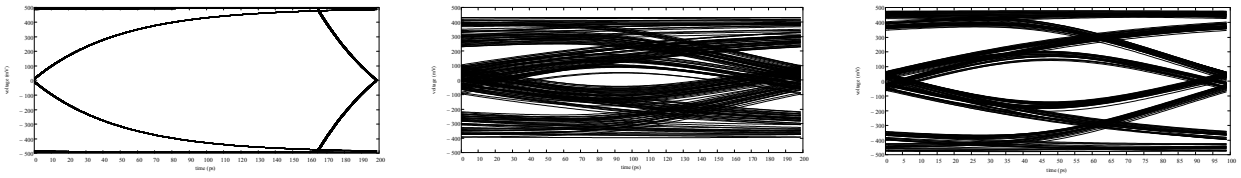


Figure 1. USB interconnect channel application range.

At multiple gigabit per second (Gb/s) data rates, frequency dependent losses from the interconnect channel cause it to act like a low pass filter. This filtering effect has a "smearing" effect on the signals, which results in a reduced eye opening, as illustrated in Figure 2(b). SuperSpeed USB uses equalizers at the transmitter and receiver to counter the effects of the channel, as seen in Figure 2(c). [2] The interactions between the channel and equalizer design are a key focus of the remainder of this document.



(a) transmitter output (b) receiver input (c) equalizer receiver input

Figure 2. Channel loss impact on data eye.

1.3 Organization

The document is organized as follows:

- Chapter two provides additional detail on the channel environment, including descriptions of the key mechanisms that impact the data eye. Models for the compliance channel are introduced, including the reference equalizer transfer function.
- Chapter three describes the models for transmit and receive equalizers, introduces the key parameters for describing their behavior, and describes the reference equalizer for use in transmitter compliance testing using the existing compliance channel. In addition, it describes the approach to optimizing the behavior of the equalizer design that is provided for by the USB 3.0 specification.
- Chapter four presents simulation results that demonstrate the impacts of the varying interconnect channels on the data eye and on the equalization requirements for the system. The chapter also introduces a supplemental compliance channel and reference equalizer for use in ensuring sure that a transceiver design operates robustly in a low loss environment.
- Chapter four demonstrates the requirements for the equalizer behavior. Specific focus is placed on the dynamic range of the receiver equalization, specifically the dynamic range, in order to ensure successful operation throughout the full range of expected channel environments.
- Chapter five discusses recommendations for the operating ranges of the equalizers in SuperSpeed designs.

1.4 References

Universal Serial Bus 3.0 Specification, revision 1.0.

Advanced Signal Integrity for High-Speed Digital Designs, John Wiley and Sons, 2009.

Electrical Compliance Test Specification, SuperSpeed Universal Serial Bus, revision 0.95.

1.5 Additional notes

- This document refers only to hosts and devices, but is intended to apply equally to hub designs.

2. Channel Environment

As described in the introduction, the characteristics of the interconnects in USB applications varies widely depending upon the length of the package and printed circuit board (PCB) traces for both host and device, and on the length of the cable providing the connection between the two. In this chapter we will provide descriptions and models of example short and long channels that we will use in analyzing equalizer performance requirements. We will further subdivide the channels into two classes, full link channels and compliance channels, providing the details and roles for each in guiding the equalizer design process.

2.1 Full Link Models

Full link models represent the application environment for a SuperSpeed signaling interface, and include models for the PCB and package for both ends of the interface (i.e. device and host). The two models that we are using are described in Figure 3. All models contain three differential pairs, so that the effects of crosstalk are included in the simulations, as Figure 4 illustrates. All simulations in this study use the middle signal pair of the model as the "victim", along with a near end crosstalk (NEXT) aggressor pair on one side and a far end crosstalk (FEXT) aggressor on the other.

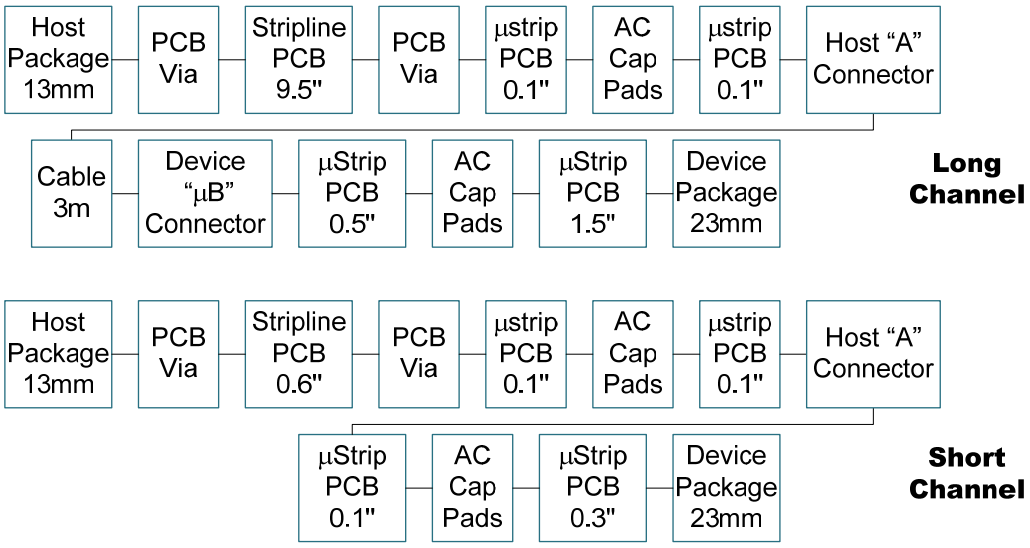


Figure 3. Full link channels used in this study.

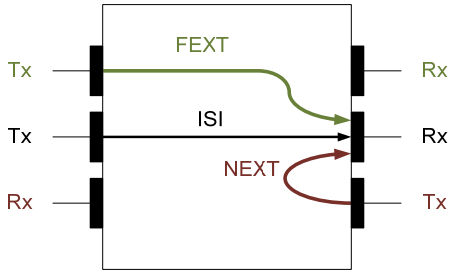
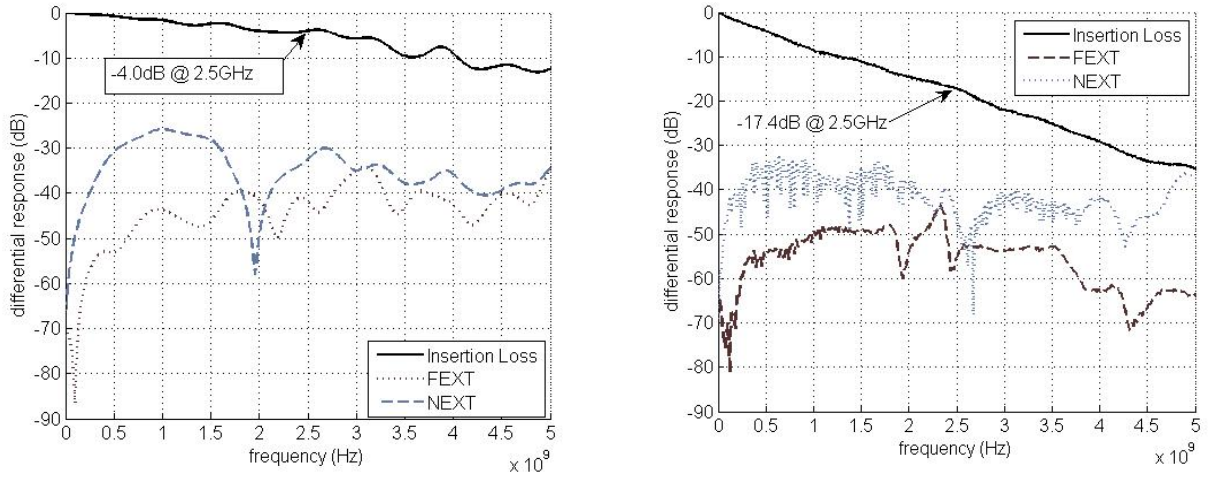


Figure 4. Crosstalk contributors.

The transmission line models for printed circuit boards and packages are based on 85Ω ±15% differential impedance, and include both microstrip and stripline structures. The models for the cables are 90Ω ±7%. Impedance variation is incorporated into the full channel models. Note that the host PCB includes both stripline and microstrip routing, based on a 6-layer board stack-up. The via models cover a transition between the top layer to the 3rd layer from the top of the board. The device PCB uses only microstrips, as it is expected that minimum layer count boards are used. Package models include connections from the silicon to the package substrate, layer-to-layer connections within the substrate, and solder ball connections to the underlying PCB.

Full link frequency responses are plotted in Figure 5 for both the short channel (device driving) and long channel (host driving) models. The plots indicate an insertion loss difference of more than 13dB at the fundamental frequency. In addition, the short channel shows approximately 6dB more NEXT than does the long channel. Chapter four will present time domain results (pulse responses) based upon these frequency responses.



(a) short channel

(b) long channel

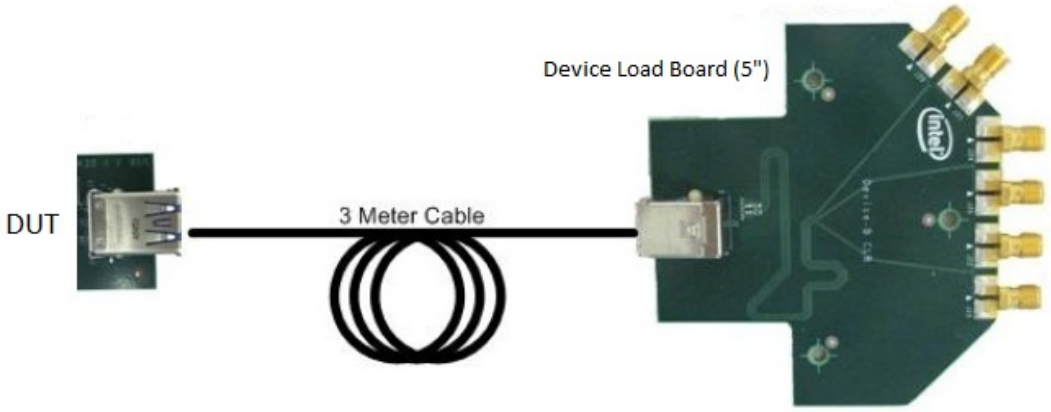
Figure 5. Example full link frequency responses.

2.2 Compliance Channels

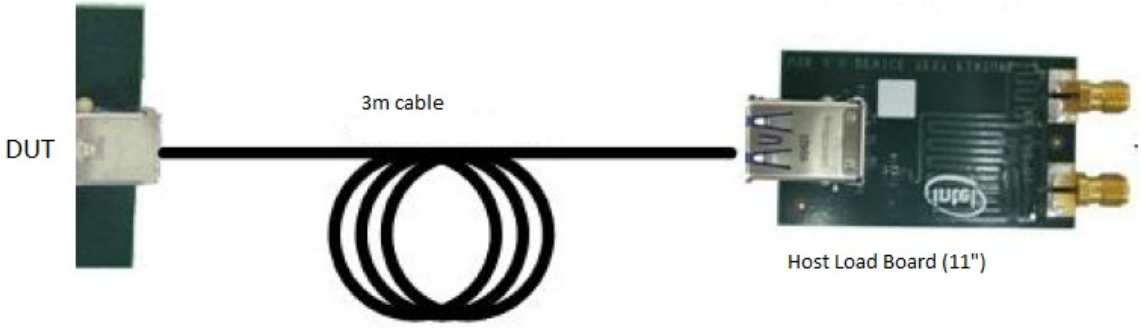
The electrical compliance testing portion of the logo certification program is intended to ensure interoperability between device and host designs. The electrical compliance tests make use of compliance channels that are designed to provide behavior that is representative of real applications. Different channels are used for host and device tests, as Figure 6 shows.

The "host compliance test channel" in Figure 6(a) is used to test compliance for host designs. The compliance channel includes a 3m length SuperSpeed cable (the maximum allowed by the spec) connected to a printed circuit board that has 5" of trace providing connection between a standard device connector and SMAs that then connect to a oscilloscope. The five inch trace length represents a maximum loss device design (PCB plus package).

The "device compliance test channel" in Figure 6(b) is used to test compliance for device designs. The compliance channel includes a 3m length SuperSpeed cable (the maximum allowed by the spec) connected to a printed circuit board that has 11" of trace providing connection between a standard host connector and SMAs that then connect to a scope. The eleven inch trace length represents a maximum loss host design (PCB plus package).



(a) Host compliance test channel



(b) Device compliance test channel

Figure 6. Compliance channels for host and device designs.

Testing specifications for transmitter and receiver compliance are contained in reference [3]. The analysis in this document will focus on the transmitter compliance test. The USB 3.0 specification requires that the transmitter compliance measurement is to be made at the SMA test points, after the signal propagates through the DUT, compliance cable, and load board. The specification requires that the DUT meet a minimum eye height of 100mV over one million unit intervals, which corresponds to an estimated average BER of 10^{-6}, after post-processing with the reference equalizer transfer function described in chapter 3. The eye width requirement is 68ps minimum, extrapolated to BER=10^{-12} after separation of jitter into random and deterministic components. The remainder of the analysis focuses on the eye height spec, which tends to be the limiting case. Transceiver designers should be sure examine eye width as well when analyzing designs.

Models of the compliance channels, in 4-port Touchstone® format, are available for use in design and characterization of SuperSpeed devices. Plots of the measured frequency response (differential insertion loss) for both compliance channels are shown in Figure 7. They can be found at the USB website (www.usb.org). The analysis and results that are presented throughout this document make use of these compliance channel models.

Figure 8 depicts the frequency response for a device model in the compliance environment. The device model consists of a package, 2" of microstrip routing, and the micro-B device connector. A quick comparison of Figure 5(a) and Figure 8 shows that a device may be used in an environment that has nearly 11dB less loss than it will see in the compliance environment. A host may see a similar difference between minimum channel loss in operation and the compliance environment. Chapter 4 presents results that demonstrate the impact on the data eye, and provides a supplemental channel environment for addressing the difference.

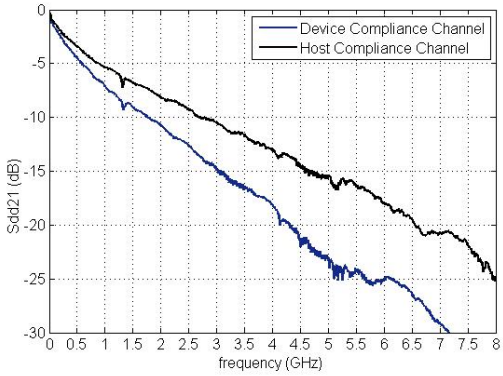


Figure 7. Compliance channel frequency responses for host and device designs.

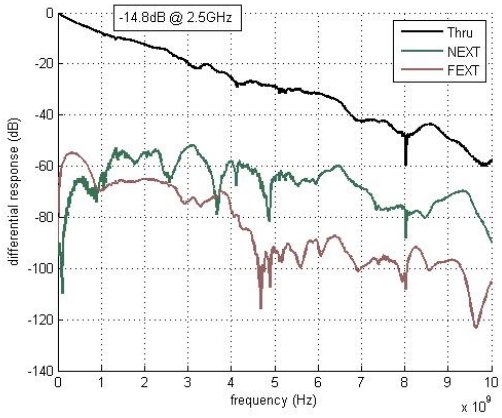
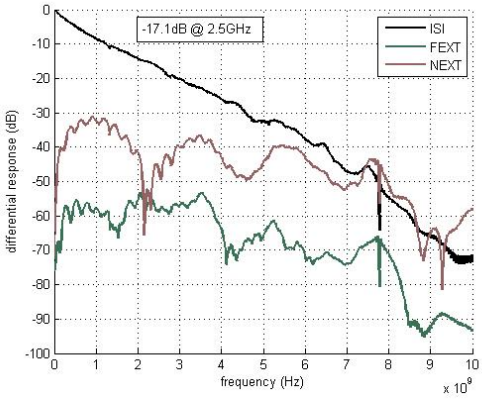
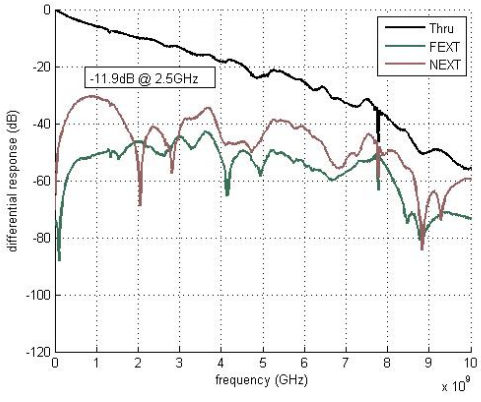


Figure 8. Frequency response for an example device design plus compliance channel.



(a) 10” Host PCB



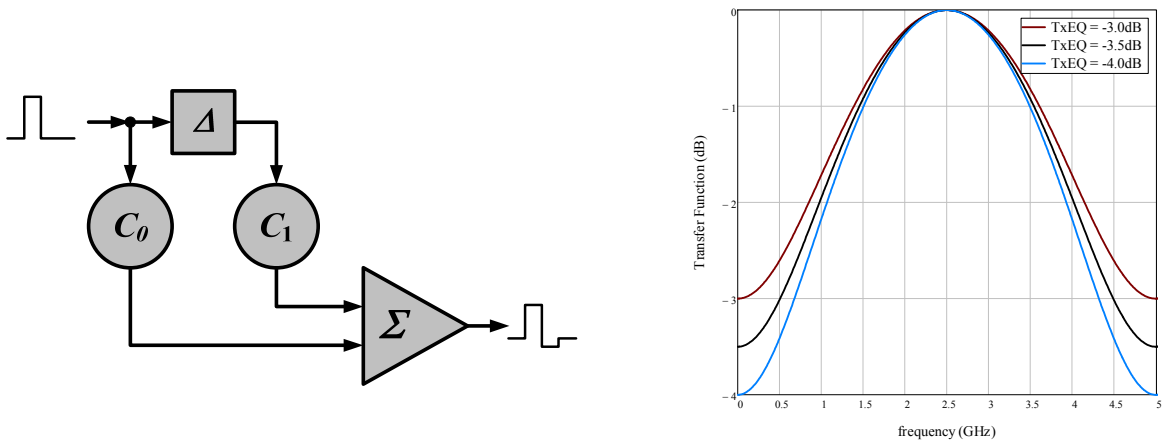
(a) 1” Host PCB

Figure 9 Frequency response for example host designs plus compliance channel.

3. Equalization in SuperSpeed USB

3.1 Transmitter Equalization

Due to the lossy nature of the channel, the data eye at the receiver input may be closed. As a result, the USB 3.0 specification provides for equalization at both transmitter and receiver in order to meet system timing and voltage specifications. Transmitter equalization is specified as 3.5dB±0.5dB of de-emphasis (attenuation), under the assumptions that it is implemented as a two-tap FIR filter, as shown in Figure 10(a). The frequency response is also contained in the figure for the full 3-4dB range of the specification, showing the high pass behavior of the equalizer up to the 2.5GHz SuperSpeed fundamental frequency.



(a) Equalizer structure

(b) Transfer function

Figure 10. Transmit equalizer & frequency response.

3.2 Receiver Equalization

Since the interconnect for USB applications may as much as 18dB or more of loss at the fundamental frequency, the USB specification provides for additional equalization at the receiver. As of April 2011, the specification provides a reference transfer function as an aid to circuit designers and for use in compliance testing. The equalizer transfer function, as shown in equation (1) and Figure 11, is expressed in terms of a second order continuous time linear equalizer. The parameters for the equalizer, along with the reference values, are contained in Table 1.

$$H_{RxEQ}(f) = \frac{A_{dc} f_{p1} f_{p2}}{f_z} \cdot \frac{jf + f_z}{(jf + f_{p1})(jf + f_{p2})} \quad (1)$$

In the equation, $H_{RxEQ}(f)$ is the reference equalizer transfer function.

Table 1. Reference CTLE design parameters

Parameter	*Value*	*Description*
A_{dc}	0.667	DC gain

f_z	650MHz	Zero frequency
f_{p1}	1.95GHz	1st pole frequency
f_{p2}	5GHz	2nd pole frequency

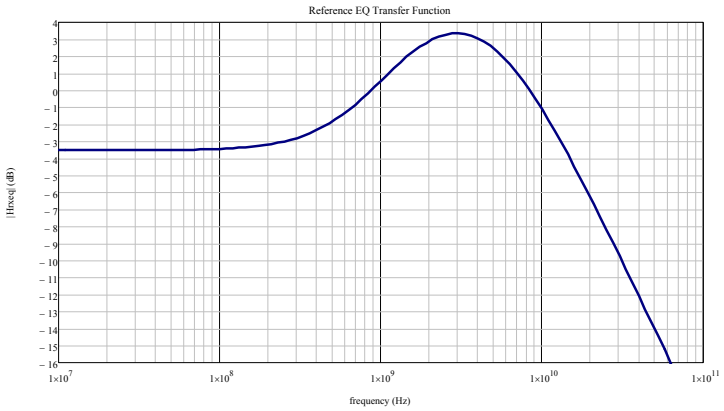


Figure 11. Receive equalizer and frequency response.

The base spec does not place specific requirements on the behavior of the equalizer in order to allow flexibility and innovation in the design implementation. However, the loss envelope described in this work can be used to establish recommended ranges for the equalizer parameters, which will be described in chapter 5.

Finally, note that although the transfer function is expressed in terms of a 2nd order continuous time filter, the specification does not mandate the actual implementation of the equalizer, leaving the designer with the freedom to choose the topology, order, and structure of the filter (or to use a digital filter).

3.3 Equalizer Training Sequence

To accommodate a wide range of channel loss the specification provides for training of the receiver equalizer during initialization of the link. This is done in order to allow both sides of the link to optimize behavior of the equalizer to counter the loss of the specific channel being used. The TSEQ training sequence (refer to section 6.4 of the specification), shown in Table 2, is designed to provide a rich spectrum for training typical receiver equalization architectures (see Figure 12), and to provide a high edge density to help the CDR maintain bit lock. The TSEQ training sequence repeats 65536 times over a total of 4194.3µs to allow for testing many coefficient settings. No SKPs are inserted during the TSEQ training sequence.

As mentioned above, the base specification does not a mandate specific design or training algorithm to allow flexibility in implementation. Instead, compliance testing is used to check the robustness of the voltage and timing margins.

Table 2. Equalization training sequence (TSEQ) ordered set

Symbol Number	Name	Value		Symbol Number	Name	Value
0	K28.5	COM (Comma)		9	D18.3	0x72

Symbol Number	Name	Value		Symbol Number	Name	Value
1	D31.7	0xFF		10	D14.3	0x6E
2	D23.0	0x17		11	D8.1	0x28
3	D0.6	0xC0		12	D6.5	0xA6
4	D20.0	0x14		13	D30.5	0xBE
5	D18.5	0xB2		14	D13.3	0x6D
6	D7.7	0xE7		15	D31.5	0xBF
7	D2.0	0x02		16-31	D10.2	0x4A
8	D2.4	0x82				

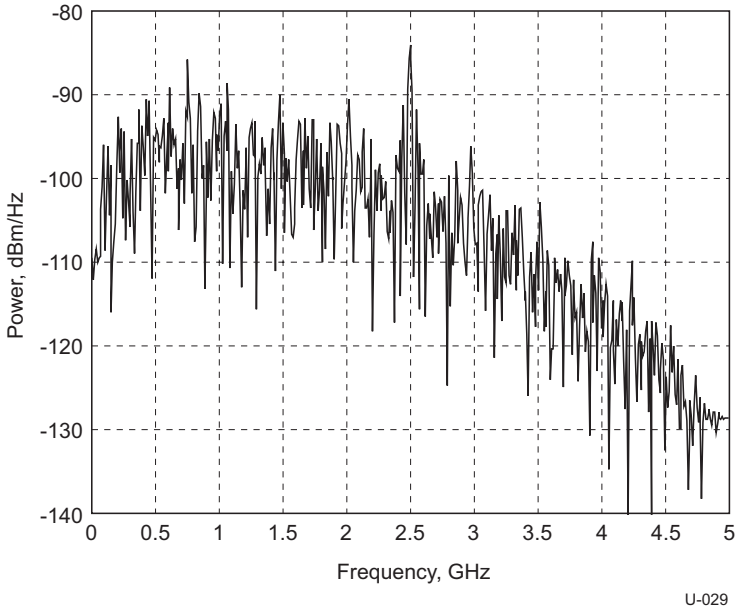


Figure 12. TSEQ frequency spectrum.

4. Results

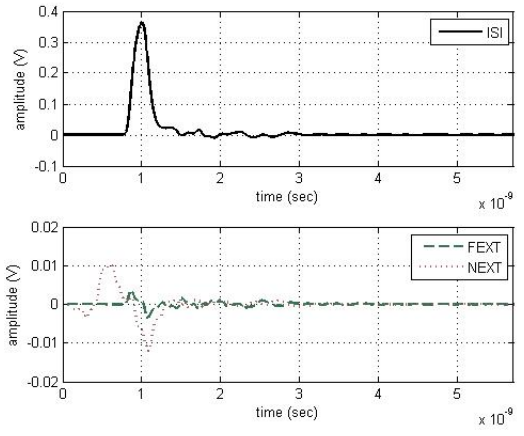
4.1 Introduction

This chapter provides simulation results for example host and device application channels (full link simulations) and for the same host and device interconnects in the compliance environment. Results include frequency responses, pulse responses, and voltage margins. They will demonstrate the benefit of to supplementing the original compliance channel with an additional channel to be used in making sure equalizer designs work properly across the entire range of application channels.

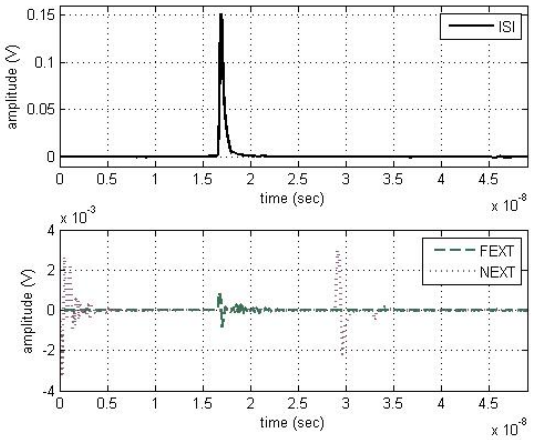
4.2 Full Link Simulations

Figure 13 shows pulse responses for the short and long channels from Figure 3. In addition to the pulse responses on signals of interest, the plots include near-end and far-end crosstalk responses (NEXT/FEXT), all of which are used in the statistical voltage margin calculations. Figure 14 contains the pulse responses after equalization by both the transmitter and equalizer. The transmit equalization uses the maximum amount allowed by the spec (4dB) and the receiver uses the reference transfer function. Figure 15 contains the bathtub curves for the voltage margin as a function of bit error ratio (BER). The curves include the effects of deterministic and random jitter from the transmitter and receiver, as well as inter-symbol interference and crosstalk due to the interconnect channel. The USB 3.0 specification mandates a BER of 10^{-12}. Both channels show positive voltage margin, though the short channel has significantly less margin than might be expected for such a short channel.

Inspection of Figure 14(a) provides insight into the reason for the small margin. The figure shows significant negative inter-symbol interference (ISI) in the interval immediately following the pulse, which is caused by applying too much equalization. The device application channel has a differential insertion loss of -4dB at the 2.5GHz fundamental frequency (refer to Figure 5). Application of the 4dB of transmit equalization will remove the vast majority of the intersymbol interference (along with some attenuation), and the reference equalization at the receiver is not needed. We will return to this point in the next section.

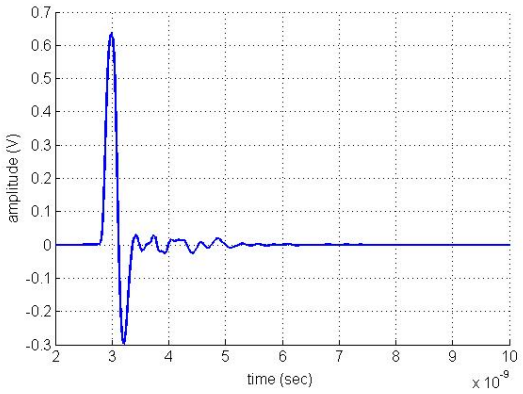


(a) short channel

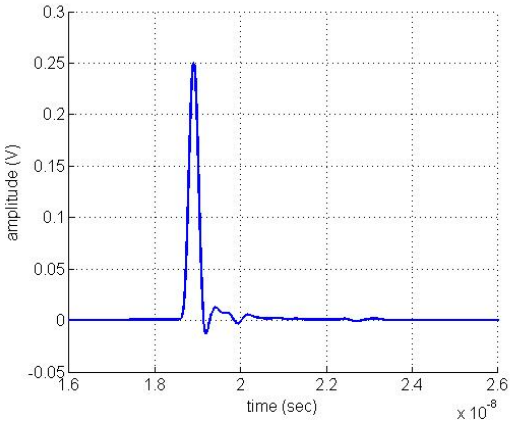


(b) long channel

Figure 13. Example pulse responses (no equalization).

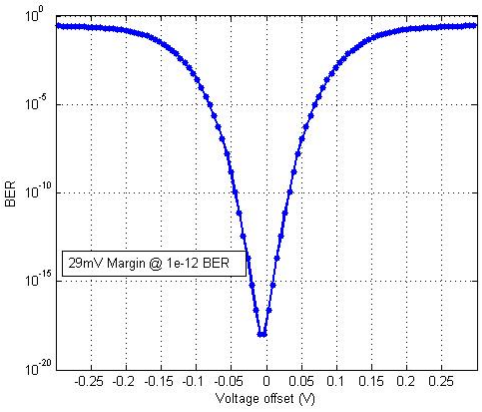


(a) short channel

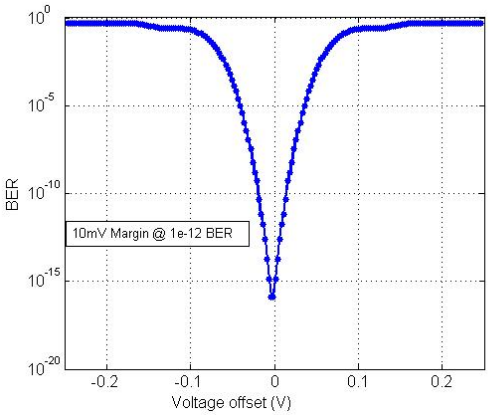


(b) long channel

Figure 14. Example equalized pulse responses (TxEQ=-4dB, RxEQ=reference).



(a) short channel



(b) long channel

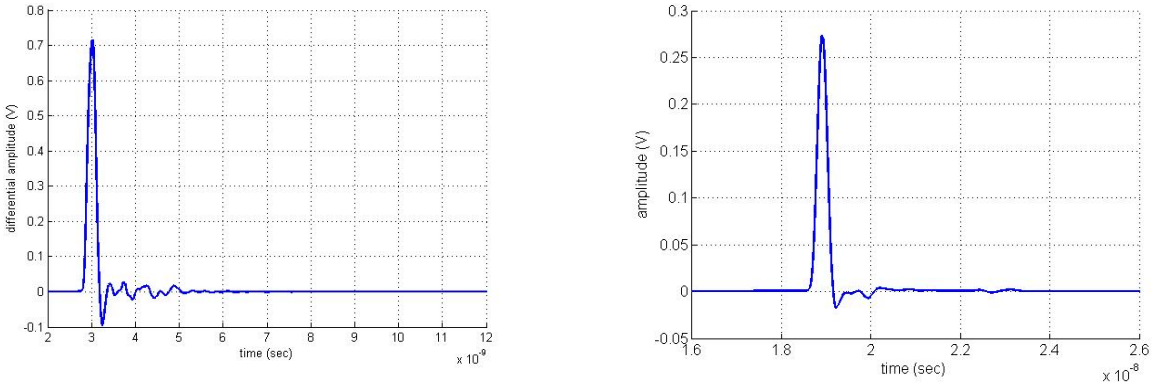
Figure 15. Example voltage margin bathtub curves (TxEQ=-4dB, RxEQ=reference).

As discussed in section 3, the USB 3.0 specification makes provisions for training the receiver in the equalizer to optimize its' frequency response to the characteristics of the specific channel. Figure 16 and Figure 17 contain pulse responses and voltage bathtub curves resulting when the receiver equalizer is trained for both the short and long channels. The equalizers were trained by allowing the behavioral parameters to vary over expected ranges, using eye width as the optimization metric.

Looking at Figure 18 reveals that the equalizer trains to a very similar response as the reference equalizer for the long channel, which we might expect given the characteristics of the compliance channel. As a result, the margin improvement realized by training the equalizer is a modest 7mV.

However, the training result for the short channel yields a very different equalizer behavior. In that case, the trained equalizer looks like a low pass filter with a small amount of amplification and a cut-off frequency above the third harmonic of the data signals. The margin for the trained case shows an improvement of more than 250% (80mV)

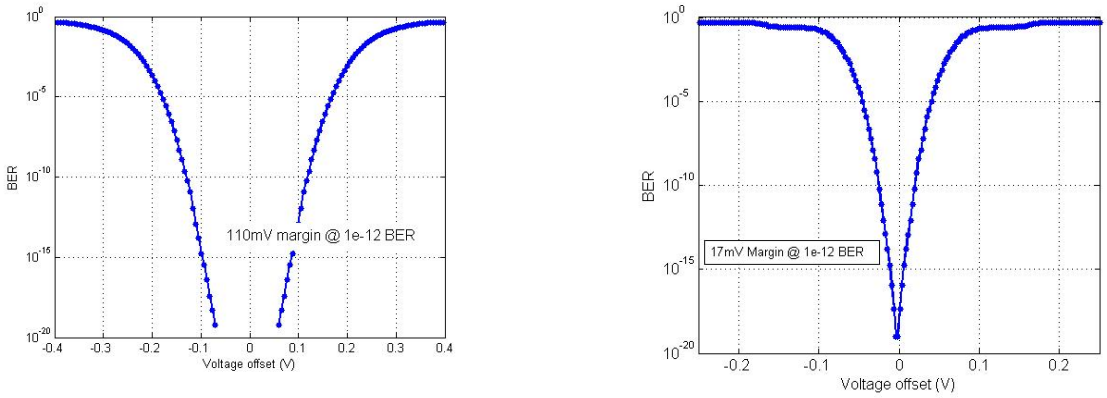
compared with the reference equalizer result, demonstrating the benefit of training the equalizer and supporting the earlier suggestion that a good equalizer design needs a wide dynamic range in order to operate under all expected channel conditions.



(a) short channel

(b) long channel

Figure 16. Example equalized pulse responses (TxEQ=-4dB, RxEQ=trained).



(a) short channel

(b) long channel

Figure 17. Example voltage margin bathtub curves (TxEQ=-4dB, RxEQ=trained).

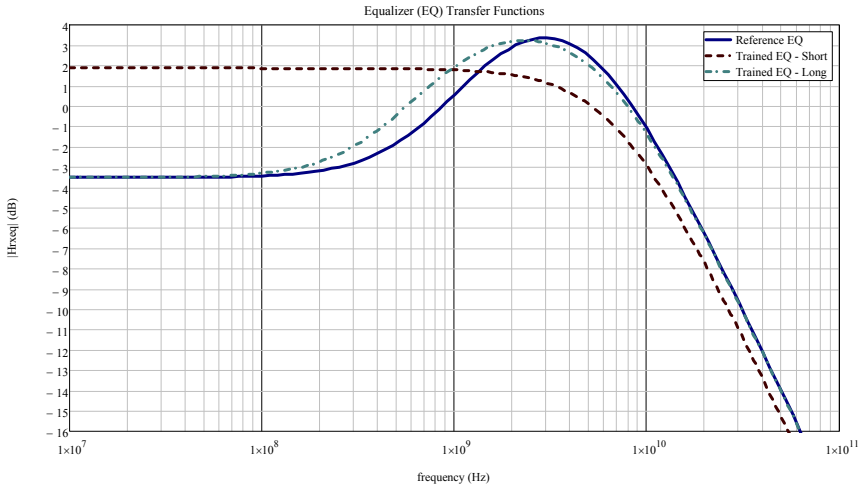
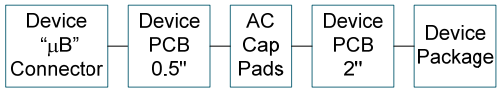


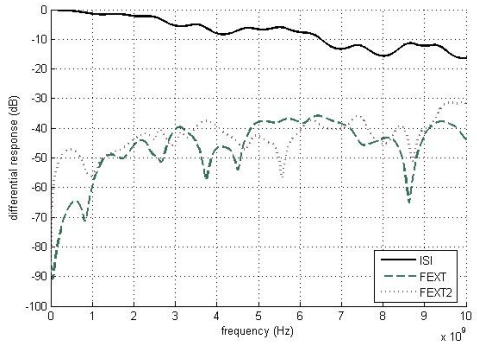
Figure 18. Frequency responses for reference equalizer and trained equalizers for the short and long channels.

4.3 Compliance Simulations

The compliance simulations in this section focus on the case in which the device is transmitting. The model for the device, including package, PCB and connector is shown in Figure 19, along with the frequency response. The frequency response in the compliance environment is shown in Figure 8. Time domain pulse response with and without equalization are shown Figure 20, and the resulting voltage bathtub plot is contained in Figure 21. The plots show symmetric 28mV voltage margins to the 100mV eye height spec for both the high and low voltage levels, indicating that the existing compliance channel and reference equalizer give reasonable results for the long channel with the example device design.

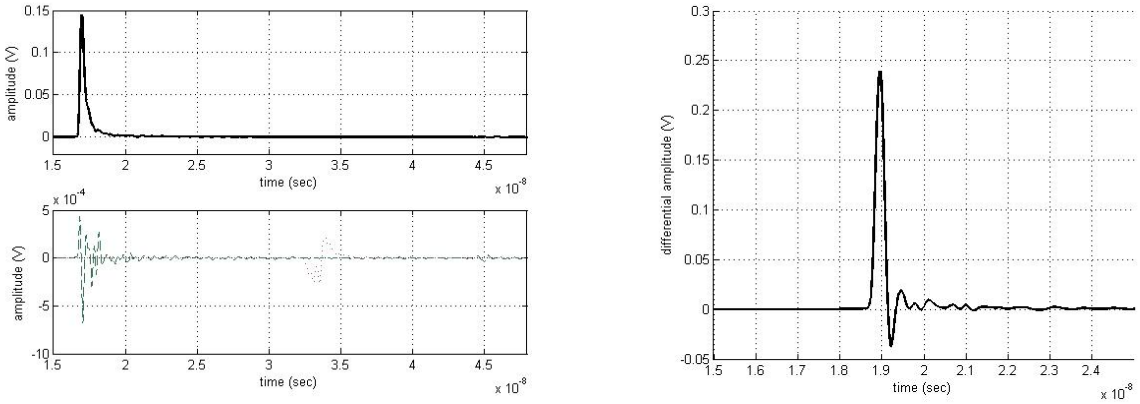


(a) Device model



(c) Frequency response

Figure 19. Device channel model and frequency response for section 4.3 and 4.4.



(a) Non-equalized

(b) Equalized

Figure 20. Example device compliance pulse responses (TxEQ=-4dB, RxEQ=reference).

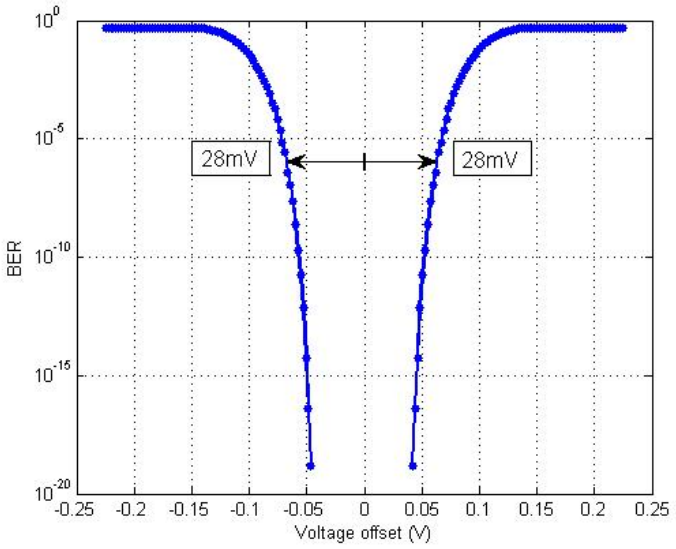


Figure 21. Example device voltage margin bathtub curve (TxEQ=-4dB, RxEQ=reference).

4.4 Supplemental Compliance Environment

The previous section addressed the compliance for the long channel. In order to establish high confidence in the design across the expected application range, an additional channel that allows characterization of the transceiver for the minimum loss case would be beneficial. The additional 'supplemental' compliance channel would consist of a minimum length cable connected to a minimum length host load board for device compliance simulation and measurement. For host compliance, the additional channel would use a minimum length cable and minimum length device load board. These channels are depicted in Figure 22 and their respective frequency response characteristics are shown in Figure 23.

Figure 24 contains pulse responses before and after filtering with the reference equalizer transfer function. The figure shows a response that appears to be reasonable prior to equalization but becomes over equalized by the reference filter. The voltage bathtub curve in Figure 25 shows +1/-3mV of margin on the bottom/top sides of the eye. These margins are far too small for such a low loss channel, which supports the visual evidence of the over-equalization in pulse responses.

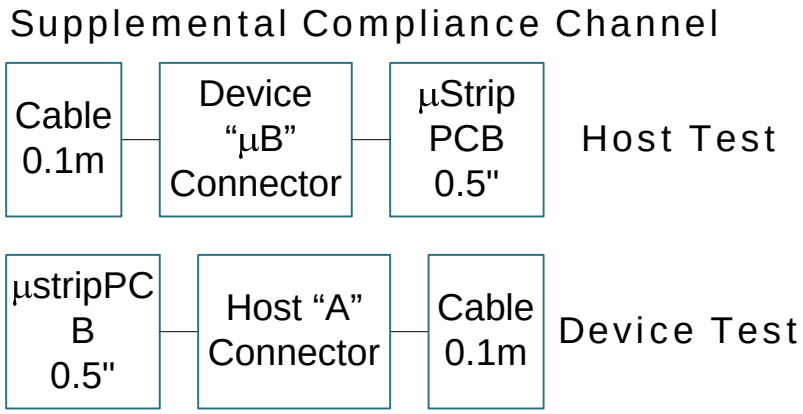
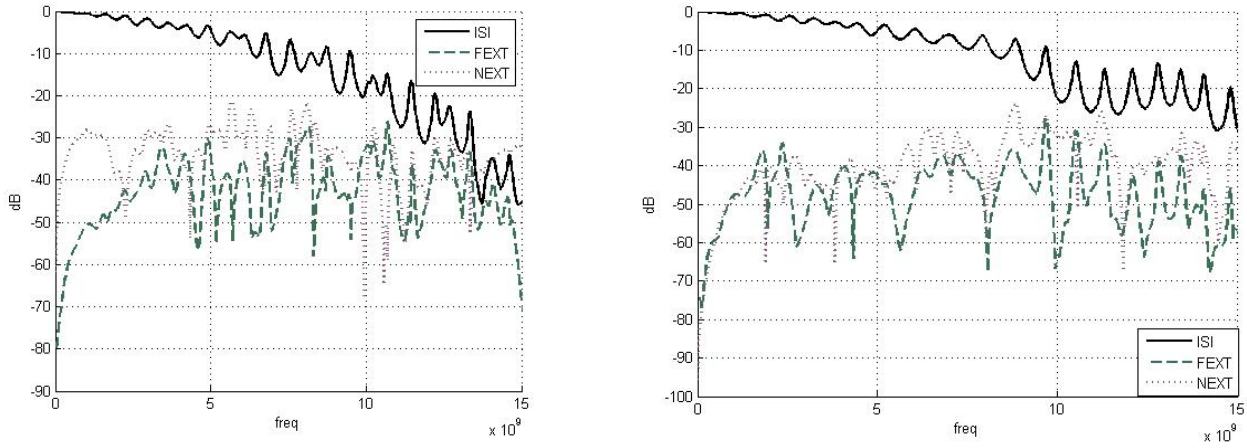


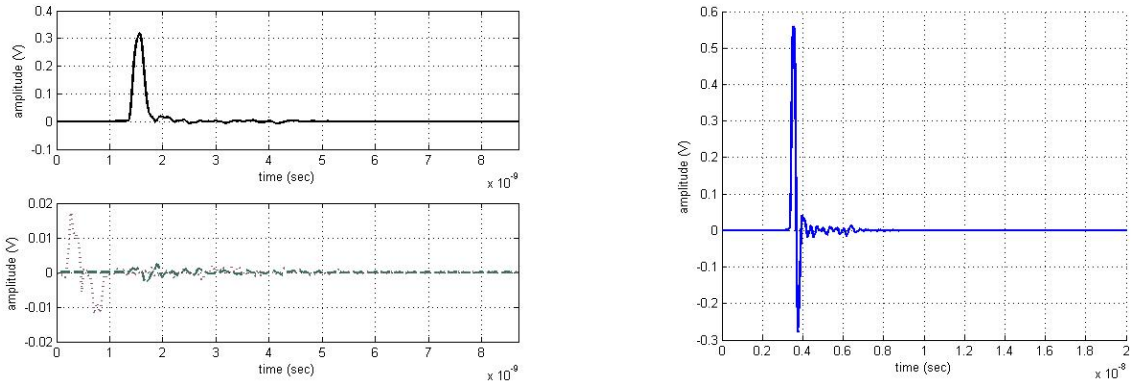
Figure 22. Supplemental compliance channels for host and device simulation & measurement.



(a) Channel for device testing

(b) Channel for host testing

Figure 23. Frequency response for supplemental compliance channels.



(a) Non-equalized (b) TxEQ=-4dB, RxEQ=reference

Figure 24. Device pulse response in supplemental compliance environment.

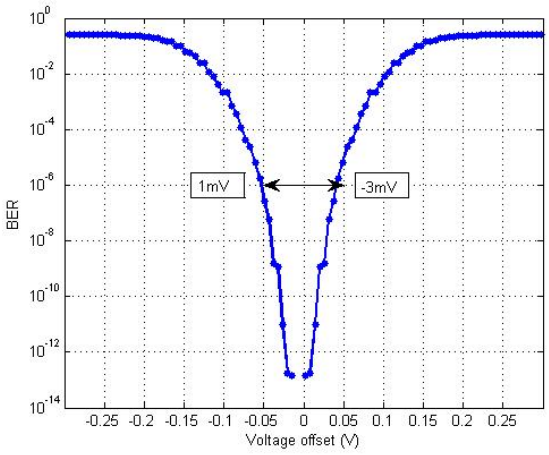


Figure 25. Device voltage margin in supplemental compliance environment with TxEQ=-4dB and RxEQ=reference.

In order to make the supplemental compliance channel useful for assessing design robustness, a supplemental reference equalizer that matches the channel response is needed. The trained equalizer transfer function for the full link short channel that was presented in Figure 18 provides insight into the desired behavior. The figures suggests that a reference equalizer that acts like a low pass filter but with a cut-off frequency well above the fundamental frequency would be sufficient. This will allow the vast majority of the signal energy to pass through without any change in magnitude. Figure 22 and Table 3 provide the behavior of a reference equalizer function what was created by taking the original reference equalizer making two slight changes. The first is to set the DC gain equal to one to make sure the magnitude is not changed at DC. The second change readjusts the pole frequencies to 650MHz and 10GHz to create a flat frequency response up to 10GHz.

Applying the new reference equalizer to the signal results in the responses shown in Figure 27. The figure show that the proper choice of reference equalizer to go with the supplemental channel creates a reasonably equalized signal that demonstrates robust eye height margins.

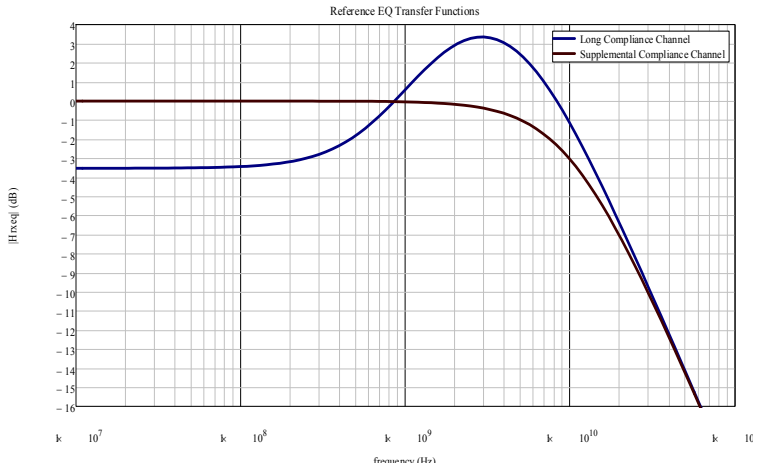
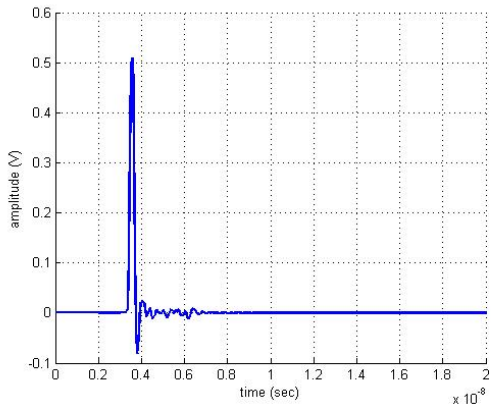


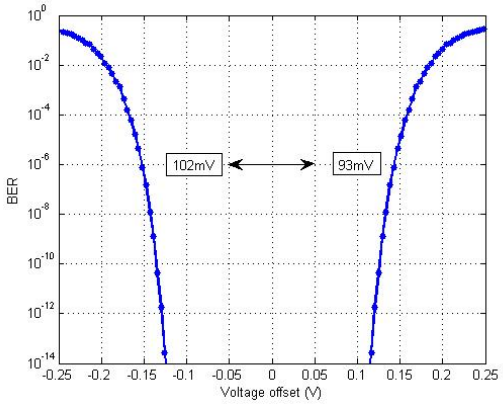
Figure 26. Reference equalizer transfer functions for use with the original and supplemental compliance channels.

Table 3. Reference CTLE design parameters for use with supplemental compliance channel

Parameter	*Value*	*Description*
A_{dc}	1	DC gain
f_z	650MHz	Zero frequency
f_{p1}	650MHz	1st pole frequency
f_{p2}	10GHz	2nd pole frequency



(a) Pulse response



(b) Voltage margin

Figure 27. Equalized device pulse response and voltage margin in supplemental compliance environment with TxEQ=-4dB and RxEQ=reference #2.

5. Summary and Recommendations

This white paper has demonstrated the need to design SuperSpeed transceivers, particularly the equalizer in the receiver, to accommodate a wide range of channel conditions. Universal Serial Bus is a consumer-based application with largely uncontrolled channel conditions, so success in the market depends heavily on the ability to adapt transceiver behavior each time a device is used. To do so, the following is recommended to the designers of SuperSpeed PHYs:

1. Design the RxEQ to accommodate a range of channel loss from at least -4dB to -18dB. Adding a couple of dB on either side is a good idea in order to guarantee robustness.
2. Use the compliance channel models (original and supplemental) in conjunction with the reference equalizers to check the eye margins of your design against the spec. The models are suitable for application to pre- and post-silicon characterization. Both the original and the supplemental compliance channels are available on the USB Developer website.