# Universal Serial Bus
# PS Interface White Paper

*Revision 1.00*

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## Editor

| | | |
|---|---|---|
| Richard Wahler | SMSC | |

## Contributors

| | | |
|---|---|---|
| Gary Verdun | Dell, Inc. | |
| Steve Sedio | Foxconn / Hon Hai | |
| Alan Berkema | Hewlett Packard | |
| Lee Atkinson | Hewlett Packard | |
| Rahul Lakdawala | Hewlett Packard | |
| Ron Schooley | Hewlett Packard | |
| Vaibhav Malik | Hewlett Packard | |
| Walter Fry | Hewlett Packard | |
| Bob Dunstan | Intel Corporation | PD Chair/Protocol WG Lead |
| Brad Saunders | Intel Corporation | |
| Dan Froelich | Intel Corporation | |
| David Harriman | Intel Corporation | |
| Jervis Lin | Intel Corporation | |
| John Howard | Intel Corporation | |
| Leo Heiland | Intel Corporation | |
| Paul Durley | Intel Corporation | |
| Rahman Ismail | Intel Corporation | System Policy Lead |
| Sarah Sharp | Intel Corporation | |
| Scott Brenden | Intel Corporation | |
| Sridharan Ranganathan | Intel Corporation | |
| Steve McGowan | Intel Corporation | |
| Toby Opferman | Intel Corporation | |
| Kenta Minejima | Japan Aviation Electronics Industry Ltd. (JAE) | |
| Mark Saubert | Japan Aviation Electronics Industry Ltd. (JAE) | |

| | | |
|---|---|---|
| Toshio Shimoyama | Japan Aviation Electronics Industry Ltd. (JAE) | |
| Dave Thompson | LSI Corporation | |
| Geert Knapen | MCCI | |
| Chris Yokum | MCCI Corporation | |
| Marwan Kadado | Microsoft Corporation | |
| Randy Aull | Microsoft Corporation | |
| Yang You | Microsoft Corporation | |
| Frank Borngräber | Nokia Corporation | |
| Richard Petrie | Nokia Corporation | PD Vice-Chair/Device Policy Lead |
| Sten Carlsen | Nokia Corporation | Physical Layer WG Lead |
| Bart Vertenten | NXP Semiconductors | |
| Robert de Nie | NXP Semiconductors | |
| Robert Heaton | Obsidian Technology | |
| Cor Voorwinden | ON Semiconductor | |
| Edward Berrios | ON Semiconductor | Power Supply WG Lead |
| Tom Duffy | ON Semiconductor | |
| Narendra Mehta | Qualcomm, Inc. | |
| Terry Remple | Qualcomm, Inc. | |
| Yoram Rimoni | Qualcomm, Inc. | |
| Atsushi Mitamura | Renesas Electronics Corp. | |
| Atsushi Mitamura | Renesas Electronics Corp. | |
| Kiichi Muto | Renesas Electronics Corp. | |
| Masami Katagiri | Renesas Electronics Corp. | |
| Patrick Yu | Renesas Electronics Corp. | |
| Peter Teng | Renesas Electronics Corp. | |
| Steve Roux | Renesas Electronics Corp. | |
| Tetsu Sato | Renesas Electronics Corp. | |

| | | |
|---|---|---|
| Alvin Cox | Seagate Technology LLC | Cab Con WG Lead |
| John Hein | Seagate Technology LLC | |
| Marc Noblitt | Seagate Technology LLC | |
| Ronald Rueckert | Seagate Technology LLC | |
| Tony Priborsky | Seagate Technology LLC | |
| John Sisto | SMSC | |
| Ken Gay | SMSC | |
| Mark Bohm | SMSC | |
| Richard Wahler | SMSC | |
| Tim Knowlton | SMSC | |
| Fabien FRIESS | ST-Ericsson | |
| Giuseppe Platania | ST-Ericsson | |
| Jean-Francois Gatto | ST-Ericsson | |
| Nicolas Florenchie | ST-Ericsson | |
| Patrizia Milazzo | ST-Ericsson | |
| Anand Dabak | Texas Instruments | |
| Deric Waters | Texas Instruments | |
| Grant Ley | Texas Instruments | |
| Ivo Huber | Texas Instruments | |
| Jean Picard | Texas Instruments | |
| Martin Patoka | Texas Instruments | |
| Srinath Hosur | Texas Instruments | |
| Steven Tom | Texas Instruments | |
| Charles Neumann | Western Digital Technologies, Inc. | |
| Curtis Stevens | Western Digital Technologies, Inc. | |
| John Maroney | Western Digital Technologies, Inc. | |

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# 1. Introduction

## 1.1. Overview

The USB Power Supply Interface White Paper defineds a means of communicating with a Power Supply to support the requirements of the USB Power Delivery Specification

## 1.2. Purpose

This White Paper defines a Control/Status interface between the Device Policy Engine and the Power Supply. The Device Policy Engine in USB Power Delivery may use this interface to communicate with a Power Supply to provide the required Power (Voltage, Current) over VBUS.

## 1.3. Scope

The USB Power Supply Interface White Paper defines the general interface requirements for the interface in Chapter 2. Chapters 3 and 4 provide an example using SMBus as the interface.

## 1.4. Conventions

### 1.4.1. Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, and then text.

### 1.4.2. Keywords

Keywords differentiate between the levels of requirements and options.

#### 1.4.2.1. May

May is a keyword that indicates a choice with no implied preference.

#### 1.4.2.2. N/A

N/A is a keyword that indicates that a field or value is not applicable and has no defined value and shall not be checked or used by the recipient.

#### 1.4.2.3. Optional

Optional is a keyword that describes features not required by this White Paper. However, if an optional feature is implemented, the feature shall be implemented as defined by this White Paper (optional normative).

#### 1.4.2.4. Reserved

Reserved is a keyword indicating reserved bits, bytes, words, fields, and code values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this White Paper. A reserved bit, byte, word, or field shall be set to zero. Receipt of a non-zero value or a reserved code value in defined fields shall be treated as an error.

#### 1.4.2.5. Shall

Shall is a keyword indicating a mandatory requirement. Designers are required to implement all such requirements to ensure interoperability with other conformant Devices.

#### 1.4.2.6. Should

Should is a keyword indicating flexibility of choice with a preferred alternative. Equivalent to the phrase “it is recommended”.

### 1.4.3. Numbering

Numbers not immediately followed by a "b", “B”, or "h" are decimal values. Numbers that are immediately followed by a lowercase "b" (e.g., 01b) are binary values. Numbers that are immediately followed by an uppercase "B" are byte values. Numbers that are immediately followed by a lowercase "h" (e.g., 3Ah) are hexadecimal values.

## 1.5. Related Documents

1. USB Power Delivery 1.0 specification
2. SMBus 2.0 specification

## 1.6. Terms and Abbreviations

This section defines terms used throughout this document. For additional terms that pertain to the Universal Serial Bus, see Chapter 2, "Terms and Abbreviations," in USB Power Delivery 1.0 specification.

**Table 1-1 Terms and Abbreviations**

| Term | Description |
|---|---|
| Consumer | The capability of a port (typically a Device's upstream port) to sink power from the power conductor (e.g. $V_{BUS}$). |
| Consumer/Provider | A Consumer with the additional capability to act as a Provider. |
| DBO | Dead Battery Output |
| Device Policy Manager (DPM) | Module running in a Provider or Consumer that applies Local Policy to each port in the Device via the Policy Engine. |
| Hard Reset | This is initiated by a Hard Reset signaling from either port partner. It restores $V_{BUS}$ to the default condition and resets the PD communications engine to its default state. |
| PD | Power Delivery (USB Power Delivery) |
| PEC | Packet Error Code (See SMBus 2.0 specification) |
| Policy | Policy defines the behavior of PD capable parts of the system and defines the capabilities it advertises, requests made to (re)negotiate power and the responses made to requests received. |
| Policy Engine (PE) | The Policy Engine interprets the Device Policy Manager's input in order to implement Policy for a given port and directs the Protocol Layer to send appropriate messages. |
| Port | A USB connection; either upstream or downstream. Typically exposed through an A, B or AB connector, but also includes captive cables. USB Power delivery defines the interaction between a pair of attached ports. |
| Port Partner | Power Delivery is negotiated between two pors connected by a USB cable. The ports are port partners. |
| Provider | A capability of a port (typically a Host or Hub downstream port) to source power over the power conductor (e.g. $V_{BUS}$). |
| Provider/Consumer | A Provider with the additional capability to act as a Consumer. |
| PS | Power Supply |
| | |
| RWP | Read Word Protocol with PEC (See SMBus 2.0 specification) |
| Sink | The port consuming power from $V_{BUS}$; most commonly a Device. |
| Soft Reset | Resets the PD communications engine to its default state. |
| Source | A role a port is currently taking to supply power over $V_{BUS}$; most commonly a Host or Hub downstream port. |
| System Policy | Overall system policy generated by the system, broken up into the policies needed by each port pair to affect the system policy. It is programmatically fed to the individual Devices for consumption by their Policy Engines. |

| Term | Description |
|---|---|
| System Policy Manager | Module running on the USB Host. It applies the System Policy through communication with PD capable Consumers and Providers that are also connected to the Host via USB. |
| vSafeDB | Safe operating voltage for Dual-Role Ports operating as Dead Battery Source. |
| WDOG | Watch Dog Timer |
| WWP | Write Word Protocol with PEC (See SMBus 2.0 specification) |

# 2. Overview

## 2.1. Introduction

In Power Delivery, a Device Policy Engine can communicate with a Power Supply to provide the required Power (Voltage, Current) over VBUS.

## 2.2. Block Diagram

An example of a Power Supply interface is shown in Figure 2-1 PS Interface Block Diagram.

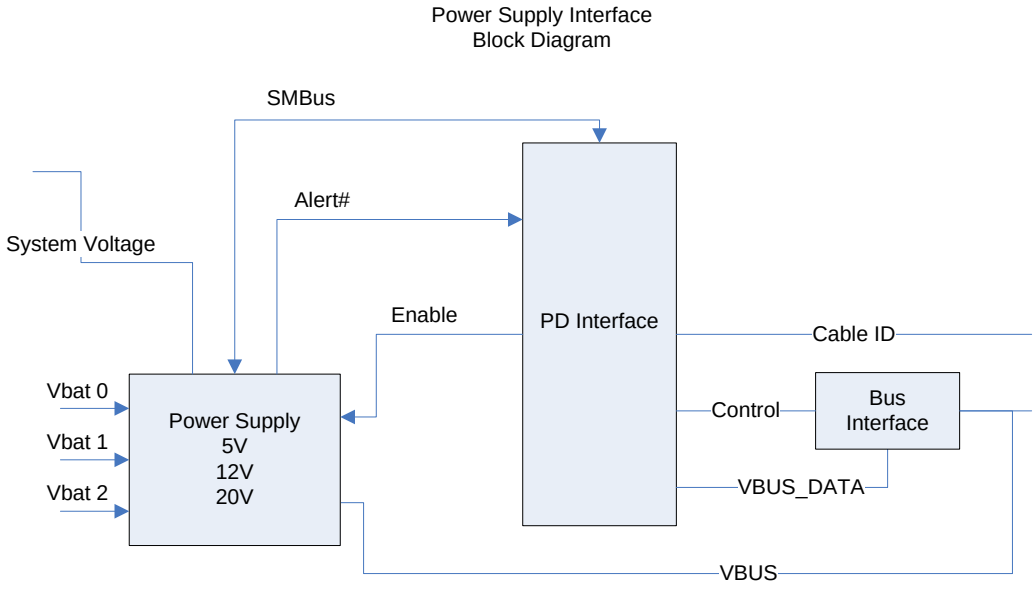


**Figure 2-1 PS Interface Block Diagram**

## 2.3. Assumptions

The following assumptions are made:

- Either the Device Policy Manager (DPM) or Policy Engine (PE) manages the Power Supply (PS) and is the bus master as appropriate for a given architecture.
- The Power Supply (PS) is the bus slave.
- Policy/Intelligence and knowledge of PD communication will reside outside of the Power Supply (PS).
- Power Supply control points are derived from the Policy Engine (PE) state machines.

## 2.4. Messages

### 2.4.1. Commands (to PS)

The following commands are implemented:

1. Reset
2. Set voltage (VBUS)
    a. Select Battery Voltage (optional)
    b. Monitor Minimum Battery Voltage (optional)

3. Set Current (iSet) – Identify expected current. This allows a power supply to optimize the power delivery. (i.e. If a power supply can provide 5V at 1mA, 3mA or 5mA, the power supply can use the "Set Current" to select the optimum power supply method.)
4. Set Current Limit (optional) – Limit used to detect over current situation by the power supply
5. Set Mode
    a. Source or Sink
    b. Dead Battery Support
    c. Watchdog Timer Support (optional)
6. Read average current over time (optional)
7. Input is now Stable (for Sink)
8. Goto Standby (to Sink)
9. Goto SwapStandby (0 current 0 voltage, {Sink or Source})
10. Alert Pin (Enable/Disable)

### 2.4.2. Status (from PS)

The following is the status that shall be reported by the PS

1. crowbar, over current, error conditions
2. Present voltage/current being supplied.
3. voltage/current change started/finished
4. PS Output Stable
5. Average current over time (optional)
6. Temperature (optional)

### 2.4.3. Alert ( from PS)

The following are the Alert events that shall be reported by the PS

1. Over current (optional)
2. Over Voltage (optional)
3. Under Voltage (optional)
4. Thermal Over Temp (optional)
5. Transition Complete
6. Hard Reset occurred
7. Invalid Command (optional)
8. Vbat Voltage below minimum (optional)

# 3. Physical Interface

1. Serial Bus for Messages ( SMBus, SPI)
2. Alert# Pin Output (from PS to DPM)
    a. Used to indicate change of state (crowbar, over current, voltage change completed, current change completed, error conditions)
    b. Active Low – will be active if enabled and any Alert Bits are set.
    c. This Pin is open drain, active low. (This allows wire "OR" with external resistor.)
3. Enable (from Phy to PS, PE and DPM)
    a. Used to turn off PS on a hard reset
    b. Used to reset DPM and PE state on a hard reset
    c. Active High – a "1"= output enabled (on); "0"=output disabled (off)

# 4. SMBus Command Implementation

## 4.1. Command Format

Refer to SMBus 2.0 specification:

1. Read Word Protocol with PEC (RWP)
2. Write Word Protocol with PEC (WWP)
3. The Address from the Register Map is used for the "Command Code" in the SMBus transfer.

### 4.1.1. Byte And Bit Order

As specified in the SMBus specification, Version 2.0:

1. When data is transmitted, the lowest order byte is sent first and the highest order byte is sent last.
2. Within any byte, the most significant bit (MSB) is sent first and the least significant bit(LSB) is sent last.

## 4.2. Register Map

| Address (SMBus Command) | Required Optional [2] | Parameter | Values | Command Type See Section 4.1 |
|---|---|---|---|---|
| 00h | R | Iset - 10mA units | See Section 4.3.1 | RWP; WWP |
| 01h | R | Vset - 50mV units | See Section 4.3.2 | RWP; WWP |
| 02h | R | Mode | See Section 4.3.3 | RWP, WWP |
| 03h | R | Alert | See Section 4.3.4 | RWP, WWP |
| 04h | R | Alert Shadow Register | See Section 4.3.5 | RWP |
| 05h | R | Status | See Section 4.3.6 | RWP |
| 06h | R | Alert Mask | See Section 4.3.7 | RWP, WWP |
| 07h | R | Manufacturer ID | See Section 4.3.8 | RWP |
| 08h | R | | | |
| 09h | R | | | |
| 0Ah | R | | | |
| 0Bh | R | Device ID | See Section 4.3.9 | RWP |
| 0Ch | R | PD/ Protocol Ver. | See Section 4.3.10 | RWP |
| 0Dh | O | Monitor V (50mV/bit) | See Section 4.3.11 | RWP |
| 0Eh | O | Monitor I (10mA/bit) [1] | See Section 4.3.12 | RWP |
| 0Fh | O | Monitor Temp | See Section 4.3.13 | RWP |
| 10h | O | Program Temp Trip | See Section 4.3.14 | RWP, WWP |
| 11h – 7Fh | O | Optional … | (Vendor Specific) | RWP, WWP |
| | | | | |

Table Notes:

1. Polarity is assumed based on the device function (source / sink). Value represents the magnitude.
2. "O" in this column means implementation is optional.

## 4.3. Register Definition

Register definitions include: b = active bit, 0 = unused bit, set to 0, f = fault (over or under flow)

### 4.3.1. Iset (Current Set)

Table 4-1 - Iset

| Bit(s) | Description |
|---|---|
| B15..10 | Reserved – shall be set to zero |
| B9..0 | Current in 10 mA units |

### 4.3.2. Vset (Voltage Set)

Table 4-2 Vset

| Bit(s) | Description |
|---|---|
| | |
| B15..12 | B15 B14 B13 B12<br>0 0 0 0 - Voltage defined by B9...0 (Fixed Power Supply)<br>1 0 0 1 - Connect Vbat0 to VBUS (optional)<br>1 0 1 0 - Connect Vbat1 to VBUS (optional)<br>1 1 0 0 - Connect Vbat2 to VBUS (optional) |
| B11..10 | Reserved – shall be set to zero |
| B9..0 | If B15 = 0; Voltage in 50 mV units<br>If B15 = 1; Minimum Battery Voltage in 50mV units (optional) |

### 4.3.3. Mode

Table 4-3 - Mode

| Bit(s) | Description |
|---|---|
| B15 | ON/OFF, (1 Bit)<br>0= OFF<br>1= ON |
| B14 | Source/Sink, (1 Bit)<br>0= Sink<br>1= Source |
| B13 | DBO, (1 Bit) – Dead Battery Output (VSafeDB) (Safe Operating Voltage for Dual-Role ports operating as Dead Battery Source)<br>1= Dead Battery Output |
| B12 | WDOG On/Off, (1 Bit) Opt<br>0= Off<br>1 = On |
| B11 | WDOG long/short, (1 Bit) Opt<br>0= WDOG short: 85msec (min) 95msec (max)<br>1= WDOG long: 170msec (min) 190msec (max)<br>WDOG timer is reset on any valid SMBus Transactions |

| Bit(s) | Description |
|---|---|
| B10 | Alert Pin<br>0 = Disabled<br>1= Enabled |
| B9 | Reset, (1 Bit)<br>0= No change<br>1= Reset – Reset chip to default power on state. This bit is self-cleared by hardware. |
| B8..5 | Reserved – shall be set to zero |
| B4..0 | Vendor Specific |

### 4.3.4. Alert

Alert bits are latched. A "1" value indicates an Alert event. The contents of the Alert register are ORed together and used to set the Alert output. The Mask register is used to disable individual Alert bits.
Alert register writes use a write "1" to clear. A "1" bit in the written word is used to clear just that bit.

Alert Register operation:
When the Alert register is read, the Alert# Pin is de-asserted (float).
When the Alert register is written with B0 set, the Alert Pin is re-enabled and will be active if any Alert Bits are active.

**Table 4-4 - Alert**

| Bit(s) | Description |
|---|---|
| B15 | Over Current |
| B14 | Over Voltage, Optional |
| B13 | Under Voltage, Optional |
| B12 | Thermal Over Temp, Optional |
| B11 | Hard Reset Occurred, (Disabled) |
| B10 | Transition Complete |
| B9 | Invalid Command, Optional |
| B8 | PEC Error, Optional |
| B7 | Watchdog, Optional |
| B6 | Vbat Voltage Below minimum as set in Vset (Optional) |
| B5..4 | Reserved – shall be set to zero |
| B3..1 | Vendor Specific |
| B0 | Alert Enable – writing a 1 to this bit enables the Alert pin. This bit is read as zero. |

### 4.3.5. Alert Shadow

This register can be used to poll the Alert bits. Reading this register does not disable the Alert# pin.

### 4.3.6. Status

Status represents real-time functionality. Bits may change when event changes.

Table 4-5 - Status

| Bit(s) | Description |
|---|---|
| B15 | Fault (any fault, over current, over temp, any other issues is present) |
| B14 | PS Output Stable |
| B13 | Output Enabled/Disabled (state of Enable input pin) |
| B12 | Alert Pin (state of Alert pin) (This bit is a "1" if driving the signal active.) |
| B11 | Output Impedance as per Power Delivery Specification vSafeDB |
| B10..6 | Reserved |
| B5..0 | Vendor specific |

### 4.3.7. Alert Mask

Set a bit to a "1" to mask (disable) an Alert bit position. The Alert register is bitwise ORed with the complement of the mask register to drive the Alert function. This allows a read of the Alert Register (or Alert Shadow Register) to be written to the mask register to disable all active Alerts. (This register shall default to all 1's on POR, Alarms are disabled.)

Table 4-6 - Alert Mask

| Bit(s) | Description |
|---|---|
| B15 | Over Current |
| B14 | Over Voltage |
| B13 | Under Voltage |
| B12 | Thermal Over Temp |
| B11 | Hard Reset Occurred |
| B10 | Transition |
| B9 | Invalid Command |
| B8 | PEC Error |
| B7 | Watchdog |
| B6 | Vbat Voltage Below minimum |
| B5..4 | Reserved – shall be set to zero |
| B3..1 | Vendor Specific |
| B0 | Reserved – shall be set to zero |

### 4.3.8. Manufacturer ID

Manufacturer ID may be a sequence of ASCII codes for a unique character string. (8 characters). It is up to the manufacturer to select a unique character string.

Table 4-7 - Manufacturer ID

| Address | Bit(s) | Description | Company "ABCDCORP" |
|---|---|---|---|
| 7h | B7..0 | 1st Character | "A" |
| | B15..8 | 2nd Character | "B" |
| 8h | B7..0 | 3rd Charcter | "C" |
| | B15..8 | 4th Character | "D" |
| 9h | B7..0 | 5th Character | "C" |
| | B15..8 | 6h Character | "O" |
| Ah | B7..0 | 7th Character | "R" |
| | B15..8 | 8th Character | "P" |

### 4.3.9. Device ID

Table 4-8 - Device ID

| Bit(s) | Description |
|---|---|
| B15..0 | Manufacturer Unique Device ID |

### 4.3.10. PD/ Protocol Ver.

Table 4-9 - PD Protocol Version

| Bit(s) | Description |
|---|---|
| B15..2 | Reserved – shall be set to zero |
| B1..0 | 00 = Power Delivery 1.0 |

### 4.3.11. Monitor V (50mV/bit)

Table 4-10 - Monitor Voltage

| Bit(s) | Description |
|---|---|
| B15 | 1 = Fault |
| B14..10 | Reserved – shall be set to zero |
| B9..0 | Voltage Low Limit in 50 mV units |

### 4.3.12. Monitor I (10mA/bit)

Table 4-11 - Monitor Current

| Bit(s) | Description |
|---|---|
| B15 | 1 = Fault |
| B14..10 | Reserved – shall be set to zero |
| B9..0 | Over Current Limit in 10 mA units |

### 4.3.13. Monitor Temperature

Table 4-12 - Monitor Temperature

| Bit(s) | Description |
|---|---|
| B15 | 1 = Fault |
| B14..0 | Temperature in 1/16 degrees,<br>0 to 255 C (12 bits) |

### 4.3.14. Program Temp Trip

Table 4-13 - Progammable Temperature Trip

| Bit(s) | Description |
|---|---|
| B15..0 | Temperature in 1/16 degrees<br>0 to 255 C (12 bits) |