USB4 GEN3 PLUG CONNECTOR HIGH SPEED DESIGN GUIDE

October 27, 2020

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REVISION HISTORY

Date	Version	Comments
06-29-2020	Rev. 1.0	First draft
10-27-2020	Rev. 1.1	Change “requirements” to “design guide” in the title

CONTENTS

1. INTRODUCTION

USB Type-C plug connector is the mating part for USB cable assembly, adaptor or thumb drive in many applications. Figure 1-1 shows an example of a USB cable assembly with plug connector. As an ingredient of a specific product, the plug connector has direct impact on the product performance. Quality control of the plug connector can help to improve the product performance.

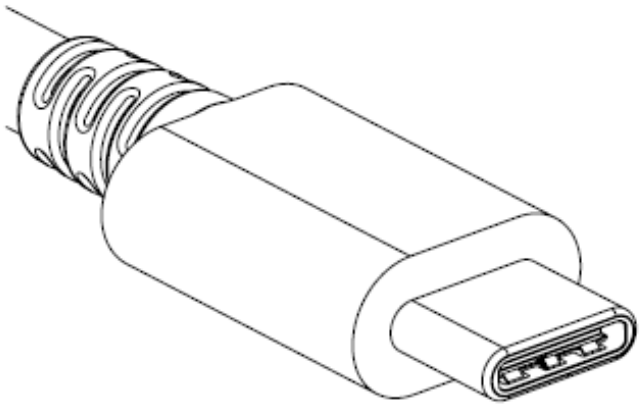


Figure 1-1: USB4 Gen3 Type C Cable

This document focuses on the high speed requirements and evaluation of the full-featured USB4 Gen3 Type-C plug connector. The pinout of a full-featured Type-C plug connector is shown in Figure 1-2.

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

Figure 1-2: Full-Featured Type-C plug Interface (Front View)

The purpose of this document is to help the plug connector vendors evaluate the plug performance and the cable/device manufacturers select right plug connector for the product.

Section 2 describes testing hardware for measuring the USB Type-C plug connector signal integrity performance and defines the recommended high speed signal integrity performance.

Section 3 provides a reference design of the test fixture used to evaluate USB4 Gen3 Type-C plug connector and test procedures.

Section 4 provides design considerations for the Type-C plug connector and the paddle card for signal integrity improvement.

This document is not part of the USB Type-C Connector specifications. Implementers may choose to deviate from the defined reference designs, but it is strongly recommended that the high speed requirements specified in this document be followed.

2. USB4 GEN3 PLUG CONNECTOR HIGH SPEED DESIGN GUIDE

A fixture is needed to evaluate the USB Type-C plug connector performance. This section describes what to evaluate for plug connector and high speed design guide for USB4 Gen3 Type-C plug connector.

2.1 Device under test (DUT)

The device under test (DUT) includes the interface on the PCB tongue, plug and interface on the paddle card.

2.1.1 PCB tongue

Instead of a USB Type C receptacle connector, a PCB tongue is used to represent the mating interface with USB4 Gen 3 Type-C plug connector, as illustrated in **Figure 2-1**. The PCB tongue provides a reliable and consistent interface performance when mating with different plugs.

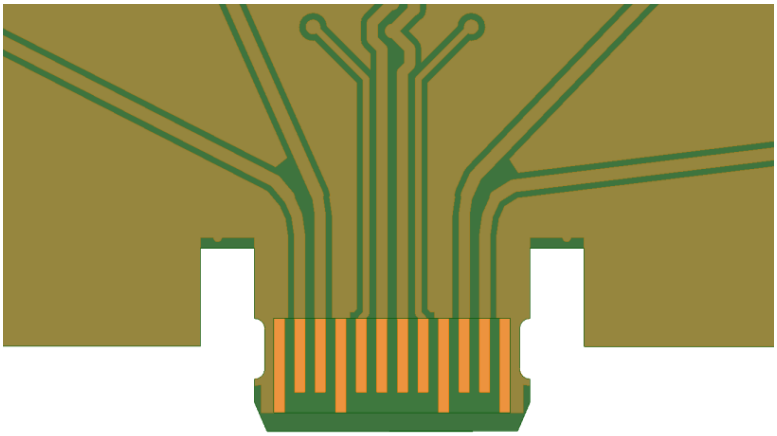


Figure 2-1: PCB tongue as receptacle

2.1.2 Plug connector

The USB Type C plug connector, as shown in **Figure 2-2**, is the stand-alone part to be manufactured. In a real application of the plug connector, itis mounted to a PCB or cable interface. The plug connector performance is not only related to plug connector itself, but also the PCB or cable interface.

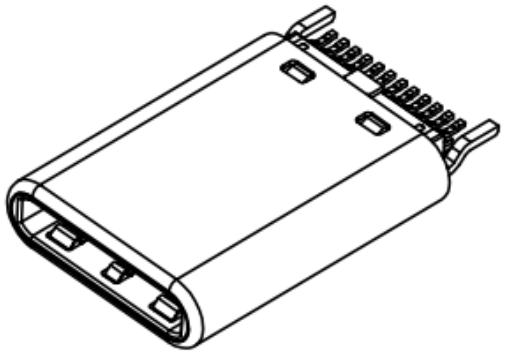


Figure 2-2: Plug connector

2.1.3 Plug PCB card

It is a common practice to attach a type-C plug connector on a paddle card, as shown in **Figure 2-3**. For a cable assembly, the paddle can help to manage wire termination of the Type-C cable and ensure electrical performance.

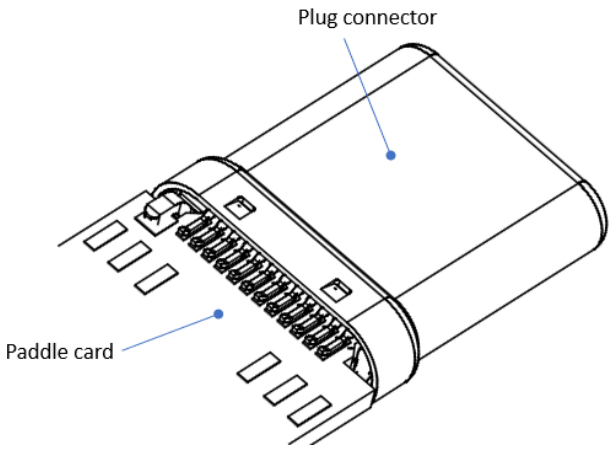


Figure 2-3: Plug connector attached on a paddle card

For plug connector testing, a PCB card is needed as well. The plug connector is soldered on the SMT pads at the edge of the PCB card. The SMT pad size is varied to match different plug connectors. **Figure 2-4** shows an example of the interface on a plug connector test fixture.

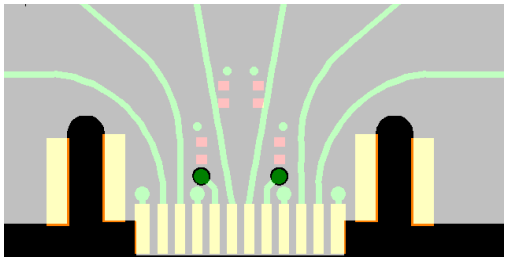


Figure 2-4: Plug PCB card and reference plane

2.2 Differential Impedance

The plug connector impedance target is specified to minimize reflection from the plug. The differential impedance of a plug connector should be within 85 Ω ± 9 Ω, as seen from a 40 ps (20% – 80%) rise time. The impedance profile of a plug connector should fall within the limits shown in Figure 2-5.

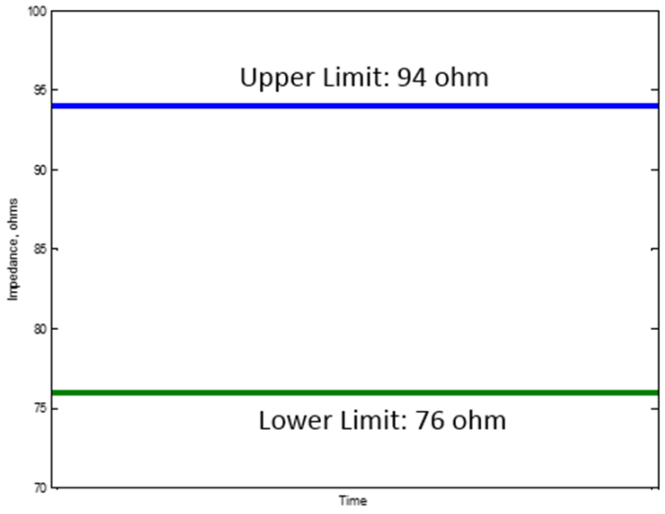


Figure 2-5 Recommended Impedance Limits of a USB Type-C Mated Connector

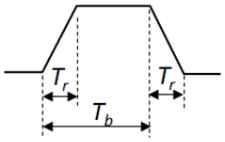
2.3 Differential Signal Integrity Characteristics

The frequency domain requirements of the USB4 Gen3 Type-C plug connector is listed in Table 2-1. Except for the differential to common mode conversion (SCD12 and SCD21), most of the item targets were specified using integrated S-parameters. The definition of the integrated S-parameters are the same as the USB4 Gen3 receptacle electrical requirements [1].

Table 2-1 USB Type-C plug Connector Signal Integrity Characteristics for USB4 Gen 3

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at a few different frequencies.	≥ −0.40 dB @ 2.5 GHz ≥ −0.55 dB at 5.0 GHz ≥ −0.75 dB @ 10 GHz ≥ −0.90 dB @ 12.5 GHz ≥ −1.10 dB @ 15 GHz5
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ Where: *ILD(f) = IL(f)-IL_fit(f)* • *IL(f)*: Insertion loss • *IL_fit(f)*: Insertion Loss fit - uses a smooth function to fit the IL to represent the signal.	≤ −38 dB
Integrated Differential Near-end Crosstalk on Tx/Rx (INEXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2\lvert NEXT(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXT* = NEXT between TX1 and RX1, and TX2 and RX2.	≤ −47 dB

Items	Descriptions and Procedures	Requirements
Integrated Differential Far-end Crosstalk on Tx/Rx (IFEXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\|Vin(f)\|^2\|FEXT(f)\|^2df}{\int_0^{f_{max}}\|Vin(f)\|^2df}}\right)$ where: *FEXT* = FEXT between TX1 and RX1, and TX2 and RX2.	≤ −47 dB
Differential Crosstalk of Tx/Rx on D+/D- Differential Crosstalk of D+/D- on Tx/Rx	The differential near-end and far-end crosstalk of the Tx/Rx pairs on the D+/D− pair in mated connectors, and the differential near-end and far-end crosstalk of the D+/D− pair on the Tx/Rx pairs in mated connectors. $dB\left(\sqrt{\frac{\int_0^{f_{max}}\|Vin(f)\|^2(\|NEXT(f)\|^2+\|FEXT(f)\|^2)df}{\int_0^{f_{max}}\|Vin(f)\|^2df}}\right)$ where: *FEXT* = Fare-end crosstalk between TX/Rx and D+/D- pairs, *NEXT* = Near-end crosstalk between TX/Rx and D+/D- pairs, and *fmax* =1.2 GHz.	≤ −60 dB
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\|Vin(f)\|^2\|SDD21(f)\|^2(\|SDD11(f)\|^2+\|SDD22(f)\|^2)df}{\int_0^{f_{max}}\|Vin(f)\|^2df}}\right)$	≤ −16 dB
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	≤ −25 dB
Notes: • *fmax* = 20 GHz (unless otherwise specified); • *Vin(f)* is defined in **Figure 2-6** with Tb (UI) = 50 ps; • *Vdd(f)* is also defined in **Figure 2-6** with Tb (UI) = 2.08 ns.		



$$|V_{in}(f)| = \left|\frac{\sin(\pi f T_r)}{\pi f T_r}\cdot\frac{\sin(\pi f T_b)}{\pi f T_b}\right|$$

T_b=Unit interval
T_r=0 to 100% rise time = $0.4T_b$

Figure 2-6 Input Pulse Spectrum

3. PLUG CONNECTOR TEST FIXTURE DESIGN

This section describes the reference design of test fixture used to evaluate the USB Type-C plug connector. The test fixture includes a Type-C PCB tongue (receptacle) board and Type-C plug board.

3.1 USB4 Gen3 Type-C PCB tongue board

The fixture for USB4 Gen3 cable assembly compliance testing will be used for plug connector testing [2]. The fixture is shown in **Figure 3-1**.

The fixture implements PCB tongue as the interface to plug. The PCB tongue is protected by the metal shell. 2X through traces are provided on the test board for calibration. Vertical 2.92 mm connectors are used for cable connection to the VNA during testing.

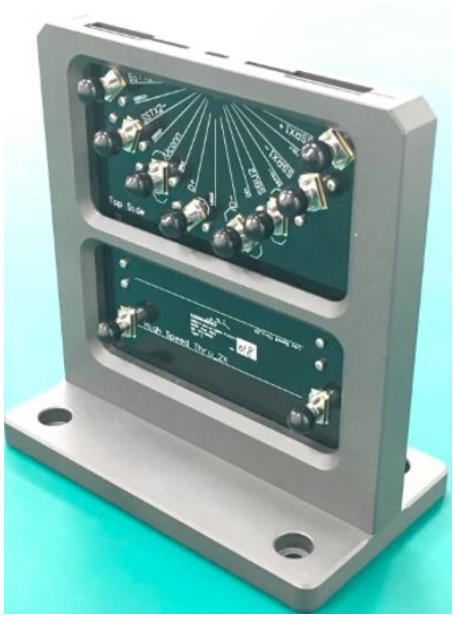


Figure 3-1: Illustration of PCB tongue test board

3.2 USB4 Gen3 plug connector board

The USB4 Gen3 Type-C high speed plug test card reference design is shown in **Figure 3-2**. 2X through calibration traces are located at both top and bottom layers. The trace length from the gold finger edge to the connector is 40 mm and the 2X through calibration traces are 78.48 mm. The plug locates at the center of the test card edge. Only the SuperSpeed pairs and one D+/D- pair are routed out to the 2.92 mm connectors. Unused pins are terminated with 50 ohm resistors. The V_{BUS} pins are designed as GND pins and connected to GND plane.

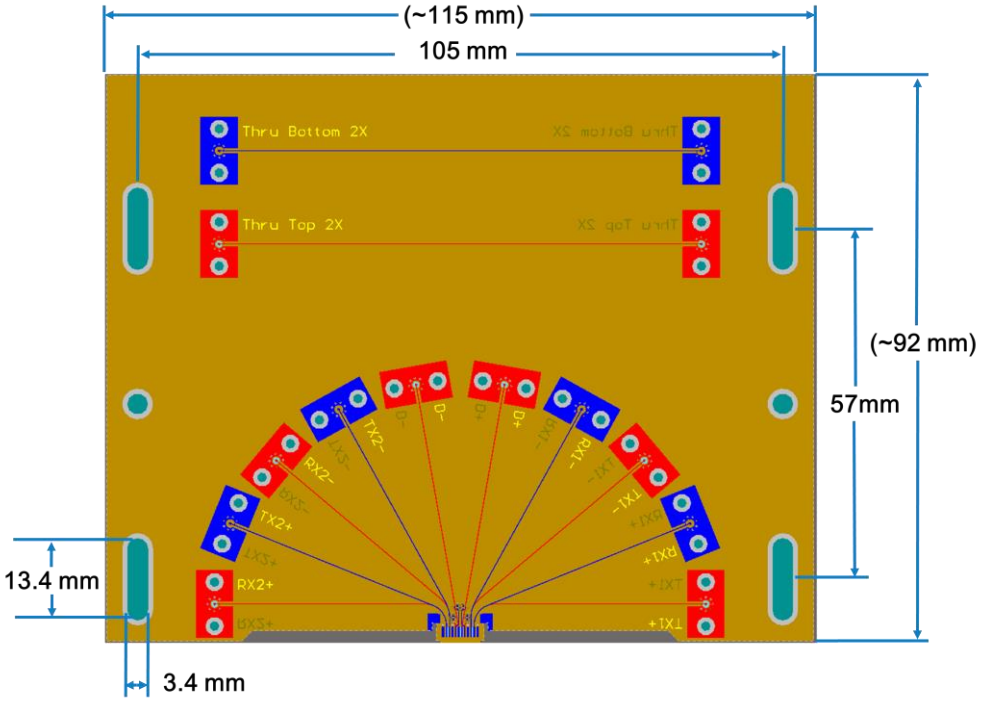


Figure 3-2 Reference design of plug connector test board

The USB4 Gen3 Type-C plug connector test card will be designed and built by USB4 Type-C plug vendor(s) or a designated test fixture vendor(s) by following the design rules.

- **PCB stackup**
  At least a 4-layer PCB with 0.8 mm thickness is required. Top and bottom layers are used for signal routing and all inner layers are used for GND plane. The dielectric thickness between the top or bottom layer to the adjacent reference plane is 0.1 mm (4 mils). Rogers or equivalent PCB dielectric material is recommended to minimize the fixture impedance variation and trace loss.

- **Signal connection**
  Figure 3-3 shows the signal connections for the fixture. Only the SuperSpeed pairs and the D+/D- pair are routed out to the 2.92 mm connectors. Unused pins are terminated with 50 ohm resistors. The V_{BUS} pins are designed as GND pins and connected to the GND plane.

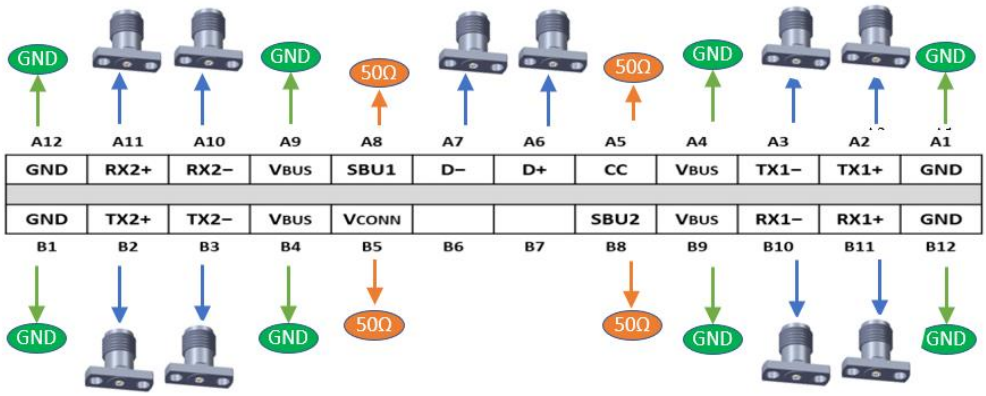


Figure 3-3 Signal schematic

- **Plug connector footprint and ground via placement**

  It is recommended to optimize the plug connector footprint and related ground voids underneath the SMT pads. The recommended ground via drill size is 0.2 mm, pad size is 0.4 mm and antipad size is 0.6 mm. The via to SMT pad edge distance is 0.3 mm, as shown in Figure 3-4

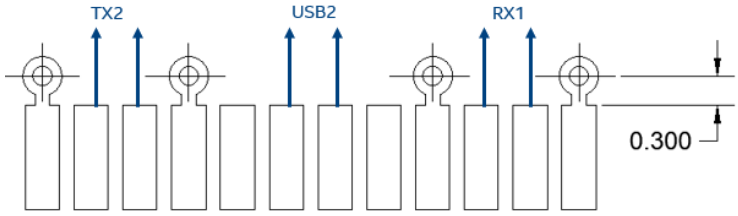


Figure 3-4 Reference design of plug connector test board

- **Calibration fixture**

  2X through calibration traces should be included in the receptacle test card. One is on the top layer and one is on the bottom layer.

- **Trace routing**

  All the traces on the test card should be single-ended with a characteristic impedance of 50 Ohms ± 5% (47.5 to 52.5 Ω). Traces between the reference plane and 2.92 mm connectors should be uncoupled from each other. Each trace length between the measurement reference plane and 2.92mm connectors should be less than
  40 mm and of equal length within a tolerance of +/- 0.025 mm.

- **Vertical 2.92 mm connector**

  2.9 2 mm vertical connectors are used on the test card, such as Molex 732520160 connector or equivalent. The 2.92 mm connector impedance should be 50 Ω and the impedance variation should be controlled within ± 5% as seen from a TDR of 40 ps (20%-80%).

- **Test card size and mounting holes**

  The USB4 mated connector test card is fragile once the VNA cables are connected. It is recommended to mount both the plug test card and the receptacle test card on a bracket for testing. An example of a mounted fixture is shown in Figure 3-1. The reference mounting holes size and location are shown in Figure 3-2.

3.3 Testing

This section describes the plug connector signal integrity testing equipment and procedures.

3.3.1 Reference equipment and setup

A VNA or equivalent equipment may be used for frequency domain measurements. If a VNA is used, its frequency range should be to at least 20 GHz for the SuperSpeed pairs (e.g., the Agilent 50 GHz PNA). Micro-coax precision 3.5 mm (e.g., UFB197C-1-0393) or 2.92 mm cables should be used to connect the VNA and test fixtures.

- The VNA should be powered on and allowed to warm up – recommendation is for 24 hours prior to measurement.

- For VNA bandwidth setup, it is recommended to limit the frequency sweep range to slightly higher than the limit required in the specification (e.g. a 20 GHz sweep range for the USB Type-C SuperSpeed pairs as

required by the spec). A sufficient number of points should also be included in the frequency sweep (for instance, a 10 MHz step for SuperSpeed pairs).

- The IF Bandwidth should be low enough to help reduce noise effects (e.g. < 300 Hz).

A TDR or equivalent equipment should be used for time domain measurements.

3.3.2 USB4 Gen3 plug connector measurements

All SuperSpeed measurements are done in frequency-domain with S-parameters. A VNA is typically used for such measurements, but other equivalent methods are allowed as long as the accuracy of the measured S-parameters is demonstrated. The following procedures apply for SuperSpeed signal measurements when using a VNA:

- The fixture effects should be removed from the measurements, using the calibration structures on both test boards. Allowed calibration methods include AFR and other equivalent methods with demonstrated accuracy and consistency. The de-embedded traces on the PCB tongue test board and the plug connector test board may have different lengths. The 2X through lines of both cards should be measured and used for calibration in right order.

- All measured S-parameters from a VNA are single-ended and they are converted to mixed mode through post processing.

- The measured frequency range shall be from 10 MHz to 20 GHz with a frequency step of 10 MHz.

- The measured S-parameters are processed by a Type-C compliance tool to do insertion loss fit and to calculate ILfitatNq, IMR, IRL, INEXT, IFEXT and other integrated parameters. The Type-C compliance tool may be downloaded from the following link:

  http://compliance.usb.org/files/

4. USB4 GEN3 PLUG CONNECTOR DESIGN CONSIDERATIONS

4.1 Plug Connector Design

The plug connector has contact pins secured in the plastic housing and is covered with metal shell. The RFI pad and mechanical latch were assembled to construct a complicated structure. To meet the high speed requirements, a few practices are recommended to be considered in plug connector design.

4.1.1 Ground middle plane

Due to the small form factor, the connector pins on the top side are very close to the pins on the bottom side. A ground middle plane can help to reduce the crosstalk from opposite side high speed differential pairs. **Figure 4-1** illustrates the ground middle plane within the plug connector. The ground middle plane is recommended to cover from tip to toe for better shielding.

With the ground middle plane, the high speed differential pair impedance may get impacted, optimization of the pin shape helps to adjust the plug connector impedance to meet the time domain requirement.

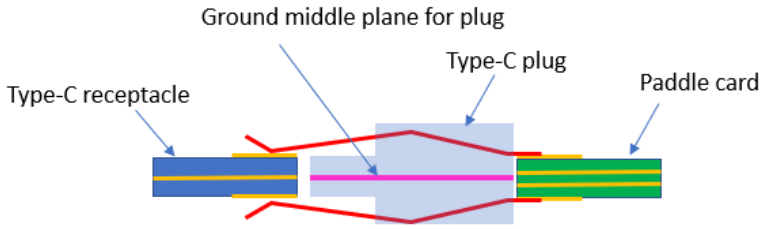


Figure 4-1 Ground middle plane for plug connector

4.1.2 Grounding mechanism

In the USB Type-C plug connector, there are several components connected to ground, such as the V_{SS} pin, side latch for mechanical retention, middle ground plane RFI pad, and shell. Any connection of those pieces to provide a short path will help in high speed performance improvement.

Figure 4-2 shows an example of plug connector structure. The side latch is integrated with GND middle plane, the V_{SS} pin is a separate part soldered to the paddle card, the GND middle plane connects to the paddle card, and the V_{SS} pin and GND middle plane are connected through the paddle card. If there is a design to overcome the manufacturing challenge to connect the V_{SS} pin and the GND middle plane at either position 1 or position 2 as shown in **Figure 4-2**, then it helps to improve the plug connector high speed performance.

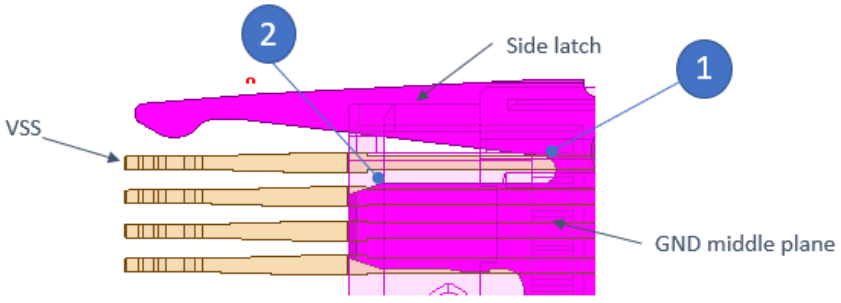


Figure 4-2 Grounding mechanism of USB Type-C plug connector

4.2 Paddle Card Design

The USB Type-C plug connector is designed to be mounted on a PCB called a paddle card. The interface between the plug connector and the paddle card has impact on the plug connector performance. Attention on the interface design is recommended to be able to meet plug connector high speed requirements.

4.2.1 Voids in the reference ground plane

Voids in the reference ground plane should be considered to meet the plug connector impedance requirement. One example of voiding is shown in **Figure 4-3**. Two USB4 type-C mated connector models were generated to check the impedance difference as shown in **Figure 4-4**. The model without ground voids has low impedance at the paddle card interface. The low impedance issue can be fixed with voids on the layer 2 reference ground plane. The size of the voids can be adjusted based on the paddle card stackup and pad size of the SuperSpeed pair.

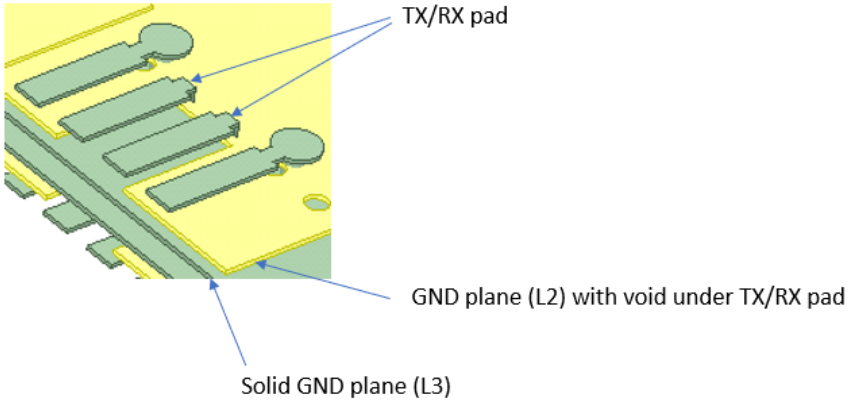


Figure 4-3 Voiding on ground reference plane

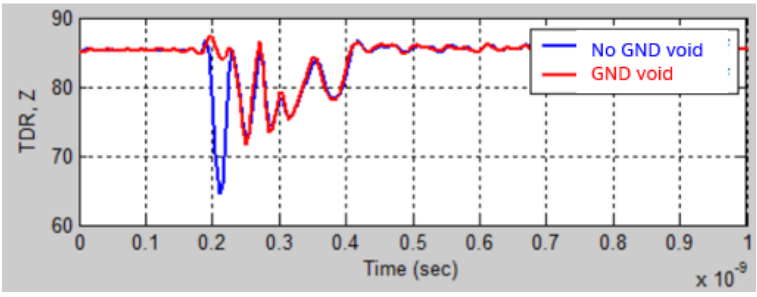


Figure 4-4 Impedance difference between two Type C mated connector models

4.2.2 Paddle card stackup design

For a four layer paddle card design, when voids on the reference ground plane were implemented for impedance adjustment, more crosstalk was observed between TX1/RX1 and TX2/RX2. An additional ground layer, shown in **Figure 4-3** , was added to the paddle card stackup to reduce the crosstalk. Three USB Type-C mated connector models were generated for comparisons.

- 4-layer paddle card with GND voids
- 4-layer paddle card without GND voids

- 6-layer paddle card with GND voids on Layer 2 and Layer 5

The DDNEXT comparisons are shown in **Figure 4-5**.

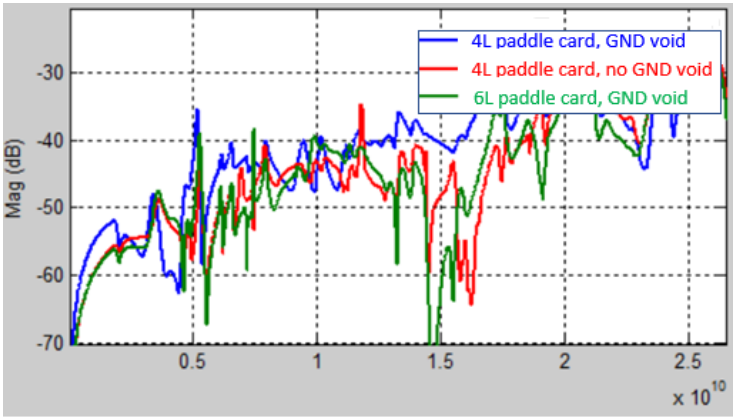


Figure 4-5 TX/RX DDNEXT comparisons

The mated connector with the 4-layer paddle card and GND voids has more crosstalk than the other mated connectors. To keep voids on ground layers for impedance control, 6 layer stackup should be considered for crosstalk improvement.

5. SUMMARY

This document summarizes the USB4 Gen3 Type-C plug connector and its interfaces for application. The high speed requirements of the USB4 Gen3 Type-C plug connector were introduced with guidelines of reference fixture design. A few design practices for the USB4 Gen3 Type-C plug connector were recommended for connector manufacturer's consideration.

The USB4 Gen3 Type-C plug connector which passes the high speed requirement does not guarantee the cable assembly will pass compliance testing. Cable manufacturers use this document as reference when selecting a USB4 Gen3 Type-C plug connector for cable assembly or device design.

6. REFERENCES

1. Universal Serial Bus Type-C Cable and Connector Specification. Release 2.0 April 2020
2. Universal Serial Bus Type-C Connectors and Cable Assemblies Compliance Document. Revision 2.1a June 2020 (To be released)