USB4™ DP Tunneling
Compliance Test Specification

Date: December 2022

Revision: 1.5

Revision History:

Revision	Issue Date	Comments
1.0	January 2021	First Release
1.1	October 2021	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.2	December 2021	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.3	March 2022	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.4	October 2022	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.5	December 2022	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021 and includes additional ECN through October 2022.

Contents

Tables

Introduction

The tests in this specification verify that a USB4 Product is compliant with Chapter 10 of the USB4™ Specification.

Reference Documents

- Universal Serial Bus 4 (USB4™) Specification Version 1.0 August, 2019 (USB4 Specification)
- VESA DisplayPort (DP) Standard Version 1.4a 19 April, 2018 (DP 1.4a Specification)
- VESA DisplayPort v1.4a Link Layer Compliance Test Specification Revision 1.0 June 12, 2019 (DP Link CTS)
- VESA DP 1.4a Link CTS rev 1.0 Errata E3 Published 11/15/19 include for DPTXs: (DP Link CTS Errata)
    - DisplayPort DSC Link Layer Compliance Test Specification
    - DSC Link Layer Compliance Test Rev 1.0 SCR on Simple 422 CRC
    - DSC Link Layer Compliance Test Rev 1.0 SCR on Line Buffer Bit Depth
    - DP1.4a Link CTS r1.0 SCR AUX reply timeout d2
- High-bandwidth Digital Content Protection Revision 2.3 on DisplayPort Compliance Test Specification Revision 1.1 4 March 2019 (HDCP CTS for DP)
- Universal Serial Bus 4 (USB4™) Connection Manager Guide

Assertions

Compliance criteria are provided as a list of assertions that describe specific characteristics or behaviors that must be met. Each assertion provides a reference to the USB4 specification or other documents from which the assertion was derived. In addition, each assertion provides a reference to the specific test description(s) where the assertion is tested.

Each test assertion is formatted as follows:

Assertion #	Test #	Assertion Description

Assertion#: Unique identifier for each spec requirement. The identifier is in the form USB4_SPEC_SECTION_NUMBER#X, where X is a unique integer for a requirement in that section.

Assertion Description: Specific requirement from the specification

Test #: A label for a specific test description in this specification that tests this requirement. Test # can have one of the following values:

NT	This item is not explicitly tested in a test description. Items can be labeled NT for several reasons – including items that are not testable, not important to test for interoperability, or are indirectly tested by other operations performed by the compliance test.
X.X	This item is covered by the test described in test description X.X in this specification.
IOP	This assertion is verified by the USB4 Interoperability Test Suite.

Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

Chapter 10 Assertions

The following Table presents the USB4 Specification Chapter 10 asserts.

Assertion #	How to Test	Assertion Description
10 DisplayPort Tunneling		
10#1	TD 10.003	A USB4 host shall support DP tunneling.
10#2	TD 10.003	A Host Router shall contain at least one DP IN Adapter and may optionally contain one or more DP OUT Adapters.
10#3	TD 10.003	A USB4 hub shall support DP Tunneling.
10#4	TD 10.003	A USB4 Hub shall contain at least one DP OUT Adapter and may optionally contain one or more DP IN Adapters.
10#5	NT	If a USB4 peripheral device supports DP Tunneling, it shall contain at least one DP Adapter.

10.1 DP Adapter Port Protocol Stack		
10.1.1 Transport Layer		
10.1.2 Protocol Adapter Layer		
10.1.3 DP Physical Layer		
10.1.3#1	TD 10.003 TD 10.003	A DP Adapter Port shall either implement the DisplayPort Physical Layer as defined in the DisplayPort 1.4a Specification or shall implement its functional equivalent (e.g. DP Adapter Port is connected to a DPRX or a DPTX as part of an SoC).
10.1.3#2	NT	A DP IN Adapter Port which does not implement a Physical Layer shall generate a stream of DisplayPort Tunneled packets as if a Physical Layer exists.
10.2 DP Adapter States		
10.2.1 Reset		
10.2.1#1	TD 10.003 TD 10.003	While in the Reset state, a DP Adapter shall set all Configuration Spaces to their default values.
10.2.1#2	NT	A DP IN Adapter shall drive HPD signal low.
10.2.1#3	NT	A DP OUT Adapter shall not apply DP_PWR.
10.2.2 Present		
10.2.2#1	TD 10.003 TD 10.003	While in the Present state, a DP Adapter shall set all Configuration Spaces to their default values.
10.2.2#2	NT	A DP IN Adapter Port shall drive HPD signal low.
10.2.2#3	NT	A DP OUT Adapter Port shall not apply DP_PWR.
10.2.3 Plugged		
10.2.3#1	NT	While in the Plugged state, a DP IN Adapter shall drive HPD signal low.

10.2.4 Paired		
10.3 Interfaces		
10.3.1 DisplayPort		
10.3.1#1	NT	A DP Adapter shall support three modes of operation: LTTPR Non-Transparent – LT-tunable PHY Repeater (Non-Transparent Mode); LTTPR Transparent – LT-tunable PHY Repeater (Transparent Mode); Non-LTTPR – Non-LT-tunable PHY Repeater.
10.3.1#2	NT	After reset, a DP Adapter shall operate in Non-LTTPR mode.
10.3.1#3	NT	A DP Adapter shall transition between the three modes as described in Section 10.4.6.1.
10.3.1#4	NT	A DP Adapter shall transition to Non-LTTPR mode upon exit from the Paired state.
10.3.1.1 LTTPR Non-Transparent		
10.3.1.1#1	NT	A DP IN Adapter shall implement LTTPR UFP.
10.3.1.1#2	NT	A DP OUT Adapter shall implement LTTPR DFP.
10.3.1.2 Non-LTTPR		
10.3.1.2#1	NT	A DP IN Adapter shall implement Non-LTTPR Non-Transparent UFP.
10.3.1.2#2	NT	A DP OUT Adapter shall implement Non-LTTPR Non-Transparent DFP.
10.3.1.3 LTTPR Transparent		
10.3.2 Programming Model		
10.3.2.1 Adapter Configuration Space		
10.3.2.2 Path Configuration Space		
10.3.2.2#1	TD 10.003 TD 10.003	A DP Adapter shall implement a Path Configuration Space as defined in Section 8.2.3.
10.3.2.2#2	NT	A DP Adapter shall support one MAIN-Link Path, one AUX Ingress Path, and one AUX Egress Path.

10.3.3 Hot Plug and Hot Removal Events		
10.3.3.1 DP OUT Adapters		
10.3.3.1#1	NT	When a DP OUT Adapter detects a Plug Event (as defined in the DisplayPort 1.4a Specification), it shall: Send a Hot Plug Event Packet with the UPG bit set to 0b as described in Section 6.8 within tDPPlug.
10.3.3.1#2	NT	When a DP OUT Adapter detects a Plug Event (as defined in the DisplayPort 1.4a Specification), it shall: Set the Plugged bit to 1b.
10.3.3.1#3	NT	When a DP OUT Adapter detects an Unplug Event (as defined in the DisplayPort 1.4a Specification), it shall: Send a Hot Plug Event Packet with the UPG bit set to 1b as described in Section 6.8 within tDPPlug.
10.3.3.1#4	NT	When a DP OUT Adapter detects an Unplug Event (as defined in the DisplayPort 1.4a Specification), it shall: Set the Plugged bit to 0b
10.3.3.2 DP IN Adapters		
10.3.3.2#1	NT	A Router shall send a Hot Plug Event Packet as described in Section 6.8 within tDPPlug of when both of the following are true: A DP IN Adapter detects a Source (as defined in the DisplayPort 1.4a Specification); The DP IN Adapter that detected the Plug Event has sufficient DP stream resources available to support a DP stream.
10.3.3.2#2	NT	A Router shall send a Hot Plug Event Packet with the *UPG* bit set to 1b as described in Section 6.8 within tDPPlug of when either of the following are true: A DP IN Adapter detects the removal of a Source (as defined in the DisplayPort 1.4a Specification); The Router has freed the DP stream resources allocated to the DP IN Adapter such that the DP IN Adapter can no longer support a DP stream.
10.3.3.2.1 DP Stream Resource Allocation		
10.3.3.2.1#1	NT	A Router shall support the DP Stream Resource Commands listed in Table 10-3 (QUERY_DP_RESOURCE, ALLOCATE_DP_RESOURCE, DEALLOCATE_DP_RESOURCE)
10.3.4 DisplayPort Over USB4 Fabric		
10.3.4.1 DisplayPort Data Packet Types		
10.3.4.1#1	NT	The Tunneled Packets types defined in Table 10-4 shall only be used for the AUX Path.
10.3.4.1#2	NT	The Tunneled Packet Types defined in Table 10-5 shall only be used for the Main-Link Path.
10.3.4.1#3	NT	If a DP Adapter receives a Tunneled Packet on the AUX Path with a PDF value other than 0 to 3, it shall discard the Tunneled Packet and shall not send any Packets in response.

10.3.4.1#4	NT	If a DP OUT Adapter receives a Tunneled Packet on the Main-Link Path with a PDF value other than 1 to 7, it shall discard the Tunneled Packet and shall not send any Packets in response.
10.3.4.2 AUX Path Packets		
10.3.4.2#1	NT	When generating an AUX Path Packet, a DP Adapter Layer shall put the value in the *AUX Tx HopID* field into the *HopID* field of the Tunneled Packet header.
10.3.4.2#2	NT	When a DP Adapter Layer receives a Tunneled Packet with a HopID that is equal to the *AUX Rx HopID* field, it shall treat that packet as an AUX Path Packet.
10.3.4.2.1 AUX Packets		
10.3.4.2.1#1	NT	An AUX Packet shall have the format shown in Table 10-7.
10.3.4.2.1#2	NT	The Tunneled Packet Header for an AUX Packet shall have the *PDF* field set to 0.
10.3.4.2.1#3	NT	AUX Packet payload shall contain the following: **CRC**: See Section 10.3.4.2.1.1.
10.3.4.2.1#4	NT	AUX Packet payload shall contain the following: **AUX Payload**: Shall contain the bytes contained between the <SYNC> and <STOP> framing bytes of a DisplayPort AUX transaction. The number of bytes in this field varies between 1 and 20.
10.3.4.2.1#5	NT	AUX Packet payload shall contain the following: **Reserved**: Shall be one byte set to 00h.
10.3.4.2.1.1 CRC		
10.3.4.2.1.1#1	NT	The CRC32 computation in an AUX Packet shall be based on the following CRC: Width: 32 Poly: 1EDC 6F41h Init: FFFF FFFFh RefIn: True RefOut: True XorOut: FFFF FFFFh
10.3.4.2.1.1#2	NT	If the AUX Payload is less than 21 bytes in length, a DP Adapter shall add the required number of zero-padding bytes for the computation of the CRC.
10.3.4.2.1.1#3	NT	The padding bytes shall not be transmitted in the AUX Packet.

10.3.4.2.1.1#4	NT	The CRC32 shall be generated by the DP Adapter that creates the AUX Packet and shall be checked by the DP Adapter that receives the AUX Packet
10.3.4.2.1.1#5	NT	A DP Adapter that receives an AUX Packet with a CRC error shall drop that packet.
10.3.4.2.2 HPD Packets		
10.3.4.2.2#1	NT	An HPD Packet shall have the format shown in Figure 10-8.
10.3.4.2.2#2	NT	The *PDF* field in the header shall be set to 1 and the *Length* field shall be 4.
10.3.4.2.2#3	NT	HPD Packet payload shall contain the following: **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the HPD Packet payload.
10.3.4.2.2#4	NT	HPD Packet payload shall contain the following: **Reserved [30:8]**: Shall be set to 0.
10.3.4.2.2#5	NT	HPD Packet payload shall contain the following: **Plug (P) Flag [Bit 31]**: Shall be set to 0 if the HPD signal is low for more than 2 ms. Shall be set to 1 if the HPD signal is high.
10.3.4.2.2#6	NT	When a DP IN Adapter receives an HPD Packet, it shall check the *ECC* field of the packet payload.
10.3.4.2.2#7	NT	The DP IN Adapter shall correct single-bit errors in the HPD Tunneled Packet payload.
10.3.4.2.2#8	NT	If an uncorrectable error is detected, the HPD Packet shall be dropped.
10.3.4.2.2#9	NT	Otherwise the DP IN Adapter shall: Generate a Plug/Re-plug HPD event if the P Flag in the HPD Packet payload is set to 1b.
10.3.4.2.2#10	NT	Otherwise the DP IN Adapter shall: Generate an Unplug HPD event if the *P Flag* in the HPD Packet payload is set to 0b.
10.3.4.2.2#11	NT	Otherwise the DP IN Adapter shall: Acknowledge the HPD Packet by sending an ACK Packet to the DP OUT Adapter within tDPAckResponse of receiving the HPD Packet.
10.3.4.2.3 SET_CONFIG Packet		
10.3.4.2.3#1	NT	A SET_CONFIG Packet shall have the format shown in Figure 10-9.
10.3.4.2.3#2	NT	The *PDF* field in the header shall be set to 2 and the *Length* field shall be 4.

10.3.4.2.3#3	NT	SET_CONFIG Packet payload shall contain the following: **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the SET_CONFIG Packet payload.
10.3.4.2.3#4	NT	SET_CONFIG Packet payload shall contain the following: **Link Rate 0 (LR0) [8]**.
10.3.4.2.3#5	NT	SET_CONFIG Packet payload shall contain the following: **Lane Count (LC) [11:9]**.
10.3.4.2.3#6	NT	SET_CONFIG Packet payload shall contain the following: **Reserved [12]**: This field shall be set to 1b by sender and ignored by receiver.
10.3.4.2.3#7	NT	SET_CONFIG Packet payload shall contain the following: **Link Rate 1 (LR1) [13]**.
10.3.4.2.3#8	NT	SET_CONFIG Packet payload shall contain the following: **Training Pattern Support (TPS) [15:14]**: This field shall specify the supported TPS which can be used in EQ Phase in Non-LTTPR and LTTPR Transparent link training.
10.3.4.2.3#9	NT	SET_CONFIG Packet payload shall contain the following: **TPS3 Support [14]**.
10.3.4.2.3#10	NT	SET_CONFIG Packet payload shall contain the following: **TPS4 Support [15]**.
10.3.4.2.3#11	NT	SET_CONFIG Packet payload shall contain the following: **MSG Data [31:24]**.
10.3.4.2.3#12	NT	SET_CONFIG Packet payload shall contain the following: **MSG Data [31:24]**.
10.3.4.2.3#13	NT	The MSG Data shall match the MSG Type of the packet as set forth in Table 10-5.
10.3.4.2.3#14	NT	A DP IN Adapter shall set the *LC* and *LR* fields in all SET_CONFIG Packets to be the same as the last SET_LINK SET_CONFIG Packet it sent.
10.3.4.2.3#15	NT	A DP OUT Adapter shall set the *LC* and *LR* fields in all SET_CONFIG Packets to be the same as the last SET_LINK SET_CONFIG Packet it received.
10.3.4.2.3#16	NT	After a DP Adapter sends a SET_CONFIG Packet, it shall wait for an ACK Packet with the *Type* field equal to 0h.
10.3.4.2.3#17	NT	After receiving an ACK Packet with the *Type* field set to 0h, the DP Adapter shall wait tDPSetConfigGap before sending the next SET_CONFIG Packet.
10.3.4.2.3#18	NT	When a DP Adapter receives a SET_CONFIG Packet, it shall check the *ECC* field of the packet payload.

10.3.4.2.3#19	NT	The DP Adapter shall correct single-bit errors in the SET_CONFIG Packet payload.
10.3.4.2.3#20	NT	If an uncorrectable error is detected, the SET_CONFIG Packet shall be dropped.
10.3.4.2.3#21	NT	Otherwise, the DP Adapter shall respond with an ACK Packet with the *Type* field equal to 0h.
10.3.4.2.3#22	NT	The ACK Packet shall be sent within tDPAckResponse of receiving the SET_CONFIG Packet.
10.3.4.2.3#23	NT	A DP Adapter that receives a SET_CONFIG Packet with a value in the *Type* field that is not listed in Table 10-5 shall respond with an ACK packet with the *Type* field equal to 0h.
10.3.4.2.4 ACK Packet		
10.3.4.2.4#1	NT	An ACK Packet shall have the format shown in Figure 10-10.
10.3.4.2.4#2	NT	The *PDF* field in the header shall be set to 3 and the *Length* field shall be 4.
10.3.4.2.4#3	NT	ACK Packet payload shall contain the following: **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the ACK Packet payload.
10.3.4.2.4#4	NT	ACK Packet payload shall contain the following: **Reserved [27:8]**: Shall be set to 0.
10.3.4.2.4#5	NT	ACK Packet payload shall contain the following: Type [31:28]: Shall be set to 8h to acknowledge the receipt of a HPD Packet. Shall be set to 0h to acknowledge the receipt of a SET_CONFIG Packet. All other values are reserved.
10.3.4.3 MAIN-Link Path Packet Formats		
10.3.4.3#1	NT	When generating a Main-Link Path Packet, a DP IN Adapter Layer shall put the value in the *Video HopID* field into the *HopID* field of the Tunneled Packet header.
10.3.4.3#2	NT	When a DP OUT Adapter Layer receives a Tunneled Packet with a HopID that is equal to the *Video HopID* field, it shall treat that packet as a Main-Link Path Packet.

10.4 System Flows		
10.4.1 Connection Manager Discovery		
10.4.2 Path Configuration		
10.4.2.1 Setup		
10.4.2.1#1	NT	A DP OUT Adapter shall poll the DP_STATUS.*CMHS* field and DP_REMOTE_CAP.*Protocol Adapter Version* field for as long as the values in those fields are both 0.
10.4.2.1#2	NT	When either DP_STATUS.CMHS = 1 or DP_REMOTE_CAP.*Protocol Adapter Version* > 0, the DP OUT Adapter shall do the following: If DP_REMOTE_CAP.*Protocol Adapter Version* was set to non-zero value while DP_STATUS_CTRL.*CMHS* remained zero, a DP OUT Adapter shall conclude it is a TBT3 Connection Manager and shall continue the flow as defined in Section 13.8.3.
10.4.2.1#3	NT	When either DP_STATUS.CMHS = 1 or DP_REMOTE_CAP.*Protocol Adapter Version* > 0, the DP OUT Adapter shall do the following: If DP_STATUS_CTRL.*CMHS* is set to 1 and DP_STATUS_CTRL.*UF* is zero, a DP OUT Adapter shall conclude it is a TBT3 DP IN Adapter and shall continue the flow as defined in Section 13.8.3.
10.4.2.1#4	NT	When either DP_STATUS.CMHS = 1 or DP_REMOTE_CAP.*Protocol Adapter Version* > 0, the DP OUT Adapter shall do the following: If DP_STATUS_CTRL.*CMHS* is set to 1 and DP_STATUS_CTRL.*UF* is set to one, a DP OUT Adapter shall reset DP_STATUS_CTRL.*CMHS* to zero.
10.4.2.1#5	TD 10.1 TD 10.9	A DP Adapter shall set the DP_COMMON_CAP register, to reflect the lowest common capability between DP_LOCAL_CAP and DP_REMOTE_CAP fields.
10.4.2.2 Tear-down		
10.4.2.2#1	TD 10.1 TD 10.9	When the *ADP_DP_CS_0.AE* bit and the *ADP_DP_CS_0.VE* bit are both set to 0, a DP Adapter shall set all the fields in its DP Adapter Configuration Capability to their default values.
10.4.3 HPD Event Propagation		
10.4.3.1 HPD Plug		
10.4.3.1#1	NT	After a Path is setup between a DP OUT Adapter and a DP IN Adapter per 10.4.2.1, the DP OUT Adapter shall send an HPD Packet with the *P Flag* set to 1b.
10.4.3.1#2	NT	Upon receiving an HPD Packet with the *P Flag* set to 1b, the DP IN Adapter shall respond with an ACK Packet, execute the DP Adapter Init flow as defined in Section 10.4.5, and then drive HPD signal high on the DisplayPort interface

10.4.3.1#3	NT	After the DP IN Adapter drives HPD high, both DP Adapters shall be ready to handle AUX transactions.
10.4.3.2 HPD Unplug		
10.4.3.2#1	NT	Upon unplug detection, the DP OUT Adapter shall send an HPD Packet with the *P Flag* set to 0b to the DP IN Adapter.
10.4.3.2#2	NT	The DP IN Adapter shall respond with an ACK Packet and drive the HPD signal low.
10.4.3.2#3	NT	When the HPD signal is low, a DP IN Adapter may disable its DP Link receiver.
10.4.3.3 IRQ		
10.4.3.3#1	NT	Upon IRQ detection, a DP OUT Adapter shall send a SET_CONFIG Packet of MSG type IRQ to the DP IN Adapter.
10.4.3.3#2	NT	A DP IN Adapter that receives a SET_CONFIG Packet of MSG type IRQ shall respond with an ACK Packet and drive the IRQ event (according to the DisplayPort 1.4a Specification) towards the DPTX.
10.4.3.3#3	NT	However, if Link training is in process or it just ended, a DP OUT Adapter shall wait tIRQDelay after it sent a SET_CONFIG Packet to the DP IN Adapter (reporting that Link training is completion) before sending the IRQ SET_CONFIG Packet.
10.4.3.4 HPD Delay Requirements		
10.4.3.4#1	NT	Table 10-7 defines the maximum propagation delay through the DP Adapters that shall be used for HPD Events.
10.4.3.4#2	NT	The propagation delay through the DP OUT Adapter shall be measured from when the event is detected by the DP OUT Adapter to when the last bit of the corresponding packet, SET_CONFIG or HPD, is sent over the AUX Path.
10.4.3.4#3	NT	The propagation delay through the DP IN Adapter shall be measured from when the last bit of an HPD Event Packet, SET_CONFIG or HPD, arrives at the DP IN Adapter to when event is driven on the HPD signal.
10.4.3.4#4	NT	A DP OUT Adapter shall send HPD packet with the *P Flag* set to 1b within tDPPlug of transitioning to the Paired state.
10.4.3.5 Manual HPD Control		
10.4.3.5#1	TD 10.003	When HPDC transitions from 0b to 1b, a DP IN Adapter shall drive the DisplayPort HPD signal low.
10.4.3.5#2	TD 10.003	When HPDS transitions from 0b to 1b, a DP IN Adapter shall drive the DisplayPort HPD signal high.

10.4.3.5#3	TD 10.003	The DisplayPort HPD signal level shall be set according to the most recent event, whether it is HPDS set, HPDC set, IRQ SET_CONFIG Packet or HPD Packet.
10.4.4 AUX Request and Response Handling		
10.4.4.1 LTTPR Non-Transparent Mode		
10.4.4.1.1 DP IN Adapter Requirements		
10.4.4.1.1#1	NT	Upon reception of a DisplayPort AUX request, a DP IN Adapter shall send an AUX Packet containing the request over the AUX Path.
10.4.4.1.1#2	NT	The AUX request coming from the DPTX shall not be modified by the DP IN Adapter.
10.4.4.1.1#3	NT	For Target transactions, the DP IN Adapter shall set the AUX_PEND flag as defined in the DisplayPort 1.4a Specification – Section 3.6.5.3.2, and take the appropriate action when the request comes back according to the DisplayPort 1.4a Specification – Section 3.6.5.3.2.
10.4.4.1.1#4	NT	When a DP IN Adapter updates the DP OUT Adapter as the results of a Snoop or Target transaction, it shall perform the update only after receiving an AUX ACK response for all cases beside SET_CONFIG Packet of type SET_VSPE.
10.4.4.1.1#5	NT	The update shall be done by sending SET_CONFIG Packets to the DP OUT Adapter.
10.4.4.1.2 DP OUT Adapter Requirements		
10.4.4.1.2#1	TD 10.005	A DP OUT Adapter shall convert an incoming AUX Packet received from the USB4 Fabric into a DisplayPort AUX request.
10.4.4.1.2#2	TD 10.005	The content of the request shall not be modified by the DP OUT Adapter.
10.4.4.1.2#3	TD 10.005	A DP OUT Adapter shall convert an incoming DisplayPort AUX response into an AUX Packet and send it on the AUX Path.
10.4.4.1.2#4	TD 10.005	The content of the response shall not be changed by the DP OUT Adapter.
10.4.4.2 Non-LTTPR Mode		
10.4.4.2#1	TD 10.004	A DP IN Adapter shall implement AUX Replier.
10.4.4.2#2	TD 10.004	A DP OUT Adapter shall implement AUX Requester.
10.4.4.2.1 AUX Timeout Timers		
10.4.4.2.1#1	TD 10.004	The AUX Response Timeout timer in a DP IN Adapter shall be set to 300µs.

10.4.4.2.1#2	TD 10.004	The AUX Reply Timeout timer in a DP OUT Adapter shall be set to 400µs.
10.4.4.2.2 DP IN Adapter Port Requirements		
10.4.4.2.2#1	TD 10.004	A DP IN Adapter that receives an AUX Request shall classify the AUX Transaction as one of the three following types:1) Internal AUX Transaction – AUX Request which targets only DPCD addresses that are defined as internal in Table 10-8; 2) External AUX Transaction – AUX Request which targets only DPCD addresses that are not defined as internal in Table 10-8; 3) Combined AUX Transaction – AUX Request which targets both Internal and External DPCD addresses. The AUX Response is initially generated by the DPRX and altered by the DP IN Adapter.
10.4.4.2.2#2	TD 10.004	For Internal AUX Transactions, a DP IN Adapter shall not send the AUX Request downstream and shall self-generate the AUX Response.
10.4.4.2.2#3	TD 10.004	For External and Combined AUX Transactions, a DP IN Adapter shall send the AUX Request downstream to the DP OUT Adapter.
10.4.4.2.2#4	TD 10.004	The DP IN Adapter shall generate an AUX DEFER if the Response timer expires while waiting for the AUX Response.
10.4.4.2.2#5	TD 10.004	A DP IN Adapter shall not send an AUX Request to a DP OUT Adapter while the AUX Reply to the preceding AUX Request is outstanding.
10.4.4.2.2#6	TD 10.004	DP IN Adapter shall increment AUX_REQ_CNTR by 1 on every received AUX request from DPTX and shall reset to zero on transition to IDLE state.
10.4.4.2.2#7	TD 10.004	Table 10-10: DP IN Adapter Port AUX Handling State Machine
10.4.4.2.3 DP OUT Adapter Requirements		
10.4.4.2.3#1	TD 10.004	A DP OUT Adapter that receives a DPTX initiated AUX Request while handling a DP OUT Adapter Initiated AUX Transaction, shall send the DPTX initiated AUX Request as soon as it is in Talk Mode.
10.4.4.2.3.1 DPTX Initiated AUX Transactions		
10.4.4.2.3.1#1	TD 10.004	A DP OUT Adapter that receives an AUX Request from a DP IN Adapter shall initiate the AUX Request as soon as it is in Talk Mode.
10.4.4.2.3.1#2	TD 10.004	A DP OUT Adapter that receives an AUX Response shall send the AUX Response over the AUX Path to the DP IN Adapter.
10.4.4.2.3.1#3	TD 10.004	If the AUX Reply Timer expires before an AUX Response is received, a DP OUT Adapter shall send a SET_CONFIG of type SET_AUX_INIT and shall not retry the AUX Request.

10.4.4.2.3.2 DP OUT Adapter Initiated AUX Transactions		
10.4.4.3 LTTPR Transparent Mode		
10.4.4.3#1	NT	A DP IN Adapter shall implement AUX Replier.
10.4.4.3#2	NT	A DP OUT Adapter shall implement AUX Requester.
10.4.4.3.1 AUX Timeout Timers		
10.4.4.3.1#1	NT	The AUX Response Timeout timer in a DP IN Adapter shall not be activated.
10.4.4.3.1#2	NT	The AUX Reply Timeout timer in a DP OUT Adapter shall be set to 3.2ms.
10.4.4.3.2 DP IN Adapter Requirements		
10.4.4.3.2#1	NT	A DP IN Adapter that receives an AUX Request shall classify the AUX Transaction as one of the following types: Internal AUX Transaction – AUX Request which targets only DPCD addresses that are defined as internal in Table 10-9; External AUX Transaction – AUX Request which targets only DPCD addresses that are not defined as internal in Table 10-9; Combined AUX Transaction – AUX Request which targets both Internal and External DPCD addresses. The AUX Response is initially generated by the DPRX and altered by the DP IN Adapter.
10.4.4.3.2#2	NT	For External and Combined AUX Transactions, a DP IN Adapter shall send the AUX Request downstream to the DP OUT Adapter.
10.4.4.3.2#3	NT	A DP IN Adapter shall not: Generate AUX DEFER; Gate any External or Combined AUX Request sent by the DPTX; Gate any AUX Response sent by the DPRX.
10.4.4.3.3 DP OUT Adapter Requirements		
10.4.4.3.3#1	NT	A DP OUT Adapter that receives a DPTX initiated AUX Request while handling a DP OUT Adapter Initiated AUX Transaction, shall send the DPTX initiated AUX Request as soon as it is in Talk Mode.
10.4.4.3.3.1 DP TX Initiated AUX Transactions		
10.4.4.3.3.1#1	NT	A DP OUT Adapter that receives an AUX Request from a DP IN Adapter shall initiate the AUX Request as soon as it is in Talk Mode.
10.4.4.3.3.1#2	NT	A DP OUT Adapter that receives an AUX Response shall send the AUX Response over the AUX Path to the DP IN Adapter.
10.4.4.3.3.1#3	NT	If the AUX Reply Timer expires before an AUX Response is received, a DP OUT Adapter shall send a SET_CONFIG of type SET_AUX_INIT and shall not retry the AUX Request.

10.4.4.3.3.2 DP OUT Adapter Initiated AUX Transactions		
10.4.4.4 AUX Delay Requirements		
10.4.4.4#1	TD 10.004	The DP-to-USB4 Fabric delay shall be measured from the time the last bit arrives at the DP Adapter from the DisplayPort interface to the time when the first bit is sent to the USB4 Fabric.
10.4.4.4#2	TD 10.004	USB4 Fabric-to-DP delay shall be measured from the time when the last bit of the AUX Packet arrives at the DP Adapter to the time when the first bit is sent to the DisplayPort Interface, assuming the DP Adapter is in Talk Mode.
10.4.4.5 Aggregation DisplayPort Capabilities		
10.4.4.5#1	TD 10.003 TD 10.004	A DP IN Adapter shall update its DP_LOCAL_CAP and DP_COMMON_CAP registers if it receives an AUX Read Response that has lower parameter values than the registers currently contain.
10.4.4.5#2	TD 10.003 TD 10.004	Before transmitting the AUX Read Response, the DP IN Adapter shall update the AUX Read Response to reflect the aggregated DisplayPort Capabilities as shown in Table 10-11.
10.4.4.6 DPCD DP Tunneling over USB4		
10.4.4.6#1	NT	When a DP IN Adapter receives an AUX Request targeting the DP Tunneling over USB4 Field DPCDs, it shall respond with its internal data.
10.4.4.6#2	NT	A DP IN Adapter shall set the *DP Tunneling Support* bit to 1b in the DP TUNNELING_CAPABILITIES DPCD (Address E000Dh bit offset 0).
10.4.5 DP Adapters Init Flow		
10.4.5#1	TD 10.007	A DP IN Adapter in the Paired state shall do the following after receiving a first HPD Packet with the *P flag* set to 1b: Update MFDP Mode inner variable according to Section 10.4.5.1.
10.4.5#2	TD 10.007	A DP IN Adapter in the Paired state shall do the following after receiving a first HPD Packet with the *P flag* set to 1b: Send a SET_CONFIG Packet of type SET_AUX_INIT.
10.4.5#3	TD 10.007	The DP IN Adapter shall not drive HPD high on the DisplayPort Interface until after it performs the steps above.
10.4.5.1 Multi-Function DP		
10.4.5.1#1	TD 10.007	If a DP IN Adapter is not connected as part of a Multi-Function (as defined in the DisplayPort Alt Mode Specification), it shall send a SET_CONFIG Packet of type SET_MFDP with the MFDP Enable bit set to 0b.

10.4.5.1#2	TD 10.007	A DP OUT Adapter which receives a SET_CONFIG Packet of type SET_MFDP shall respond with a SET_CONFIG Packet of type SET_MFDP within tDPInit.
10.4.5.1#3	TD 10.007	If the DP OUT Adapter is connected as part of Multi-Function as defined in the DisplayPort 1.4a Specification, then the MFDP Enable bit shall be set to 1b, otherwise it shall be set to 0b.
10.4.6 DP Source Discovery		
10.4.6.1 LTTPR Recognition and Modes Change		
10.4.6.1#1	NT	A DP IN Adapter shall modify the resulting AUX read response as defined in Section 10.4.4.5.
10.4.6.1#2	NT	If DP_COMMON_CAP.*LTTPR Not Supported* is set to 1b, a DP Adapter shall operate only in Non-LTTPR mode.
10.4.6.1#3	NT	A DP IN Adapter shall do the following before transitioning to LTTPR Transparent mode: Complete the AUX Transaction according to the current operation mode; Send a SET CONFIG Packet of type SET_LTTPR_MODE with LTTPR_Mode set to 0b.
10.4.6.1#4	NT	A DP IN Adapter shall do the following before transitioning to LTTPR Non-Transparent mode: Complete the AUX Transaction according to the current operation mode; Send a SET CONFIG Packet of type SET_LTTPR_MODE with LTTPR_Mode set to 1b.
10.4.6.2 DPRX Capabilities Read		
10.4.6.2#1	NT	The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall: 1) Snoop the read response and record the values of the DPCD_REV, MAX_LINK_RATE, MAX_LANE_COUNT, TPS3_SUPPORTED and TPS4_SUPPORTED fields located at DPCD addresses 00000h, 00001h, 00002h and 00003h respectively.
10.4.6.2#2	NT	The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall: 2) Update the Maximal DPCD Rev, Maximal Link Rate, Maximal Lane Count, TPS3 Capability and TPS4 Capability fields in the DP_LOCAL_CAP and DP_COMMON_CAP registers to reflect the lowest common capabilities between the existing values of those registers and the recorded values from step 1.
10.4.6.2#3	NT	The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall: 3) Send a SET_CONFIG Packet of type SET_CMN_DPRX with MSG Data equal to the snooped DPCD_REV which reflects the DPRX DPCD_REV.

10.4.6.2#4	NT	The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall: 4) Set the *DPRX Capabilities Read Done* field in the DP_COMMON_CAP register to 1b. Note that this field is set to 1b regardless of whether or not the values in the *Maximal Link Rate* and *Maximal Lane Count* fields in Step 2 were changed.
10.4.6.3 Sink Count Read		
10.4.6.3#1	TD 10.003	When DPCD addresses 00200h or 02002h are read by the DPTX, a DP IN Adapter shall snoop the read response and record the value of the SINK_COUNT.
10.4.6.3#2	TD 10.003	When the recorded SINK_COUNT value is zero, the DP IN Adapter shall send a SET_CONFIG Packet of type SET_SINK_COUNT, reflecting the recorded value.
10.4.6.3#3	TD 10.003	When a DP OUT Adapter receives a SET_CONFIG Packet of type SET_SINK_COUNT with the SINK_COUNT value equal to zero, the DP OUT Adapter shall: Report an Unplug event as defined in Section 10.3.3.
10.4.6.3#4	TD 10.003 TD 10.004	When a DP OUT Adapter receives a SET_CONFIG Packet of type SET_SINK_COUNT with the SINK_COUNT value equal to zero, the DP OUT Adapter shall: Set the ADP_DP_CS_2.*HPD Status* to 0b in the *DP OUT Adapter Configuration Capability* Field.
10.4.6.3#5	TD 10.003 TD 10.004	While a DP OUT Adapter is Unplugged and has the ADP_DP_CS_2.*HPD Status* set to 0b in the *DP OUT Adapter Configuration Capability* Field, it shall do the following upon IRQ detection: Report a Plug event as defined in Section 10.3.3.
10.4.6.3#6	TD 10.003 TD 10.004	While a DP OUT Adapter is Unplugged and has the ADP_DP_CS_2.*HPD Status* set to 0b in the *DP OUT Adapter Configuration Capability* Field, it shall do the following upon IRQ detection: Set the ADP_DP_CS_2.*HPD Status* to 1b in the *DP OUT Adapter Configuration Capability* Field.
10.4.7 Down-Spread Control		
10.4.7#1	NT	When DPCD address 00107h is written by a DPTX, a DP IN Adapter, operating in Non-LTTPR or LTTPR Transparent Modes, shall respond with AUX ACK and shall send a SET_CONFIG Packet of type SET_DOWNSPREAD.
10.4.7#2	NT	The *MSG Data* field in the SET_CONFIG Packet shall be equal to the value written by the DPTX.
10.4.7#3	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of type SET_DOWNSPREAD shall initiate an AUX write request to DPCD address 00107h with the value received in the MSG Data of the SET_CONFIG Packet.

10.4.8 Stream Mode Set		
10.4.8#1	NT	If the DPTX writes to DPCD address 00111h, a DP IN Adapter shall snoop the write request and record the value of the MST_EN bit.
10.4.8#2	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_STREAM_MODE, reflecting the recorded value of the MST_EN bit when a new recorded MST_EN value is different than the previous value
10.4.8#3	NT	The MST_EN default value at the DP Adapters shall be as defined in the DisplayPort 1.4a Specification.
10.4.8#4	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of type SET_STREAM_MODE shall respond with a SET_CONFIG Packet of type SET_STREAM_MODE, to signify the acknowledgment of the mode change.
10.4.8#5	NT	The value of the *MSG Data* field in the return packet has no meaning and shall be ignored by the DP IN Adapter.
10.4.9 DSC and FEC Enable		
10.4.9#1	NT	If the DPTX writes to DPCD address 00120h, a DP IN Adapter shall snoop the write request and record the values of the *FEC_READY*, *FEC_ERROR_COUNT_SEL* and *LANE_SELECT* fields.
10.4.9#2	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_FEC_READY, reflecting the recorded value of the FEC_READY bit when a new recorded FEC_READY value is different than the previous value.
10.4.9#	NT	The FEC_READY default value at the DP Adapters shall be as defined in the DisplayPort 1.4a Specification.
10.4.9#	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of type SET_FEC_READY shall respond with a SET_CONFIG Packet of type SET_FEC_READY within tDPInit, to signify the acknowledgment of the mode change.
10.4.9#	NT	The value of the *MSG Data* field in the return packet has no meaning and shall be ignored by the DP IN Adapter.

10.4.10 DP Link Training		
10.4.10.1 LTTPR		
10.4.10.1#1	NT	The DP IN and DP OUT Adapters shall follow the LTTPR Non-Transparent link training as defined in the DisplayPort 1.4a Specification while noting the following points: DP IN as UFP and DFP – As described in Section 10.4.4, the DP IN Adapter serves as UFP and DFP for AUX handling, therefore it updates the DP OUT Adapter with the different stages of the LTTPR Non-Transparent link training through SET_CONFIG Packets; Training Patterns – Training Patterns are not carried over the USB4 Fabric.
10.4.10.1.1 DP IN Adapter Requirements		
10.4.10.1.1#1	NT	After DP Link training is finished on the UFP, a DP IN Adapter shall maintain symbol lock and lane alignment in its receiver while DPTX trains the rest of downstream DP Links
10.4.10.1.1#2	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_LINK after DPTX writes TPS1 to the DP IN Adapter TRAINING_PATTERN_SET_PHY_REPEATERx DPCD register.
10.4.10.1.1#3	NT	The SET_CONFIG packet shall have the following values: LC = LANE_COUNT_SET value written by DPTX; LR = LINK_BW_SET value written by the DPTX; MSG Data = 1b, representing DP Link Training Mode = LTTPR Non-Transparent.
10.4.10.1.1#4	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_TRAINING with TS = 0xFF after DPTX writes 0x0 to the DP IN Adapter TRAINING_PATTERN_SET_PHY_REPEATERx DPCD register.
10.4.10.1.1#5	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_TRAINING with TS = 0x0 after DPTX writes 0x0 to the DPRX TRAINING_PATTERN_SET DPCD register.
10.4.10.1.1#6	NT	After DP Link training is finished on the UFP, a DP IN Adapter shall detect a Training pattern on its receiver.
10.4.10.1.1#7	NT	After detecting the Training pattern, the DP IN Adapter shall send a single corresponding SET_CONFIG Packet of type SET_TRAINING for every change in Training pattern.
10.4.10.1.1#8	NT	The *TS* field shall be equal to the detected Training pattern as defined in Table 10-5.
10.4.10.1.1#9	NT	A DP IN Adapter shall send SET_CONFIG Packet of Type SET_VSPE when DPTX writes the TRAINING_LANE0_SET or TRAINING_LANE0_SET_PHY_REPEATERx DPCD register of the next downstream receiver.
10.4.10.1.1#10	NT	The *MSG Data* field shall carry the value in the write request.

10.4.10.1.1#11	NT	The SET_VSPE SET_CONFIG Packet shall be sent by the DP IN Adapter before sending the AUX Request Packet.
10.4.10.1.1#12	NT	A DP Adapter shall have higher priority generating and parsing SET_CONFIG packets over AUX Transaction.
10.4.10.1.1#13	NT	A DP IN Adapter shall respond to a DPTX that link training has ended successfully only when all the following are true: The DP IN Adapter internal status indicates link training has ended successfully; The DP IN Adapter sent at least nine DP Clock Sync Packets after it sent the SET_CONFIG Packet of type SET_LINK.
10.4.10.1.2 DP OUT Adapter Requirements		
10.4.10.1.2#1	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of Type SET_LINK with the DP Link Training Mode bit set to 1b shall start its internal Symbol clock PLL according to the *Link Rate* field, and start the Lifetime Counter as defined in Section 10.6.1.2.
10.4.10.1.2#2	NT	Deprecated.
10.4.10.1.2#3	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of Type SET_TRAINING with *TS* field equal to 0 shall transmit IDLE pattern according to the DisplayPort 1.4a Specification.
10.4.10.1.2#4	NT	A DP OUT Adapter shall set its Voltage Swing (VS) and Pre-Emphasis (PE) levels for all enabled lanes upon receiving a SET_CONFIG Packet of type SET_VSPE. The VS and PE levels shall be according to the MSG Data. The DP OUT Adapter shall transition on the 10-bit symbol boundary when: Transitioning from one training pattern to another training pattern; Transitioning to IDLE sequence after DP Link training is done.
10.4.10.1.3 DP Link Training Example		
10.4.10.1.3.1 LTTPR - CR_DONE Phase		
10.4.10.1.3.2 LTTPR - EQ Phase		
10.4.10.1.3.3 DPRX - CR_DONE Phase		
10.4.10.1.3.4 DPRX - EQ Phase		
10.4.10.2 Non-LTTPR and LTTPR Transparent		
10.4.10.2#1	NT	A DP Adapter shall perform DisplayPort link training according to the DisplayPort 1.4a Specification with the modifications and requirements defined in Section 10.4.10.2.1 and Section 10.4.10.2.2

10.4.10.2.1 DP IN Adapter Requirements		
10.4.10.2.1#1	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_LINK after DPTX writes TPS1 to the DP RX TRAINING_PATTERN_SET DPCD register.
10.4.10.2.1#2	NT	The SET_CONFIG packet shall have the following values: LC = LANE_COUNT_SET value written by DPTX; LR = LINK_BW_SET value written by the DPTX; TPS = Reflects TPS3 and TPS4 support as indicated in the DP_COMMON_CAP register; MSG Data = 0b, representing DP Link Training Mode = Non-LTTPR and LTTPR Transparent modes.
10.4.10.2.1#3	NT	A DP IN Adapter shall respond to a status read of LANEx_CR_DONE as follows: If a SET_CONFIG Packet of type STATUS_CR_DONE was not received since link training started, set the LANEx_CR_DONE bits to 0b.
10.4.10.2.1#4	NT	A DP IN Adapter shall respond to a status read of LANEx_CR_DONE as follows: If a SET_CONFIG Packet of type STATUS_CR_DONE was received since link training started, set the LANEx_CR_DONE bits to be the internal DP IN Adapter status for a lane ANDed with the relevant bit present in the last received SET_CONFIG MSG Data.
10.4.10.2.1#5	NT	A DP IN Adapter shall respond to a DPTX that link training has ended successfully only when all the following are true: The DP IN Adapter internal status indicates link training has ended successfully; The DP IN Adapter received a SET_CONFIG Packet of type SET_LINK, carrying the same *LC* and *LR* fields that it sent to the DP OUT Adapter when link training was initiated; The DP IN Adapter sent at least nine DP Clock Sync Packets after it received a SET_CONFIG Packet of type STATUS_CR_DONE.
10.4.10.2.1#6	NT	While the conditions (as defined in this section) for successful link training are not met, a DP IN Adapter shall respond to a status read of INTERLANE_ALIGN_DONE, LANEx_CHANNEL_EQ_DONE and LANEx_SYMBOL_LOCKED as follows: If a SET_CONFIG Packet of type STATUS_TRAINING_FAIL was received since link training started, set the following bits: INTERLANE_ALIGN_DONE shall be set to 0b. LANEx_CHANNEL_EQ_DONE is equal to the DP IN internal status ANDed with LANEx_CHANNEL_EQ_DONE that was received as MSG Data by the STATUS_TRAINING_FAIL. LANEx_SYMBOL_LOCKED is equal to the DP IN internal status ANDed with LANEx_SYMBOL_LOCKED that was received as MSG Data by the STATUS_TRAINING_FAIL.
10.4.10.2.1#7	NT	Else, a DP IN Adapter shall use one or more of the methods below to indicate to DPTX that link training has not completed successfully yet: Set INTERLANE_ALIGN_DONE to 0b; Set LANEx_CHANNEL_EQ_DONE to 0b for any of the active lanes; Set LANEx_SYMBOL_LOCKED to 0b for any of the active lanes.

10.4.10.2.2 DP OUT Adapter Requirement		
10.4.10.2.2#1	NT	A DP OUT Adapter receiving a SET_CONFIG Packet of type SET_LINK, with *LC* field other than 0h shall: Initiate link training with the target Link Rate and Lane Count received from the SET_LINK Packet.
10.4.10.2.2#2	NT	A DP OUT Adapter receiving a SET_CONFIG Packet of type SET_LINK, with *LC* field other than 0h shall: Link training proceeds according to the DisplayPort 1.4a spec except that a DP OUT Adapter that concludes that it needs to either reduce the Link Rate or Lane Count shall treat it as link training failure and shall not reduce the Link Rate or Lane Count.
10.4.10.2.2#3	NT	A DP OUT Adapter which finishes the Clock Recovery Sequence (as defined in the DisplayPort 1.4a Specification) shall send a SET_CONFIG Packet of type STATUS_CR_DONE, reflecting the LANEx_CR_DONE statuses of the active lanes.
10.4.10.2.2#4	NT	The *Phase* field shall be set to 0b.
10.4.10.2.2#5	NT	A DP OUT Adapter in EQ phase which detects that the DP receiver has lost Clock Recovery on one or more of the active lanes shall conclude that link training has failed and shall send a SET_CONFIG Packet of type STATUS_CR_DONE, reflecting the new LANEx_CR_DONE statuses of the active lanes.
10.4.10.2.2#6	NT	The *Phase* field shall be set to 1b.
10.4.10.2.2#7	NT	If link training fails for a reason other than lost Clock Recovery, a DP OUT Adapter shall send a SET_CONFIG Packet of type STATUS_TRAINING_FAIL.
10.4.10.2.2#8	NT	If link training finishes successfully, a DP OUT Adapter shall send a SET_CONFIG Packet of type SET_LINK, with the same *LC* and *LR* fields it received from the DP IN Adapter when link training was initiated.
10.4.10.2.2#9	NT	Deprecated.
10.4.10.2.2#10	NT	The MSG Data shall be set as follows: LANEx_CHANNEL_EQ_DONE is equal to the value of the last read from LANEx_CHANNEL_EQ_DONE field in DPRX. LANEx_SYMBOL_LOCKED is equal to the value of the last read from LANEx_SYMBOL_LOCKED field in DPRX.
10.4.10.3 Transition to High Speed Tunnel		
10.4.10.3#1	NT	A DP IN Adapter shall start converting DisplayPort Main-Link Symbols into Tunneled Packets and sending those Packets over the Main-Link Path when all of the following are true: Link Training has completed successfully; The DP IN Adapter received an SR.

10.4.11 Power States Set		
10.4.11#1	NT	When DPTX writes to DPCD address 00600h, a DP IN Adapter shall snoop the write request and record the value of the *SET_POWER_STATE* field.
10.4.11#2	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_POWER, reflecting the recorded value in the following cases: A first DPCD write of address 00600h after an HPD Plug event.
10.4.11#3	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_POWER, reflecting the recorded value in the following cases: The new recorded SET_POWER_STATE is different than the previous value.
10.4.12 DP Main-Link Disable		
10.4.12#1	NT	DP OUT Adapter which receives a Main-Link disable message shall disable its transmitters.
10.4.13 Link-Init		
10.4.13#1	NT	Upon Link-Init activation, a DP IN Adapter shall turn off its DisplayPort receivers and stop any transmission of Tunneled Packets over the Main-Link Path until the end of the next successful Link training, as defined in Section 10.4.10.3.
10.4.13#2	NT	Upon Link-Init activation, a DP OUT Adapter shall turn off its DisplayPort transmitters.
10.4.14 DP PHY Testability		
10.4.14.1 DP IN Adapter PHY Layer Testing		
10.4.14.1#1	NT	The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Before entering DP IN PHY Test Mode: Connect a Router with a DP OUT Adapter and a DPRX. Both the DP OUT Adapter and the DPRX need to support the Link Rate and Lane Count required by the test; Verify that a DP Link is established.
10.4.14.1#2	NT	The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Entering DP IN PHY Test Mode: The DP IN Adapter shall enter DP IN PHY Test Mode when the DPTX writes a non-zero value to LINK_QUAL_LANEx_SET in the DPCD registers.
10.4.14.1#3	NT	The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: While in DP IN PHY Test Mode: The DP IN Adapter shall keep the Hot Plug Detect signal high; The DP IN Adapter shall respond to all AUX transactions related to the PHY layer testing.

10.4.14.1#4	NT	The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Exiting DP IN PHY Test Mode: The DP IN Adapter shall exit DP IN PHY Test Mode when the DPTX initiates DP Link Training.
10.4.14.2 DP OUT Adapter PHY Layer Testing		
10.4.14.2#1	NT	The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Before entering DP OUT PHY Test Mode: Connect a Router with a DP IN Adapter and a DPTX. Both the DP IN Adapter and the DPTX need to support the test required Link Rate and Lane Count; Verify that a DP Link is established.
10.4.14.2#2	NT	The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Entering DP OUT PHY Test Mode: When the DPTX reads the following sequence, the DP IN Adapter shall send a SET_CONFIG Packet of Type SET_PHY_TEST_MODE and enter DP OUT PHY Test Mode: AUTOMATED_TEST_REQUEST is set to 1b (DPCD 00201h or 02003h bit 1); PHY_TEST_PATTERN is set to 1b (DPCD 00218h bit 3).The DP OUT Adapter shall enter DP OUT PHY Test Mode when it receives a SET_CONFIG Packet of type SET_PHY_TEST_MODE.
10.4.14.2#3	NT	The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: While in DP OUT PHY Test Mode: The DP OUT Adapter shall act as the DPTX under test; The DP OUT Adapter shall send HPD Packet with Plug Flag set to 0b; The DP IN Adapter shall not forward any AUX Transactions to the DP OUT Adapter.
10.4.14.2#4	NT	The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Exiting DP OUT PHY Test Mode: Upon a DPRX HPD signal de-assertion: The DP OUT Adapter shall exit DP OUT PHY Test Mode; The Connection Manager tears down the DP Paths, causing both of the DP Adapters to enter the Present State.
10.5 High Speed Tunneling		
10.5.1 SST Tunneling		
10.5.1.1 Video Data Packet		
10.5.1.1.1 Transfer Unit Set		
10.5.1.1.1#1	NT	A DP IN Adapter shall pack the active pixel data of a TU into either one or two TU Sets.
10.5.1.1.1#2	NT	When EOC control link symbols are present in a TU, a DP IN Adapter shall pack the EOC symbols using the same scheme as for active pixel symbols.

10.5.1.1.1#	NT	The EOC symbols shall be packed in their 8-bit value representation (DCh).
10.5.1.1.1#	NT	Each TU Set shall be prepended with a TU Set Header.
10.5.1.1.1#	NT	The header in Figure 10-26(A) shall be used for a TU Set that contains a TU with no EOC Symbol.
10.5.1.1.1#	NT	The header in Figure 10-26(B) shall be used for a TU Set that contains a TU with an EOC symbol.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the TU Set Header.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: **Video Count [13:8]**: This field shall contain the number of active video symbols per lane. A value of zero represents 64. The total number of active video symbols in the TU Set is equal to (Video Count * Number of Lanes).
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: **(No EOC) Fill Count [27:14]**: This field shall have the value as defined in 10.5.1.5.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: **(EOC) Fill Count [21:14]**: This field shall have the value as defined in 10.5.1.5.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: **(EOC) EOC Index [27:22]**: This field shall contain the index of the EOC symbol inside the TU Set. Symbols within a TU Set are indexed starting with zero (for the first symbol) and ending with (Video Count – 1) for the last symbol.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: **L [Bit 28]**: Last TU Flag. This flag shall be set to 1b if the TU is the last TU Set of a line. Otherwise shall be set to 0b.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: **RSV [30:29]**: Reserved.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: **RSV [30:29]**: Reserved.
10.5.1.1.2 Packet Format		
10.5.1.1.2#1	NT	A Video Data Packet shall have the format shown in Figure 10-28.
10.5.1.1.2#2	NT	All TU Set headers within the Video Data Packet payload shall be aligned to 32-bits by adding padding bytes at the end of the TU set payload if necessary.

10.5.1.1.2#3	NT	A DP IN Adapter shall follow the rules below when constructing a Video Data Packet: A Video Data Packet shall contain at least 1 TU Set and no more than 16 TU Sets. If a TU cannot fit within a single Video Data Packet, it shall be split into two TU sets.
10.5.1.1.2#4	NT	A DP IN Adapter shall follow the rules below when constructing a Video Data Packet: When a TU is split into two TU Sets, the remainder of the active pixel symbols shall be sent in the first TU Set in the next Video Data Packet. The *Fill Count* field in the TU Set Header of the second Video Data Packet for a TU that is split into multiple Video Data Packets shall be set to 0.
10.5.1.1.2#5	NT	A DP IN Adapter shall follow the rules below when constructing a Video Data Packet: The length of all TU Set Padding is included when calculating the *Length* field in the Tunneled Packet header.
10.5.1.2 Main Stream Attribute Packet		
10.5.1.2#1	NT	A Main Stream Attribute Packet shall consist of an MSA header followed by packet payload.
10.5.1.2#2	NT	The packet payload shall contain the encoding of the 36-byte attribute information following the <SS, SS> control symbol pair.
10.5.1.2#3	NT	The fields forming an MSA Header shall be as defined below: **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the MSA Header.
10.5.1.2#	NT	The fields forming an MSA Header shall be as defined below: **Fill Count [24:8]**: This field shall contain the fill count as defined in Section 10.5.1.5.
10.5.1.2#	NT	The fields forming an MSA Header shall be as defined below: **Reserved [31:25]**: Reserved.
10.5.1.2#	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Verify the *ECC* field in the MSA header. If an uncorrectable error has occurred, the Main Stream Attribute Packet shall be dropped and ignored.
10.5.1.2#	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Send Fill Count number of Stuffing Symbols on all lanes of the DP Main-Link according to Section 10.5.1.5.
10.5.1.2#	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Send the control symbol pair <SS, SS> on all lanes of the DP Main-Link.
10.5.1.2#	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Send the stream attribute information contained in the first 36 bytes of the payload of the Main Stream Attribute Packet by steering bytes from the payload onto the lanes of the DP Main-Link in a round robin fashion starting with lane 0.

10.5.1.2#	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Send the control symbol <SE> on all lanes of the DP Main-Link.
10.5.1.3 Blank Start Packet		
10.5.1.3#1	NT	A Blank Start Packet shall consist of a Blank Start header followed by packet payload.
10.5.1.3#2	NT	The packet payload shall contain the encoding of all 4 sets of <VB-ID, Mvid 7:0, Maud 7:0>.
10.5.1.3#3	NT	The fields forming the Blank Start header shall be as defined below: **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the Blank Start Header.
10.5.1.3#4	NT	The fields forming the Blank Start header shall be as defined below: **Fill Count [24:8]**: This field shall have the value as defined in Section 10.5.1.5.
10.5.1.3#5	NT	The fields forming the Blank Start header shall be as defined below: **Reserved [29:25]**: Reserved.
10.5.1.3#6	NT	The fields forming the Blank Start header shall be as defined below: **CP [30]**: Content Protection Flag shall be set to 1b if Blank Start DP Control Link Symbols sequence were <BS,CP,CP,BS> or <SR,CP,CP,SR>.
10.5.1.3#7	NT	The fields forming the Blank Start header shall be as defined below: **SR [31]**: Scrambler Reset Flag shall be set to 1b if Blank Start DP Control Link Symbols sequence were <SR,BF,BF,SR> or <SR,CP,CP,SR>.
10.5.1.3#8	NT	Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations: 1) Verify the *ECC* field at the Blank Start Header. If an uncorrectable error has occurred, the Blank Start Packet shall be dropped.
10.5.1.3#9	NT	Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations: 2) Generate Stuffing Symbols on each lane of the DP Main-Link according to the *Fill Count* field in the Blank Start Header and Section 10.5.1.5.
10.5.1.3#10	NT	Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations: 3) Generate control symbols on each lane of the DP Main-Link marking the start of the blanking period based on the *SR Flag* and *CP Flag* as shown in Table 10-12.
10.5.1.3#11	NT	Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations: 4) Steer the three double-words of Blank Start Packet payload starting with the second double-word onto the Main-Link by interleaving a byte at a time onto the lanes of the DP Main-Link starting with lane 0.

10.5.1.4 Secondary Data Packet		
10.5.1.4.1 Secondary Transfer Unit		
10.5.1.4.1#1	NT	A DP IN Adapter shall pack secondary data into one or more Secondary Tus.
10.5.1.4.1#	NT	Each Secondary TU shall be prepended with a Secondary TU Header.
10.5.1.4.1#	NT	The fields forming the Secondary TU Header shall be as defined below: **ECC [7:0]**: Error correction field that is calculated over bits [31:8] of the Secondary TU Header.
10.5.1.4.1#5	NT	The fields forming the Secondary TU Header shall be as defined below: **Secondary Count [13:8]**: This field shall contain the number of secondary data symbols per lane. A value of zero represent 64 if ND bit equals 0. The total number of secondary data symbols in the Secondary TU is equal to (Secondary Count * Number of Lanes).
10.5.1.4.1#6	NT	The fields forming the Secondary TU Header shall be as defined below: **Fill Count [27:14]**: This field shall have the value as defined in Section 10.5.1.5. When both the *NSS* and *NSE* fields are 0b, the *Fill Count* field is extended by one bit and is constructed as {EFC, Fill Count} where EFC is the most significant bit.
10.5.1.4.1#7	NT	The fields forming the Secondary TU Header shall be as defined below: **L [Bit 28]**: Last TU Flag. This flag shall be set to 1b if the Secondary TU is either the last TU before a split or the TU represents the Secondary End Symbol. Otherwise it shall be set to 0b.
10.5.1.4.1#8	NT	The fields forming the Secondary TU Header shall be as defined below: **NSE [Bit 29]**: No Secondary End. This bit shall be set to 1b if Last TU Flag is set to 1b and a Secondary End Control symbol is not present at the DP Main-link. Otherwise it shall be set to 0b.
10.5.1.4.1#9	NT	The fields forming the Secondary TU Header shall be as defined below: **NSS [Bit 30]**: No Secondary Start. This bit shall be set to 1b if this is the first Secondary TU after a non-Secondary Tunneled Packet and a Secondary Start Control symbol is not present at the DP Main-Link. Otherwise it shall be set to 0b.
10.5.1.4.1#10	NT	The fields forming the Secondary TU Header shall be as defined below: **EFC/ND [31]**: Extended Fill Count/No Data. This bit shall be set to 1b if the Secondary TU does not have any Secondary data.
10.5.1.4.1#11	NT	The fields forming the Secondary TU Header shall be as defined below: **EFC**: When both the NSS and NSE fields are 0b, this bit is used as an extension to the Fill Count field.

10.5.1.4.1#12	NT	The fields forming the Secondary TU Header shall be as defined below: **ND**: When either the *NSS* or *NSE* fields are 1b, this bit is used to indicate whether or not the Secondary TU has any Secondary data. This bit shall be set to 1b if the Secondary TU does not contain Secondary data. If the Secondary TU contains Secondary data, this bit shall be set to 0b.
10.5.1.4.1#13	NT	A DP IN Adapter shall start packing secondary data into a Secondary TU in the following cases: A single Secondary Start Control symbol <SS> is present on the DP Main-link.
10.5.1.4.1#14	NT	A DP IN Adapter shall start packing secondary data into a Secondary TU in the following cases: The previous Secondary TU has reached the maximum capacity and the secondary data continues.
10.5.1.4.1#15	NT	A DP IN Adapter shall start packing secondary data into a Secondary TU in the following cases: The secondary data is split (as defined by the DisplayPort 1.4a Specification) by a non-Secondary Data Packet and this packet has now ended.
10.5.1.4.1#16	NT	A DP IN Adapter shall stop packing secondary data into a Secondary TU upon one of the following cases: Secondary End Control symbol <SE> is present on the DP Main-link.
10.5.1.4.1#17	NT	A DP IN Adapter shall stop packing secondary data into a Secondary TU upon one of the following cases: Maximum capacity is reached: For 1-Lane and 2-Lanes links: maximum capacity is reached when the *Secondary Count* field is 64; For 4-Lane links: maximum capacity is reached when the *Secondary Count* field is 62.
10.5.1.4.1#18	NT	A DP IN Adapter shall stop packing secondary data into a Secondary TU upon one of the following cases: Secondary data stream was split by MSA, BS or Active video as defined in the DisplayPort 1.4a Specification.
10.5.1.4.1#19	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 1) Verify the *ECC* field in the Secondary TU Header. If an uncorrectable error has occurred, the whole Secondary TU and the subsequent TUs within that packet shall be dropped and ignored.
10.5.1.4.1#20	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 2) Send Fill Count number of Stuffing Symbols on all lanes of the DP Main-Link according to Section 10.5.1.5.
10.5.1.4.1#21	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 3) If this Secondary TU is the first Secondary TU to follow a non-Secondary Data Packet and the NSS bit is not set in the Secondary TU Header, send the control symbol <SS> on all lanes of the DP Main-Link.

10.5.1.4.1#22	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 4) Send the secondary data contained in the Secondary TU. The number of cycles of data shall be as according to the *Secondary Count* field in the Secondary TU Header. The secondary data shall be sent on the DP Main-Link by steering bytes from the payload onto the lanes in a round robin fashion starting with lane 0.
10.5.1.4.1#23	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 5) If the *L Flag* is set and the *NSE* bit is not set in the Secondary TU header, send the control symbol <SE> on all lanes of the DP Main-Link.
10.5.1.4.2 Packet Format		
10.5.1.4.2#1	NT	A Tunneled Secondary Data Packet shall have the format shown in Figure 10-34.
10.5.1.4.2#2	NT	A Tunneled Secondary Data Packet shall not include Secondary TUs from more than one DisplayPort SDP.
10.5.1.4.2#3	NT	All Secondary TU Headers within the Tunneled Secondary Data Packet payload shall be aligned to 32-bits by adding Secondary TU Padding bytes at the end of the Secondary TU payload if necessary.
10.5.1.4.3 Secondary Data to Secondary TU Mapping Examples		
10.5.1.5 Fill Count		
10.5.1.5#1	NT	DP IN Adapter shall calculate the *Fill Count* field according to the following formula: *Fill Count* field = Act_Fill_Count + DP_K_Prev_Pkt – Prev_Factor
10.5.1.5#2	NT	The following cycles shall be counted as the Act_Fill_Count: Stuffing Symbols; BE - Blanking End; FS - Filling Start; FE - Filling End.
10.5.1.5#3	NT	A DP OUT Adapter shall use the following formula to calculate the actual number of Stuffing Symbols to be driven over the DP link: Act_Fill_Count = *Fill Count* field + Prev_Factor – DP_K_Prev_Pkt
10.5.1.5#4	NT	A DP OUT Adapter shall ignore the *Fill Count* field in the first Tunneled Packet sent on the Main-Link Path after DP link training.
10.5.2 MST Tunneling		
10.5.2.1 Sub-MTP TU		
10.5.2.1#1	NT	A Sub-MTP TU Header shall have the format shown in Figure 10-38.
10.5.2.1#2	NT	The fields forming the Sub-MTP TU Header shall be as defined below: **ECC [7:0]**: Error correction field that is calculated over bits [23:8] of the Sub-MTP TU Header.

10.5.2.1#3	NT	The fields forming the Sub-MTP TU Header shall be as defined below: **Data Count[13:8]**: This field shall contain the number of Data symbols per lane. The total number of Data symbols in the Sub-MTP TU is equal to (*Data Count* * Number of Lanes).
10.5.2.1#4	NT	The fields forming the Sub-MTP TU Header shall be as defined below: **Type[17:14]**: This field shall contain the Type encoding of the Sub-MTP TU.
10.5.2.1#5	NT	The fields forming the Sub-MTP TU Header shall be as defined below: **Slot Number[23:18]**: This field shall contain the first slot number in the MTP which this Sub-MTP TU Header is describing.
10.5.2.1#6	NT	A DP IN Adapter that receives an MST stream shall perform the DisplayPort PHY layer and De-scrambler functions defined in the DisplayPort 1.4a Specification.
10.5.2.1#7	NT	Upon reception of the first SR after link training completion, a DP IN Adapter shall: Track the total number of allocated MST slots by snooping any DPCD AUX transactions that configure the VC Payload ID Table.
10.5.2.1#8	NT	Upon reception of the first SR after link training completion, a DP IN Adapter shall: Start mapping MTP from the DP Main-Link into Sub-MTP TUs.
10.5.2.1#9	NT	When a Parameter includes a Data byte, the DP IN Adapter shall append the de-scrambled Data byte as the Parameter.
10.5.2.1#10	NT	A DP IN Adapter shall pack the Data bytes by selecting a byte from each Lane of the Main-Link in a cyclic way, starting with lane 0.
10.5.2.1#11	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: A Sub-MTP TU is byte-aligned.
10.5.2.1#12	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: The total length of a Sub-MTP TU (Header + Parameter Bytes + Data Bytes) does not exceed 252 Bytes.
10.5.2.1#13	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: Slot 0 always starts a new Sub-MTP TU.
10.5.2.1#14	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: A Sub-MTP TU includes data from one MTP only.
10.5.2.1#15	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: A DP IN Adapter shall map an MTP into the minimum possible number of Sub-MTP TU.
10.5.2.1#16	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: A Sub-MTP TU shall be split into 2 Sub-MTP TUs if it does not fit into an MTP packet according to Section 10.5.2.3.

10.5.2.2 MTP to Sub-MTP TU Examples		
10.5.2.2.2 Shifting SR		
10.5.2.2.2#1	NT	Upon detecting a sequence of four consecutive SR with 216 time-slot intervals, a DP IN Adapter shall switch to the new SR location.
10.5.2.2.2#2	NT	The first three SR that are not at Slot Zero's original location shall be mapped to a non-zero Slot Type 8 (1 K-Symbol), for the case of 1-lane, carrying Parameter byte = 8 (as defined in Table 10-17).
10.5.2.2.2#3	NT	The fourth SR shall be mapped to a non-zero Slot Type 1 (Shifting SR) forcing the next slot to be slot number 1.
10.5.2.2.2#4	NT	For the case of 2-Lane DP links, the first three SR shall be mapped to Type 9 (2 K-Symbols).
10.5.2.2.2#5	NT	For the case of and 4-Lane DP links, the first three SR shall be mapped to Type 11 (4 K-Symbols).
10.5.2.2.3 ACT		
10.5.2.2.4 SF and VCPF		
10.5.2.2.4#1	NT	A DP IN Adapter shall not map a SF sequence into a Sub-MTP TU unless the SF sequence comes immediately after a VCPF sequence.
10.5.2.3 MST Packet Format		
10.5.2.3#1	NT	An MST Packet shall have the format shown in Figure 10-46.
10.5.2.3#2	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: The first 3 bytes of the MST Packet payload contains the first Sub-MTP TU Header.
10.5.2.3#3	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: When concatenating two Sub-MTP TUs, the first TU is not be padded.
10.5.2.3#4	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: The maximum number of MTPs packed into one MST Packet does not exceed 17.
10.5.2.3#5	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: The *Length* field in the Tunneled Packet Header does not include padding bytes.
10.5.2.3#6	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: The Payload of the Tunneled Packet shall be between 230 and 252 Bytes (inclusive), unless the Payload contains at least 16 MTPs.

10.5.2.4 MST Packets to DP MTP		
10.5.2.4#1	NT	A DP OUT Adapter shall analyze each Sub-MTP TU Header and recreate the MTP K-Code and data bytes according to Table 10-16 (for slot zero) or Table 10-17 (for non-zero slots).
10.5.2.4#2	NT	If a DP OUT Adapter has a slot for which it lacks sufficient information to recreate the MTP K-Code and/or data bytes, it shall follow the rules below: If the last Sub-MTP TU Header was VCPF, insert VCPF.
10.5.2.4#3	NT	If a DP OUT Adapter has a slot for which it lacks sufficient information to recreate the MTP K-Code and/or data bytes, it shall follow the rules below: If the last Sub-MTP TU Header was Unallocated, insert unallocated (data bytes equal zero).
10.5.2.4#4	NT	If a DP OUT Adapter has a slot for which it lacks sufficient information to recreate the MTP K-Code and/or data bytes, it shall follow the rules below: For all other cases, insert SF.
10.5.2.4#5	NT	After creating the MTPs, the DP OUT Adapter shall follow all the PHY Layer functions required functions by the DisplayPort 1.4a Specification.
10.5.3 FEC		
10.5.3.1 SR Count		
10.5.3.1#1	NT	A DP Adapter shall implement the SR Count counter, which counts the number of cycles that have elapsed since the last SR.
10.5.3.1#2	NT	A DP IN Adapter shall initiate the SR Count at the first cycle after receiving an SR.
10.5.3.1#3	NT	A DP OUT Adapter shall initiate the SR Count at the first cycle after transmitting an SR.
10.5.3.2 DP IN Adapter Requirements		
10.5.3.2#1	NT	A DP IN Adapter shall: Implement FEC Decoding as defined in the DisplayPort 1.4a Specification.
10.5.3.2#2	NT	A DP IN Adapter shall: Construct an FEC_DECODE Packet as defined in Section 10.5.3.4 upon FEC_DECODE_EN or FEC_DECODE_DIS sequence detection.
10.5.3.2#3	NT	A DP IN Adapter shall: The Adapter Layer shall prioritize the FEC_DECODE Packet over all other Main-Link Path packets when pass it to the Transport Layer.
10.5.3.2#4	NT	A DP IN Adapter shall not: Tunnel any FEC-related symbols including FEC_PARITY_MARKER, FEC_DECODE & FEC_PARITY_PH.

10.5.3.2#5	NT	A DP IN Adapter shall not: Count the Link cycles of FEC Symbols for fill count purposes.
10.5.3.3 DP OUT Adapter Requirements		
10.5.3.3#1	NT	A DP OUT Adapter shall: Implement FEC Encoding as defined in the DisplayPort 1.4a Specification.
10.5.3.3#2	NT	A DP OUT Adapter shall: Apply majority voting for the repeated fields with in the FEC_DECODE Packet: SR Count; FEN; FDS.
10.5.3.3#3	NT	A DP OUT Adapter shall: Generate FEC_DECODE_EN and FEC_DECODE_DIS upon reception of a FEC_DECODE Packet.
10.5.3.3#4	NT	FEC_DECODE_EN sequence shall be generated if *FEN* field in the FEC_DECODE Packet is 1b.
10.5.3.3#5	NT	FEC_DECODE_DIS sequence shall be generated if *FDS* fields in the FEC_DECODE Packet is 1b.
10.5.3.3#6	NT	The first symbol of the FEC_DECODE_EN and FEC_DECODE_DIS sequences shall be transmitted according to the *SR Count* field of the FEC_DECODE Packet, i.e. the FEC_DECODE_EN and FEC_DECODE_DIS sequence shall be transmitted *SR Count* link clock cycles after the most recently transmitted SR.
10.5.3.3#7	NT	When a FEC_DECODE Packet is received, a DP OUT Adapter compares the Packet SR Count and the Counter SR Count as follows: If Packet SR Count > Counter SR Count the DP OUT Adapter waits for the Counter SR Count to be equal to Packet SR Count then generate the FEC sequence.
10.5.3.3#8	NT	When a FEC_DECODE Packet is received, a DP OUT Adapter compares the Packet SR Count and the Counter SR Count as follows: Else, a DP OUT Adapter waits for next SR to be transmitted, then waits for the Counter SR Count to be equal to Packet SR Count then generate the FEC sequence.
10.5.3.3#9	NT	A DP OUT Adapter shall not: Count the Link cycles of FEC Symbols for fill count purposes.
10.5.3.4 FEC_DECODE Packet		
10.5.3.4#1	NT	A FEC_DECODE Packet shall have the format shown in Figure 10-47.
10.5.3.4#2	NT	The *PDF* field in the header shall be set to 7 and the *Length* field shall be 14h.
10.5.3.4#3	NT	An FEC Command shall have the format defined in Figure 10-48.
10.5.3.4#4	NT	The three FEC Commands in an FEC_DECODE Packet shall be identical to each other.

10.5.3.4#5	NT	The fields in an FEC Command shall contain the following: **SR Count [29:0]**: This field contains the number of DP Link clock cycles between the last received SR and the first FEC_DECODE_EN or FEC_DECODE_DIS sequences. The minimum value for this field is1h. (occurs when SR is immediately followed by FEC_DECODE sequence).
10.5.3.4#6	NT	The fields in an FEC Command shall contain the following: **FEC DISABLE (FDS) [30]**: This field shall be set to 1b if a FEC_DECODE_DIS sequence was detected. In all other cases it shall be set to 0b.
10.5.3.4#7	NT	The fields in an FEC Command shall contain the following: **FEC ENABLE (FEN) [31]**: This field shall be set to 1b if a FEC_DECODE_EN sequence was detected. In all other cases it shall be set to 0b.
10.5.4 DP OUT Adapter Buffer		
10.5.4#1	NT	A DP OUT Adapter shall implement a buffer that can be used to compensate for the jitter in the latency of the received Tunneled Packets.
10.5.4#2	NT	Deprecated.
10.5.4#3	NT	The DP OUT Adapter transitions from sending self-generated idle pattern to reconstructing the DP Main-Link from the Tunneled Packets after completing the following steps: 1) The DP OUT Adapter shall adjust the PLL frequency at least once as a result of an Adjust PLL event as described in Section 10.6.
10.5.4#4	NT	The DP OUT Adapter transitions from sending self-generated idle pattern to reconstructing the DP Main-Link from the Tunneled Packets after completing the following steps: 2) The DP OUT Adapter ensures, in an implementation specific manner, that within eight PLL frequency adjustments the link symbol clock frequency difference between its own and the DPTX is such that buffer overflow and buffer underrun is avoided.
10.5.4#5	NT	The DP OUT Adapter transitions from sending self-generated idle pattern to reconstructing the DP Main-Link from the Tunneled Packets after completing the following steps: 3) The DP OUT Adapter shall wait to receive an SR from the DP IN Adapter.
10.5.4#6	NT	All Main-Link Path Tunneled Packets, besides DP Clock Sync Packets, are dropped by the DP OUT Adapter until reception of the SR.
10.5.4#7	NT	After the next step is completed, the received SR, shall be the first symbol driven by the DP OUT Adapter as the reconstructed Main-link.
10.5.4#8	NT	The DP OUT Adapter transitions from sending self-generated idle pattern to reconstructing the DP Main-Link from the tunneled packets after completing the following steps: 4) The DP OUT Adapter delays sending the SR in Step 3 for a number of Accumulation Cycles.

10.5.4#9	NT	During the delay, the DP OUT Adapter shall accumulate the DP Main-Link traffic from the DP IN Adapter.
10.5.4.1 Buffer Operation		
10.5.4.1#1	NT	If the buffer becomes empty, a DP OUT Adapter shall continue to drive Dummy Symbols on the DP Main Link, assuming that the next Main-Link Path Tunneled Packet holds a Fill Count value larger than the driven Dummy Cycles.
10.5.4.2 Accumulation Cycles		
10.5.4.2#1	NT	A DP OUT Adapter shall report the Maximum Accumulation Cycles it performs.
10.5.5 HDCP		
10.5.5#1	NT	A DP IN Adapter shall not perform HDCP decryption.
10.5.5#2	NT	It shall not drop or modify an AUX Request or AUX Response associated with HDCP functionality.
10.5.5#3	NT	A DP OUT Adapter shall not perform HDCP encryption.
10.6 DP Link Clock Sync		
10.6.1 Synchronization Method		
10.6.1.1 Events		
10.6.1.1.1 Measuring Events		
10.6.1.1.2 Adjust PLL Event		
10.6.1.2 Lifetime Counter		
10.6.1.2#1	NT	A DP OUT Adapter shall start counting as soon as Link Symbol clock is stable for starting link training with DPRX.
10.6.1.2#1	NT	A DP IN Adapter shall start counting as soon as it completed its equalization process.
10.6.1.2#3	NT	In order to filter out the variation introduced by spread-spectrum modulation, the LC shall be filtered using a first order IIR filter.
10.6.1.2#4	NT	The filtering operation shall be done with 8-bit truncation at the fraction part to assure reproducible result.
10.6.1.2#5	NT	All operands of IIR filter shall have the same format of 64 bits of integer followed by 8 bits of fraction.

10.6.1.3 DP Clock Sync Packet		
10.6.1.3#1	NT	A DP Clock Sync Packet shall have the format shown in Figure 10-53.
10.6.1.3#2	NT	The fields forming a DP Clock Sync Packet shall be as defined below: **Reserved**: This field is reserved and shall be set to 0.
10.6.1.3#3	NT	The fields forming a DP Clock Sync Packet shall be as defined below: **Window Count**: This field is defined in Section 10.6.2.1. The *Window Count* field structure is shown in Figure 10-52(A).
10.6.1.3#4	NT	The fields forming a DP Clock Sync Packet shall be as defined below: **FLC**: This field contains the snapshot of the Filtered Lifetime Counter at the time the Window Measured Event occurred.
10.6.1.3#5	NT	The fields forming a DP Clock Sync Packet shall be as defined below: **CRC32**: This field contains a CRC32 computed over the entire payload using the following DW order: DW1, DW3, DW2, DW7, DW6, DW5, DW4. The following CRC shall be used: Width: 32; Poly: 1EDC 6F41h; Init: FFFF FFFFh; RefIn: True; RefOut: True; XorOut: FFFF FFFFh.
10.6.2 DP Adapter Requirements		
10.6.2.1 DP IN Adapter Requirements		
10.6.2.1#1	NT	A DP IN Adapter shall: Implement a Lifetime Counter as described in Section 10.6.1.1.2.
10.6.2.1#2	NT	A DP IN Adapter shall: Implement the logic to perform the LC filtering.
10.6.2.1#3	NT	A DP IN Adapter shall: Update FLC upon an Update Counter Event.
10.6.2.1#4	NT	A DP IN Adapter shall: Upon the first Measure Window Event: Capture the current FLC; Store the current captured FLC to be used as previous captured FLC at the next Measure Window Even.
10.6.2.1#5	NT	A DP IN Adapter shall: Upon each subsequent Measure Window Event: Capture the current FLC; Compute the Window Count by calculating the current captured FLC minus the FLC that was captured at the previous Measure Event; Construct a DP Clock Sync Packet and send it over the Main-Link Path within tDPClockSync after the Measure Window Event; Store the current captured FLC to be used as previous captured FLC at the next Measure Window Event.
10.6.2.2 DP OUT Adapter Requirements		
10.6.2.2#1	NT	A DP OUT Adapter shall: Implement a Lifetime Counter as described in Section 10.6.1.2.
10.6.2.2#2	NT	A DP OUT Adapter shall: Implement the logic to perform the LC filtering.
10.6.2.2#3	NT	A DP OUT Adapter shall: Update FLC upon an Update Counter Event.

10.6.2.2#4	NT	A DP OUT Adapter shall: Upon a Measure Window Event: Capture the current FLC; Compute the Window Count as described in Section 10.6.1.3.
10.6.2.2#5	NT	A DP OUT Adapter shall: Upon receiving a DP Clock Sync Packet after the Measure Window Event and before the PLL Adjust Event, compute the PLL frequency adjustment. The method for computing the PLL frequency adjustment is outside the scope of this specification.
10.6.2.2#6	NT	A DP OUT Adapter shall: Upon an Adjust PLL Event, adjust the PLL frequency based on the computation performed at the Measure Window Event.
10.6.2.2#7	NT	If a DP OUT Adapter receives a DP Clock Sync Packet after an Adjust PLL Event but before the next Measure Window Event, it shall not adjust the PLL and shall silently discard the packet.
10.6.2.2#8	NT	If a DP OUT Adapter receives a DP Clock Sync Packet before it computed the first Window Count, it shall not adjust the PLL and shall silently discard the packet.
10.6.2.2#9	NT	When a DP OUT Adapter changes the DisplayPort Main-Link transmitter frequency as a result of adjusting the PLL frequency, it shall adhere to the DisplayPort 1.4a Specification.
10.6.2.2#10	NT	The PLL frequency adjustment shall be completed within tDPPLLAdjust after the Adjust PLL Event.
10.7 DP BW Allocation Mode		
10.7#1		If a DP IN Adapter supports DP BW Allocation Mode, it shall do so as defined in this section.
10.7.1 DP BW Allocation Mode Enablement		
10.7.1#1		If a DP IN Adapter supports DP BW Allocation Mode, it shall: Set the DP_LOCAL_CAP.DP_IN_BW_Allocation Mode Support bit to 1b.
10.7.1#2		If a DP IN Adapter supports DP BW Allocation Mode, it shall: Update the AUX Response for DPCD DP TUNNELING and PANEL REPLAY OPTIMIZATION SUPPORT. DP_IN_BW_Allocation_Mode_Support (E000Dh, bit 7) to 1b.
10.7.1#3		If a DP IN Adapter supports DP BW Allocation Mode, it shall: Update the AUX Response for DPCD USB4_DRIVER_BW_CAPABILITY.USB4_Driver_BW Allocation Mode Support (E0020h, bit 7) to have the same value as ADP_DP_CS_2.CM BW Allocation Mode Support.
10.7.1#4		When a Connection Manager changes ADP_DP_CS_2.CM BW Allocation Mode Support bit, a DP IN Adapter shall: Set the BW_Allocation_Capability_Changed field to 1b in DP_TUNNELING_STATUS DPCD register.

10.7.1#5		When a Connection Manager changes ADP_DP_CS_2.CM BW Allocation Mode Support bit, a DP IN Adapter shall: Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h)
10.7.1#6		When a Connection Manager changes ADP_DP_CS_2.CM BW Allocation Mode Support bit, a DP IN Adapter shall: If Unmask_BW_Allocation_IRQ is 1b, generate an IRQ_HPD.
10.7.1#7		When DPTX sets DPTX_BW_ALLOCATION_MODE_CONTROL.DP_Display_Driver_BW_Allocation_ Mode_Enable (E0030h, bit 7) to 1b, a DP IN Adapter shall: Enable DP BW Allocation Mode.
10.7.1#8		When DPTX sets DPTX_BW_ALLOCATION_MODE_CONTROL.DP_Display_Driver_BW_Allocation_ Mode_Enable (E0030h, bit 7) to 1b, a DP IN Adapter shall: Send the Connection Manager a Notification Packet with Event Code = DP_BW as defined in Table 6-11.
10.7.2 Interaction with DPTX		
10.7.2#1		When a DP IN Adapter receives a DPCD AUX Write transaction that targets a DPCD register within Table 10-23, and the targeted DPCD field Type is Read/Write, it shall update the corresponding field in Adapter configuration space with the value of the write transaction.
10.7.2#2		When a DP IN Adapter receives a DPCD AUX Read transaction that targets a DPCD register within Table 10-23, and the targeted DPCD field Type is Read Only, it shall update the read transaction with the value in the corresponding field in Adapter Configuration Space.
10.7.2#3		When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW register, a DP IN Adapter shall: Store the current Allocated BW in an internal variable.
10.7.2#4		When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW register, a DP IN Adapter shall: If the recovery timer is advancing, stop and reset it.
10.7.2#5		When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW register, a DP IN Adapter shall: Initiate a bandwidth request handshake with the Connection Manager as defined in Section 10.7.3.
10.7.2#6		When a Connection Manager writes a value to the Allocated BW field that is equal to or greater than the Requested BW, a DP IN Adapter shall: Set the BW Request Succeeded field to 1b in DP_TUNNELING_STATUS DPCD register.

10.7.2#7		When a Connection Manager writes a value to the Allocated BW field that is equal to or greater than the Requested BW, a DP IN Adapter shall: Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h).
10.7.2#8		When a Connection Manager writes a value to the Allocated BW field that is equal to or greater than the Requested BW, a DP IN Adapter shall: If Unmask_BW_Allocation_IRQ is 1b, generate an IRQ_HPD.
10.7.2#9		When a Connection Manager writes a value to the Allocated BW field that is equal to or greater than the Requested BW, a DP IN Adapter shall: If the ESTIMATED_BW field was locked for updates due to bandwidth request failure, unlock it.
10.7.2#10		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: Set the ESTIMATED_BW field to the Allocated BW, and lock its value (i.e. ignore any changes in the Estimated_BW field).
10.7.2#11		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: Set the BW Request Failed to 1b in DP_TUNNELING_STATUS DPCD register.
10.7.2#12		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h).
10.7.2#13		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: If Unmask_BW_Allocation_IRQ is 1b, generate an IRQ_HPD.
10.7.2#14		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: Start the recovery timer.
10.7.2#15		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: If the recovery timer has reached tDPBWRecoveryTimeout, the DP IN Adapter initiates a bandwidth allocation request. The DP BW that a DP IN Adapter requests shall be the same bandwidth as before the failed bandwidth allocation (i.e. the same value as in the Allocated BW field before the DPTX last updated the DPCD Requested BW register).
10.7.2.1 Estimated Bandwidth		
10.7.2.1#1		Upon a change in the Estimated BW field, a DP IN adapter shall: Set Estimated BW Changed bit in the DPCD DP_TUNNELING_STATUS register to 1b.

10.7.2.1#2		Upon a change in the Estimated BW field, a DP IN adapter shall: Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_
10.7.2.1#3		Upon a change in the Estimated BW field, a DP IN adapter shall: If Unmask_BW_Allocation_IRQ is 1b, generate an IRQ_HPD.
10.7.3 Interaction with the Connection Manager		
10.7.3#1		When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW field, a DP IN Adapter shall: 1)Set the ADP_DP_CS_8.DPTX Req field to 1b; 2) Send the Connection Manager a Notification Packet with Event Code = DP_BW as defined in Table 6-11; 3)Wait for the Connection Manager to set the ADP_DP_CS_2.CM Ack bit to 1b; 4) Set the ADP_DP_CS_8.DPTX Req field to 0b.
10.8 Timing Parameters		

Chapter 13 Assertions

Assertion #	How to Test	Assertion Description
13 TBT3 Compatibility		
13.8.1.1 DP IN Adapter Requirements		
13.8.1.1#1	TBD	A DP IN Adapter operating in TBT3-Compatible mode follows the requirements listed in Section 10.4.4.2.1 except the following: The Link Status DPCD registers, as defined in Table 10-9, shall be mapped statically as Internal registers.
13.8.1.1#2	TBD	A DP IN Adapter operating in TBT3-Compatible mode follows the requirements listed in Section 10.4.4.2.1 except the following: DPCD address 00600h is mapped as Internal register.
13.8.1.1#3	TBD	A DP IN Adapter operating in TBT3-Compatible mode follows the requirements listed in Section 10.4.4.2.1 except the following: An AUX Read Transaction to the LTTPR DPCD Field, addresses F0000h-F02FFh, are mapped as Internal registers. A DP IN Adapter shall set the data of the AUX Response to 0h.
13.8.1.1#4	TBD	A DP IN Adapter operating in TBT3-compatible mode follows the requirements listed in Section 10.4.4.5 except the following: DSC Support field in the DSC SUPPORT DPCD register shall always be set to 0b.
13.8.1.1#5	TBD	A DP IN Adapter operating in TBT3-compatible mode follows the requirements listed in Section 10.4.4.5 except the following: FEC_CAPABLE field in FEC_CAPABILITY DPCD register shall always be set to 0b.

Test Setups

Host with DP IN Adapter

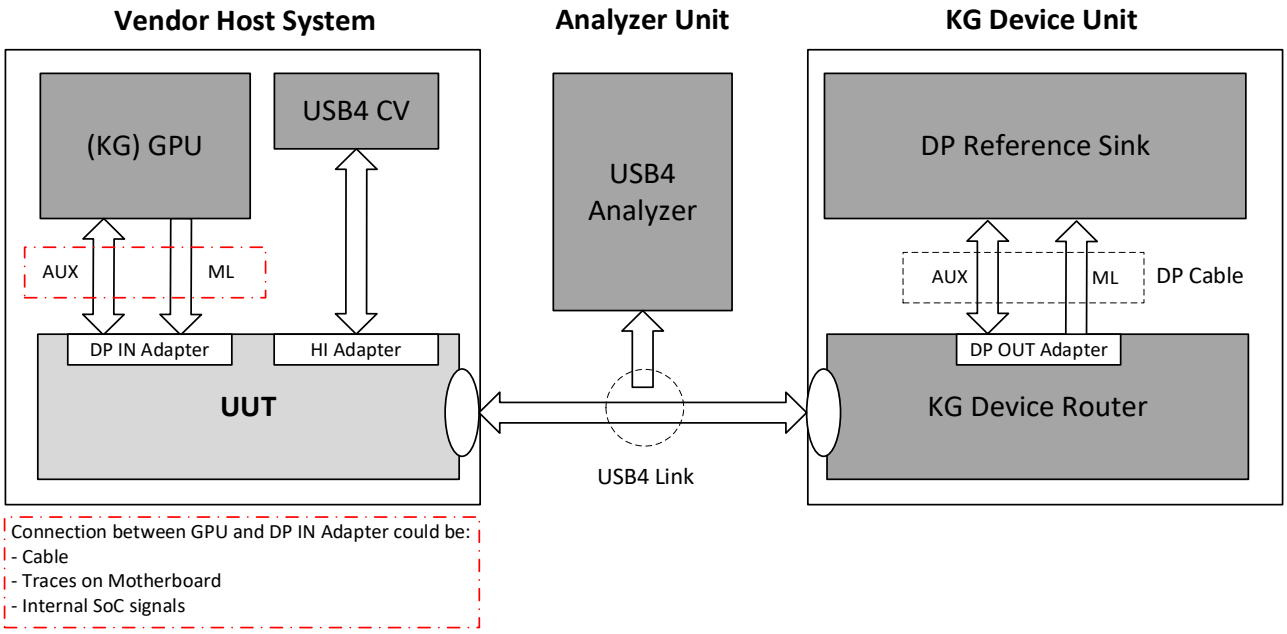
This section describes the test setups for a Host Router that contains a DP IN Adapter.

AN_HOST_DFP1—DPIN_01

This section describes the test setup for a Host Router that is running DP IN Adapter general testing.

- Vendor provides host system for UUT with a Host Router and a GPU in one of the following configurations:
    - The Host Router and the GPU are integrated into the same SoC
    - The Host Router and the GPU are both down on the motherboard
    - The Host Router is an Add-in Card connected to a KG GPU (or DP Source) through a cable
- KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout)
- In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 16
- USB4 CV should be installed on the Vendor host system
- KG Device Unit connects to the UUT and presents as UFP
- KG Device Unit contains:
    - KG Device Router
    - DP Reference Sink CTS tools

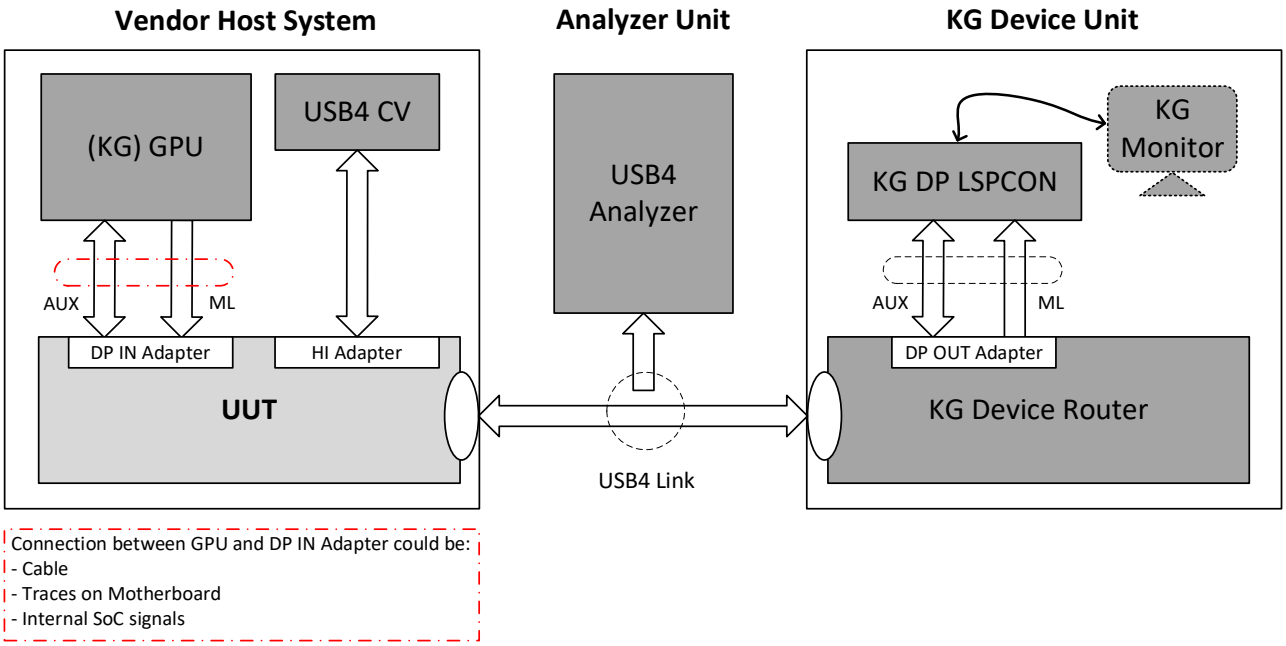
A USB4 Host must support DP Alt mode on its DFPs. The full VESA CTS shall be run on a Host system with a DP Reference Sink in DP Alt Mode.


Vendor Host System
Analyzer Unit
KG Device Unit
(KG) GPU
USB4 CV
USB4 Analyzer
DP Reference Sink
AUX
ML
AUX
ML
DP Cable
DP IN Adapter
HI Adapter
DP OUT Adapter
UUT
KG Device Router
USB4 Link
Connection between GPU and DP IN Adapter could be:
- Cable
- Traces on Motherboard
- Internal SoC signals

AN_HOST_DFP1—DPIN_02

This section describes the test setup for a Host Router running DP IN Adapter specific testing.

- Vendor provides host system for UUT with a Host Router and a GPU in one of the following configurations:
    - The Host Router and the GPU are integrated into the same SoC
    - The Host Router and the GPU are both down on the motherboard
    - The Host Router is an Add-in Card connected to a KG GPU (or DP Source) through a cable
- KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout)
- In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 16
- USB4 CV should be installed on the Vendor host system
- KG Device Unit connects to the UUT and presents as UFP
- KG Device Unit contains:
    - KG Device Router
    - KG DP LSPCON dongle and KG monitor



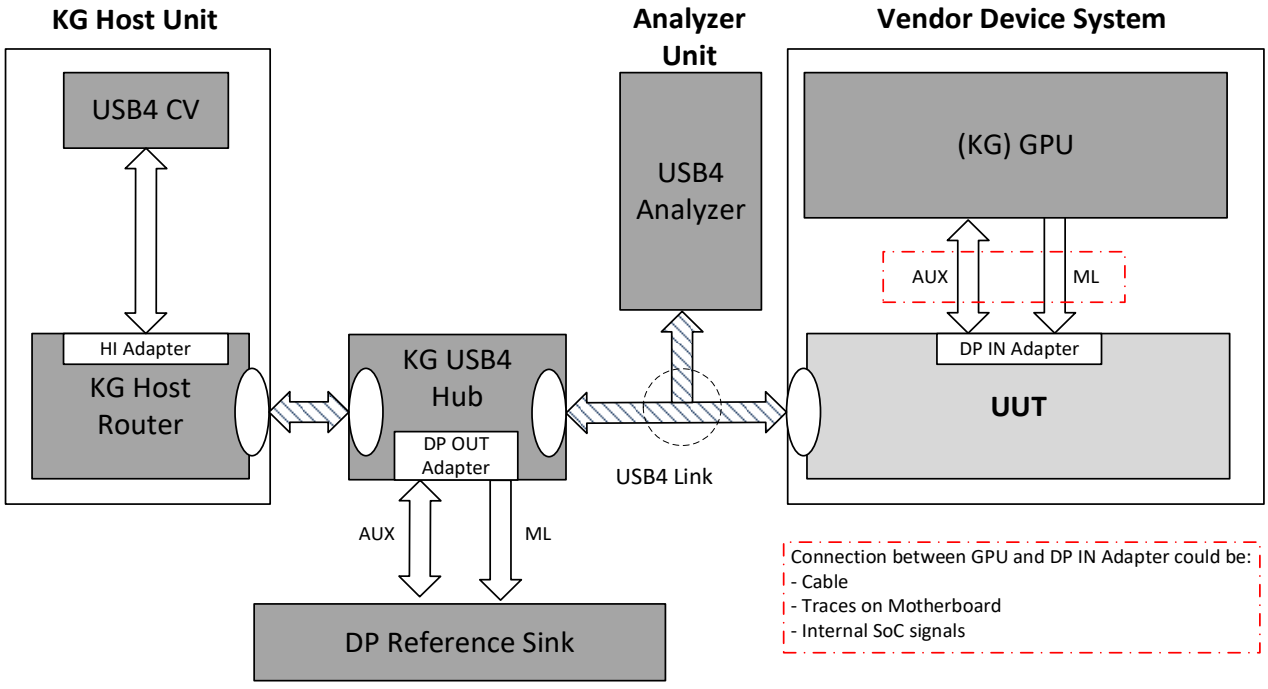
Device with DP IN Adapter

This section describes the test setups for a Device Router that contains a DP IN Adapter and no USB4 DFP.

AN_DEV_UFP1—DPIN_03

This section describes the test setup for a Device Router running DP IN Adapter general testing.

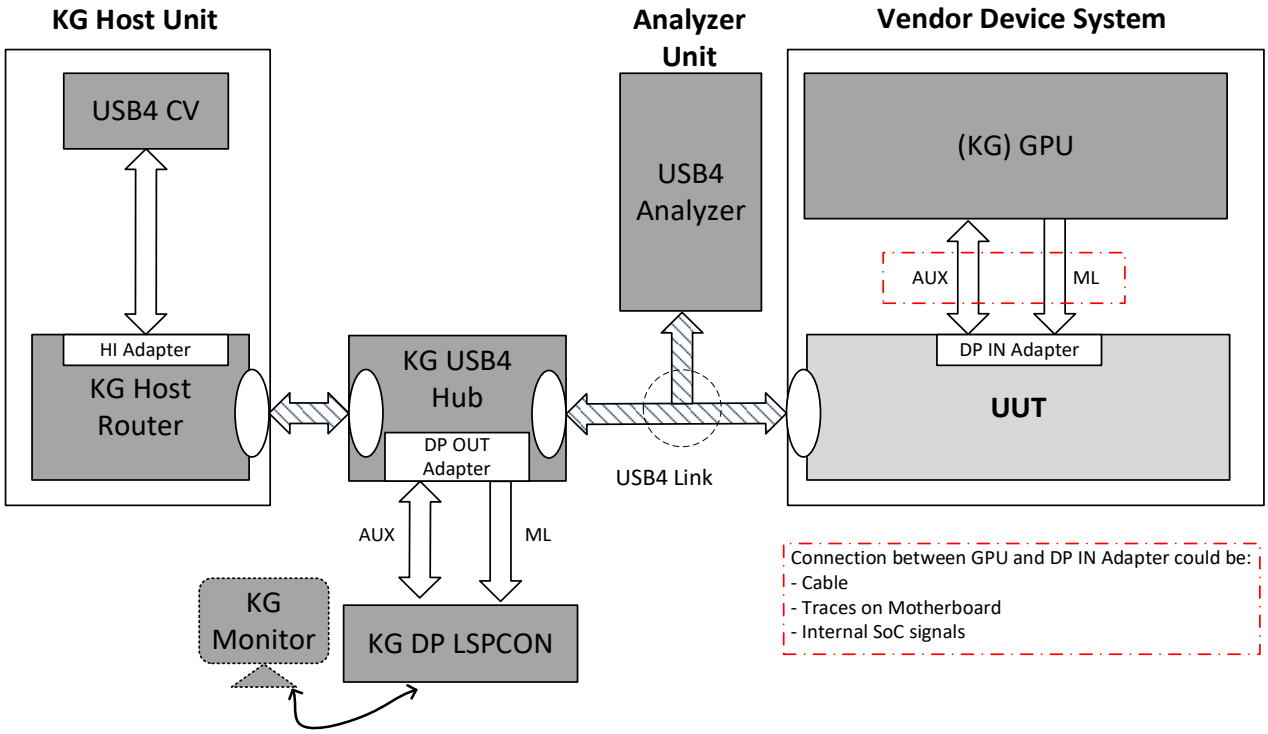
- Vendor provides Device System for UUT with a Device Router and a GPU in one of the following configurations:
    - The Device Router and the GPU are integrated into the same SoC
    - The Device Router and the GPU are both down on a motherboard
    - The Device Router is connected to a KG GPU (or DP Source) through a cable
- KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout)
- In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 16
- KG Host Unit with USB4 CV installed
- KG USB4 Hub with at least two USB4 DFPs
- DP Reference Sink CTS tools



AN_DEV_UFP1—DPIN_04

This section describes the test setup for a Device Router running DP IN Adapter specific testing.

- Vendor provides Device System for UUT with a Device Router and a GPU in one of the following configurations:
    - The Device Router and the GPU are integrated into the same SoC
    - The Device Router and the GPU are both down on a motherboard
    - The Device Router is connected to a KG GPU (or DP Source) through a cable
- KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout)
- In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 16
- KG Host Unit with USB4 CV installed
- KG USB4 Hub with at least two USB4 DFPs
- KG DP LSPCON Dongle and KG monitor



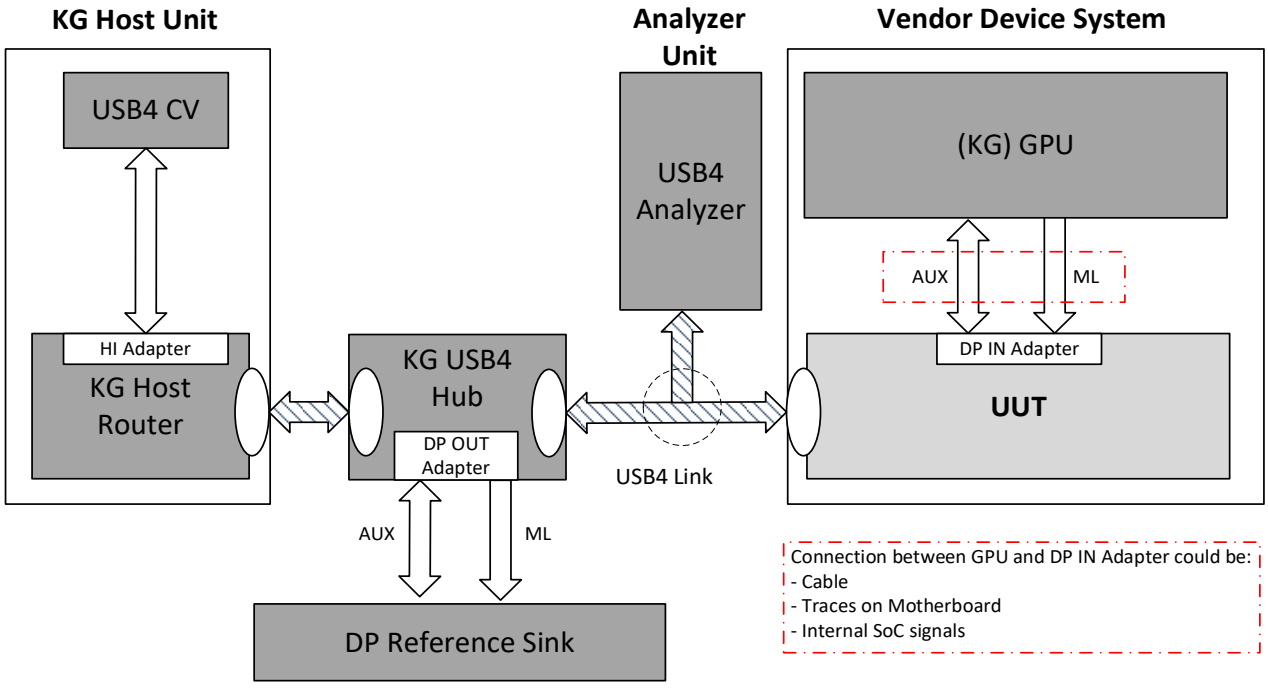
Hub with DP IN Adapter

This section describes the test setups for a Device Router that contains a DP IN Adapter and one or more USB4 DFP.

AN_HUB_UFP1—DPIN_05

This section describes the test setup for a Device Router running DP IN Adapter general testing.

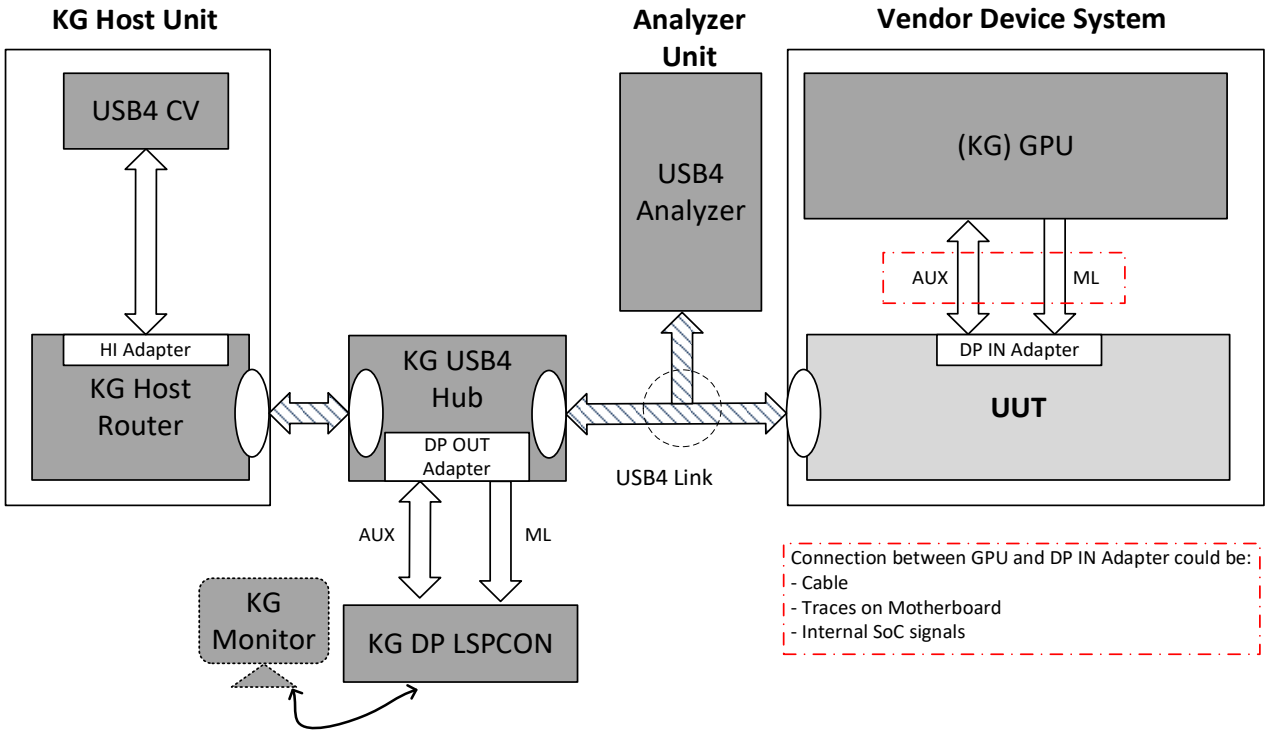
- Vendor provides Device System for UUT with a Device Router and a GPU in one of the following configurations:
    - The Device Router and the GPU are integrated into the same SoC
    - The Device Router and the GPU are both down on a motherboard
    - The Device Router is connected to a KG GPU (or DP Source) through a cable
- KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout)
- In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 16
- KG Host Unit with USB4 CV installed
- KG USB4 Hub with at least two USB4 DFPs
- DP Reference Sink CTS tools



AN_HUB_UFP1—DPIN_06

This section describes the test setup for a Device Router running DP IN Adapter specific testing.

- Vendor provides Device System for UUT with a Device Router and a GPU in one of the following configurations:
    - The Device Router and the GPU are integrated into the same SoC
    - The Device Router and the GPU are both down on a motherboard
    - The Device Router is connected to a KG GPU (or DP Source) through a cable
- KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout)
- In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 16
- KG Host Unit with USB4 CV installed
- KG USB4 Hub with at least two USB4 DFPs
- KG DP LSPCON Dongle and KG monitor



Host with DP OUT Adapter

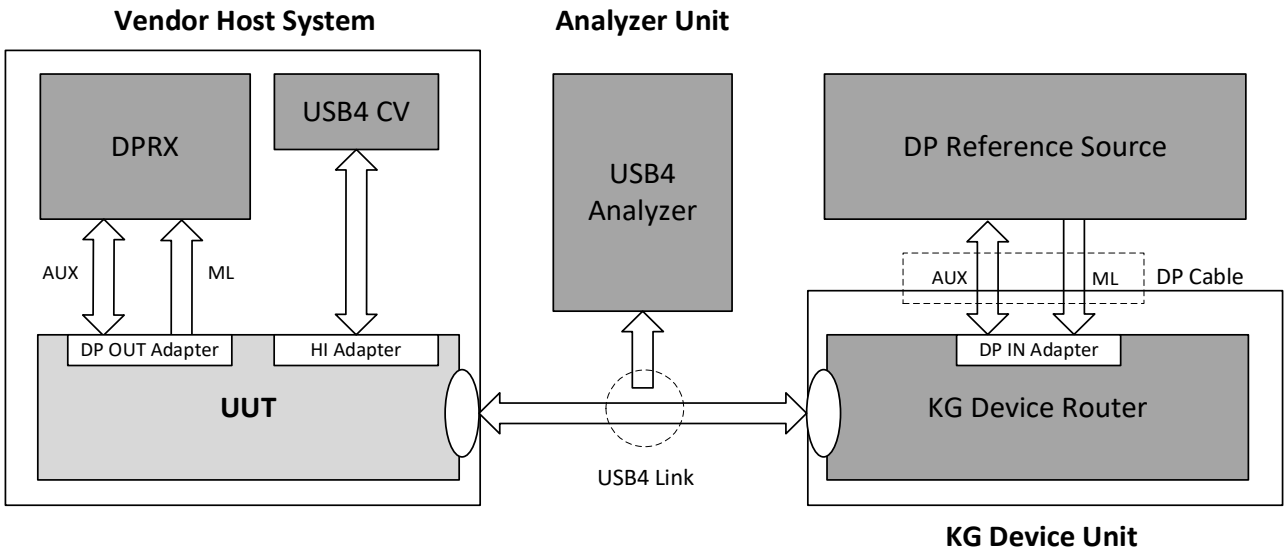
This section describes the test setups for a Host Router that contains a DP OUT Adapter. This setup is for a DP OUT Adapter that is integrated with a DPRX.

AN_HOST_DFP1—DPOUT_01

This section describes the test setup for a Host Router running DP OUT Adapter general testing.

- Vendor provides host system for UUT with an integrated DPRX connected to the DP OUT Adapter.
- USB4 CV should be installed on the Vendor host system
- KG Device Unit connects to UUT and presents as UFP
- KG Device Unit contains a KG Device Router with a DP IN Adapter that connects to an exposed connector
- DP Reference Source CTS tools

Note: A KG Device Router with a DP IN Adapter is not available yet. This test setup is not currently used.



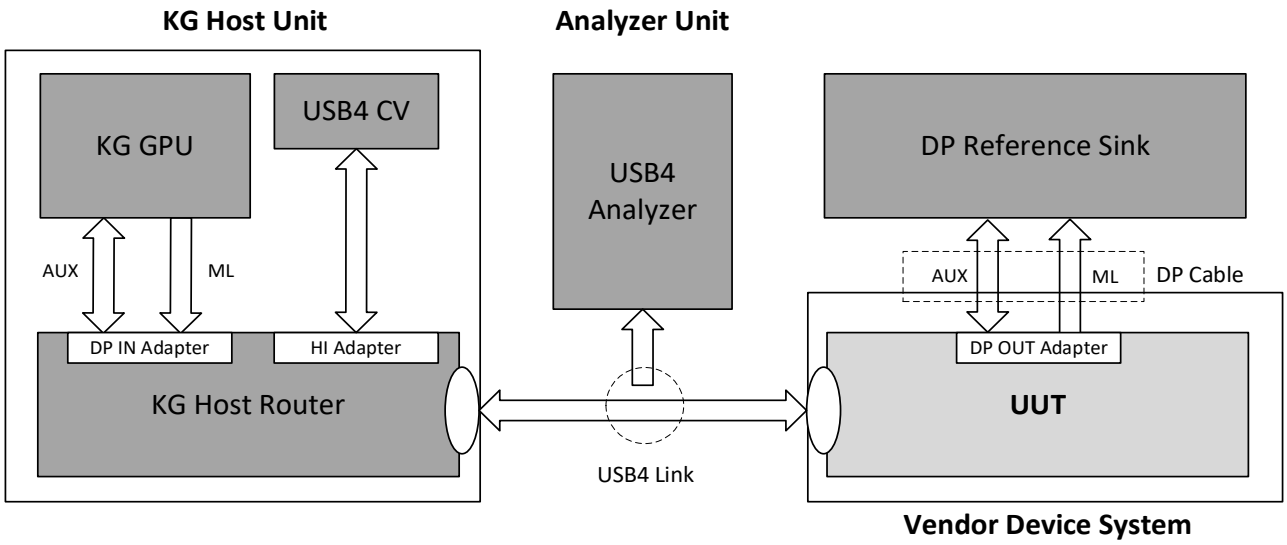
Device with DP OUT Adapter

This section describes the test setups for a Device Router that contains a DP OUT Adapter and no USB4 DFP.

AN_DEV_UFP1—DPOUT_02

This section describes the test setup for a Device Router running DP OUT Adapter general testing. This setup is for a DP OUT that connects to an exposed connector.

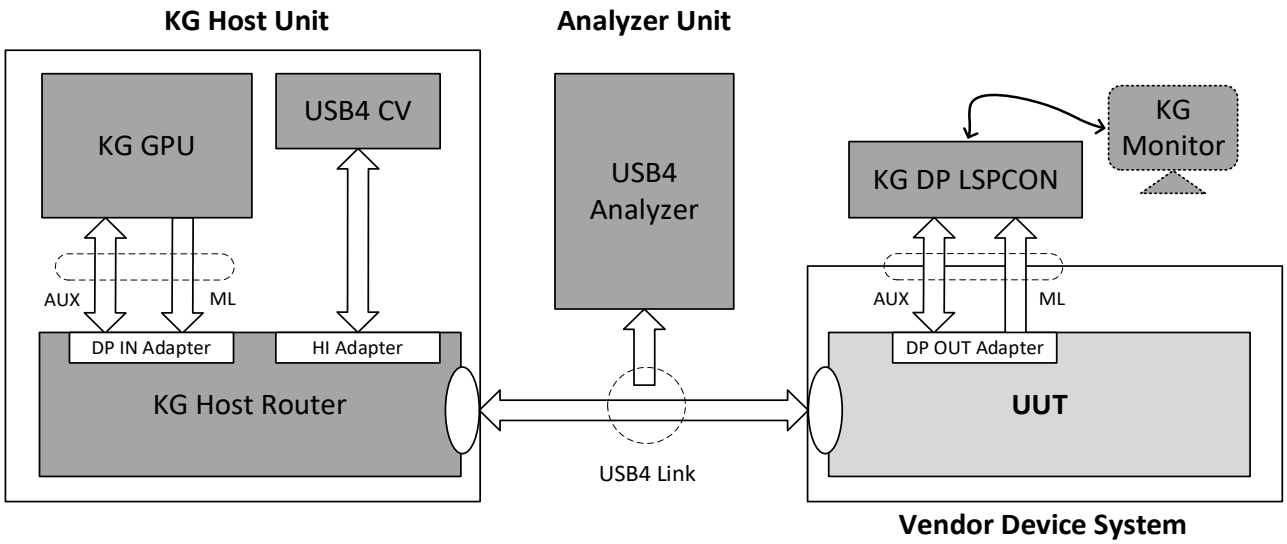
- Vendor provides Device System for UUT with an exposed connector
- DP Reference Sink CDT tools
- KG Host Unit connects to UUT and presents as DFP
- KG Host Unit contains:
    - KG Host Router
    - KG GPU
    - USB4 CV
- KG GPU(s) (or DP Source) are VESA compliant and LTTPR Aware (provides the 3.2 ms AUX Timeout) and shall meet the capability requirements outlined in Table 16



AN_DEV_UFP1—DPOUT_03

This section describes the test setup for a Device Router running DP OUT Adapter specific testing. This setup is for a DP OUT that connects to an exposed connector.

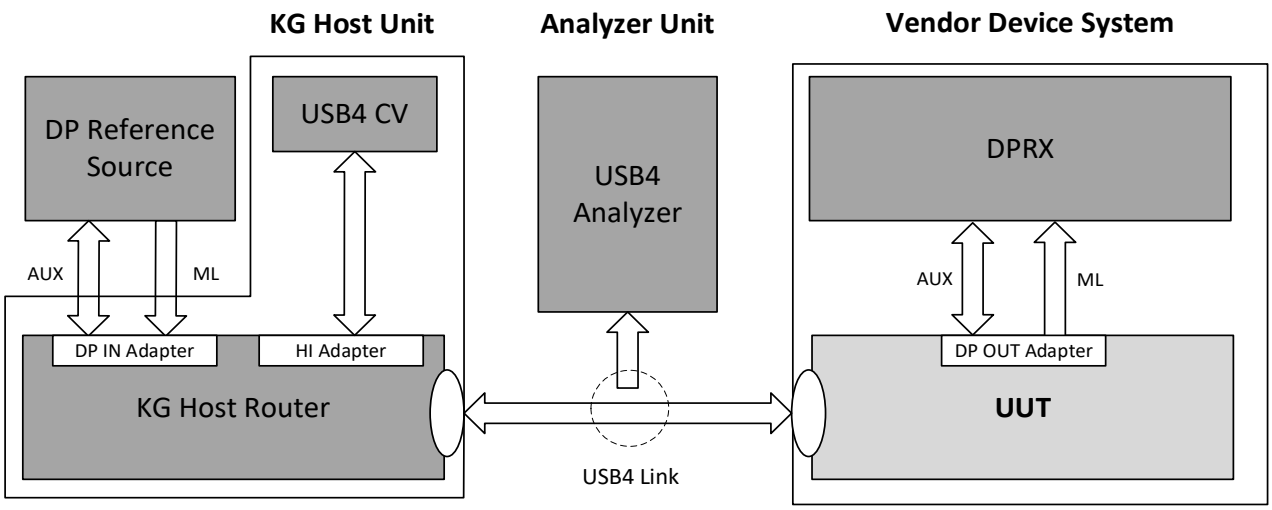
- Vendor provides Device System for UUT with an exposed connector
- KG DP LSPCON Dongle and KG monitor
- KG Host Unit connects to UUT and presents as DFP
- KG Host Unit contains:
    - KG Host Router
    - KG GPU
    - USB4 CV
- KG GPU(s) (or DP Source) are VESA compliant and LTTPR Aware (provides the 3.2 ms AUX Timeout) and shall meet the capability requirements outlined in Table 16



AN_DEV_UFP1—DPOUT_04

This section describes the test setup for a Device Router running DP OUT Adapter general testing. This setup is for a DP OUT Adapter that is integrated with a DPRX.

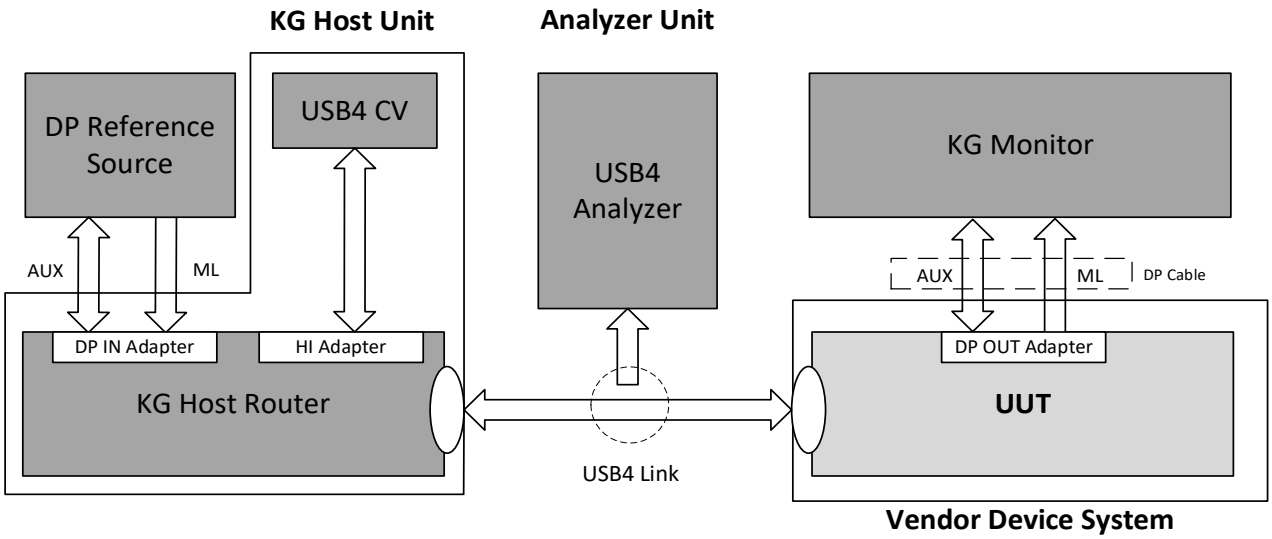
- Vendor provides Device System for UUT with an integrated DPRX
- DP Reference Source CTS tools
- KG Host Unit connects to UUT and presents as DFP
- KG Host Unit contains:
    - KG Host Router
    - USB4 CV



AN_DEV_UFP1—DPOUT_05

This section describes the test setup for a Device Router running DP OUT Adapter general testing. This setup is for a DP OUT that connects to an exposed connector.

- Vendor provides Device System for UUT with an exposed connector
- KG Monitor
- DP Reference Source CTS tools
- KG Host Unit connects to UUT and presents as DFP
- KG Host Unit contains:
    - KG Host Router
    - USB4 CV



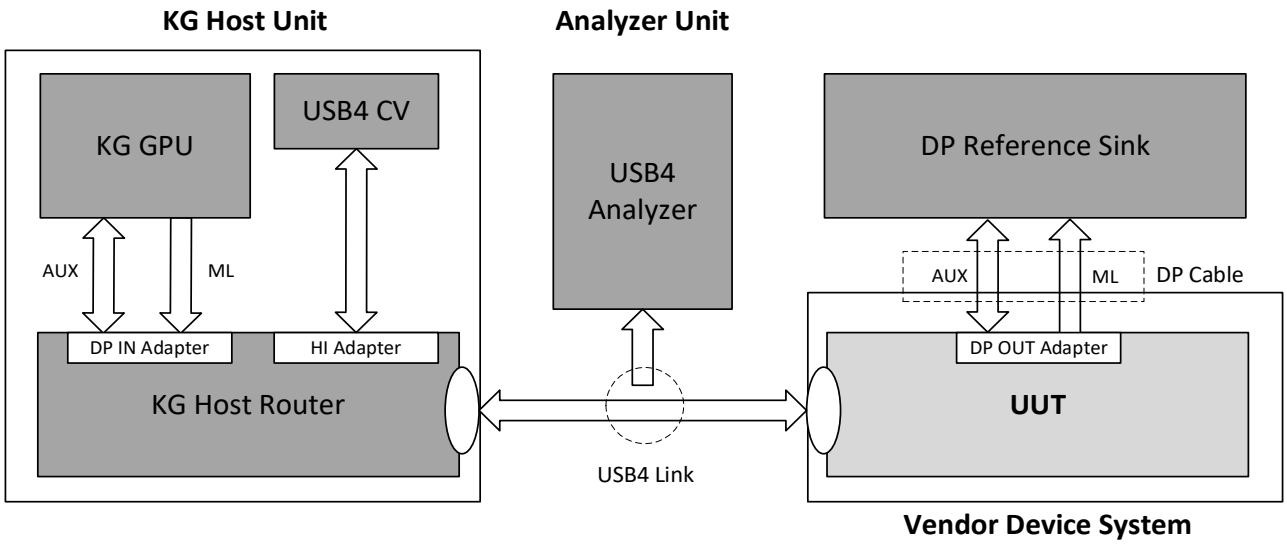
Hub with DP OUT Adapter

This section describes the test setups for a Device Router that contains a DP OUT Adapter and one or more USB4 DFP.

AN_HUB_UFP1—DPOUT_06

This section describes the test setup for a Device Router running DP OUT Adapter general testing. This setup is for a DP OUT that connects to an exposed connector.

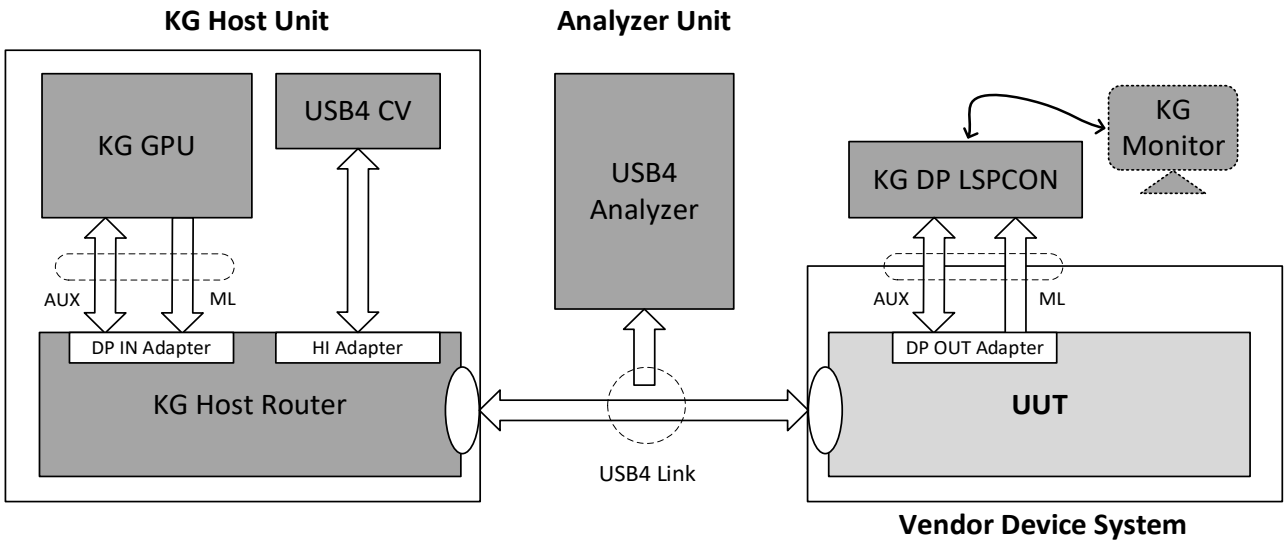
- Vendor provides Device System for UUT with an exposed connector
- DP Reference Sink CDT tools
- KG Host Unit connects to UUT and presents as DFP
- KG Host Unit contains:
    - KG Host Router
    - KG GPU
    - USB4 CV
- KG GPU(s) (or DP Source) are VESA compliant and LTTPR Aware (provides the 3.2 ms AUX Timeout) and shall meet the capability requirements outlined in Table 16



AN_HUB_UFP1—DPOUT_07

This section describes the test setup for a Device Router running DP OUT Adapter specific testing. This setup is for a DP OUT that connects to an exposed connector.

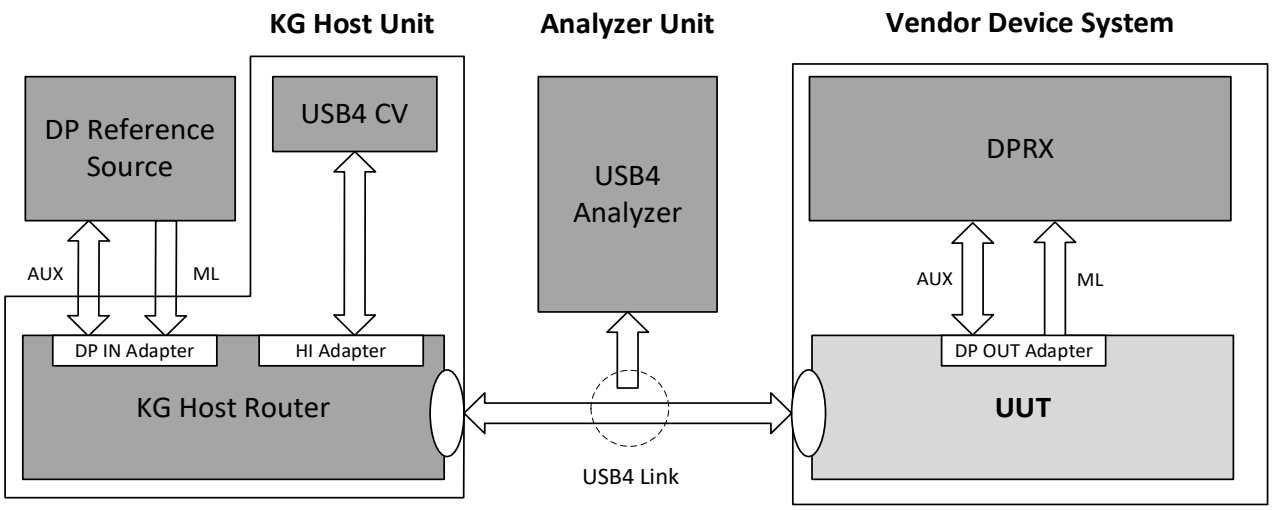
- Vendor provides Device System for UUT with an exposed connector
- KG DP LSPCON Dongle and KG monitor
- KG Host Unit connects to UUT and presents as DFP
- KG Host Unit contains:
    - KG Host Router
    - KG GPU
    - USB4 CV
- KG GPU(s) (or DP Source) are VESA compliant and LTTPR Aware (provides the 3.2 ms AUX Timeout) and shall meet the capability requirements outlined in Table 16



AN_HUB_UFP1—DPOUT_08

This section describes the test setup for a Device Router running DP OUT Adapter general testing. This setup is for a DP OUT Adapter that is integrated with a DPRX.

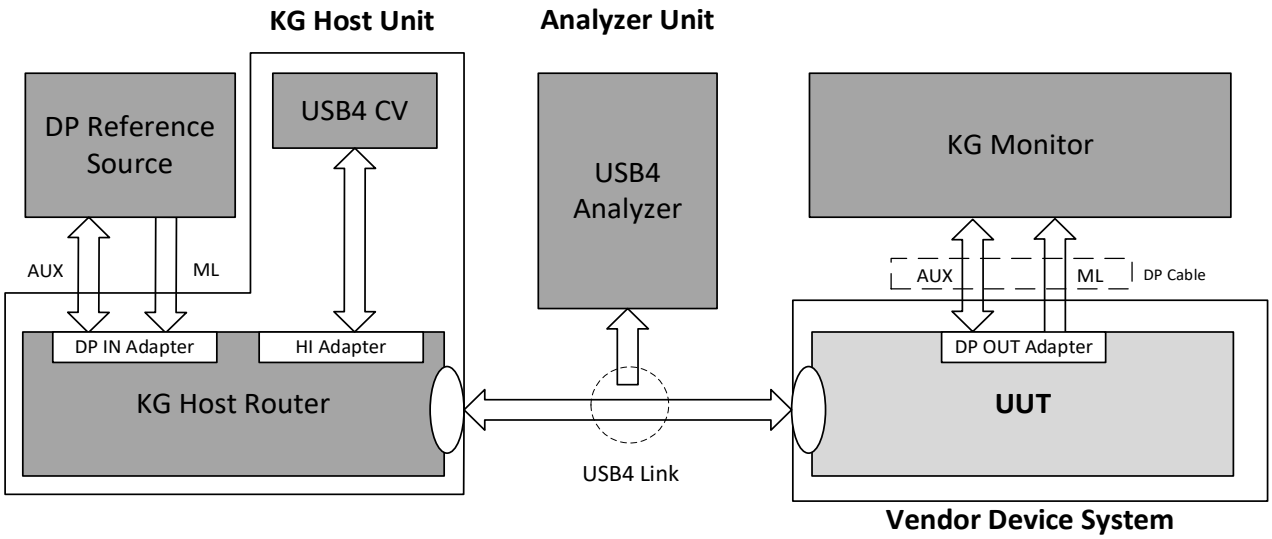
- Vendor provides Device System for UUT with an integrated DPRX
- DP Reference Source CTS tools
- KG Host Unit connects to UUT and presents as DFP
- KG Host Unit contains:
    - KG Host Router
    - USB4 CV



AN_HUB_UFP1—DPOUT_09

This section describes the test setup for a Device Router running DP OUT Adapter general testing. This setup is for a DP OUT that connects to an exposed connector.

- Vendor provides Device System for UUT with an exposed connector
- KG Monitor
- DP Reference Source CTS tools
- KG Host Unit connects to UUT and presents as DFP
- KG Host Unit contains:
    - KG Host Router
    - USB4 CV



USB4 Naming Convention Changes

- DisplayPort DP Reference Sink – USB4 DP Sink.
- Source DUT functionality is split between DP IN Adapter in UUT and DP OUT Adapter in KG Device Router.
- In DP CTS tests including a Source DUT writes to Exerciser DP Sink DPCD, The writes are performed by the DP OUT Adapter in KG Device Router.

DP Question List

DP IN Adapter Capability Question List

Question	Answer
What is the maximum supported lane count?	1 lane 2 lanes 4 lanes
What is the maximum supported link rate (and associated bit rate)?	1.62Gbps/lane (RBR) 2.7Gbps/lane (HBR) 5.4Gbps/lane (HBR2) 8.1Gbps/lane (HBR3)
What is the Maximal DPCD Rev?	DPCD r1.1 DPCD r1.2 DPCD r1.3 DPCD r1.4a
Does Router support MST?	Not supported Supported
Does Router Support FEC?	Not supported Supported
Does Router support SST SDP Split	Not supported Supported
Does Router support LTTPR?	Not supported Supported
Does Router support DSC?	Not supported Supported
Does Router support HDCP	Not supported Supported

DP OUT Adapter Capability Question List

Question	Answer
What is the maximum supported lane count?	1 lane 2 lanes 4 lanes
What is the maximum supported link rate (and associated bit rate)?	1.62Gbps/lane (RBR) 2.7Gbps/lane (HBR) 5.4Gbps/lane (HBR2) 8.1Gbps/lane (HBR3)
What is the Maximal DPCD Rev?	DPCD r1.1 DPCD r1.2 DPCD r1.3 DPCD r1.4a
Does Router support MST?	Not supported Supported
Does Router Support FEC?	Not supported Supported
Does Router support SST SDP Split	Not supported Supported
Does Router support LTTPR?	Not supported Supported
Does Router support DSC?	Not supported Supported
Does Router support HDCP	Not supported Supported
Does the DP OUT Adapter connect to a USB Type-C connector	Not supported Supported

Test Descriptions

DP IN Adapter Tests

TD 10.001 DP IN Adapter Configuration Capability TD_DP IN_1

A. Purpose:

- Verify that a DP IN Adapter contains the correct values in the Adapter Configuration Space Basic Attributes and DP Configuration Capability

B. Asserts:

- 10.2.1#1
- 10.2.2#1
- 10.3.2.2#1
- 10.4.2.1#5
- 10.4.2.2#1
- 10.4.3.5#1
- 10.4.3.5#2
- 10.4.3.5#3

C. Setup:

- AN_HOST_DFP1—DPIN_01 or AN_HOST_DFP1—DPIN_02
- AN_DEV_UFP1—DPIN_03
- AN_HUB_UFP1—DPIN_05

D. Procedure:

USB4 CV performs the following steps:

Part 1 – Verify Default Values

1. Connect the setup without the DP Reference Sink
2. Read the Adapter Configuration Space of DP IN Adapter on the UUT
3. Basic Attributes shell have the values as in Table 1
4. DP Configuration Capability shell have the values as in Table 2
5. Connect the DP Reference Sink to the KG Device Router
6. Configure DP path after getting a HOT Plug Event Packet from the DP OUT Adapter, according to Universal Serial Bus 4 (USB4™) Connection Manager Guide section 5.4.
7. It is a test failure if the DPRX capabilities Read Done bit is not 1b within 5 sec
8. Read the Adapter Configuration Space of the DP IN on the UUT
9. Verify that the Basic Attributes have the values in Table 1
10. Verify that the DP Configuration Capability has the values in Table 2

Part 2 – Verify Configuration Bits

11. Wait for the DP link to be stable
12. Set the SWLI bit to 1b in the DP IN Adapter in the UUT
13. Verify that the DP IN Adapter initiates Link training
14. Wait for the DP link to be stable
15. Write to HPDC in the DP IN Adapter in the UUT
16. Verify that the HPD toggles between DP IN Adapter and DPTX.
17. Write to HPDS in the DP IN Adapter in the UUT
18. Verify that HPD is set between DP IN Adapter and DPTX

Part 3 – Verify Default Values After Path Teardown

19. Disconnect the DP Reference Sink from the KG Device Router
20. After receiving a Hot Unplug Event Packet from the DP OUT Adapter, tear down the DP Path as described in Section 5.4 of the Universal Serial Bus 4 (USB4™) Connection Manager Guide
21. Read the Adapter Configuration Space of the DP IN Adapter in the UUT
22. Verify that the Basic Attributes have the default values described in Table 1
23. Verify that the DP Configuration Capability has the values described in Table 2

Table 1 – Adapter Configuration Space Basic Attributes

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value		Paired
0	ADP_CS_0	31:0	Vendor Defined	VD	Vendor Defined		VD
1	ADP_CS_1	7:0	Next Capability Pointer	RO	Vendor Defined		VD
		18:8	Max Counter Sets	RO	Vendor Defined		VD
		19	Counters Configuration Space (CCS) Flag	RO	Vendor Defined		VD
		31:20	Reserved	Rsvd	0		0
2	ADP_CS_2	7:0	Adapter Type Sub-type	RO	IN 01h	OUT 02h	01/02
		15:8	Adapter Type Version	RO	01h		01
		23:16	Adapter Type Protocol	RO	0Eh		0E
		31:24	Reserved	Rsvd	01h		01h
3	ADP_CS_3	19:0	Reserved	Rsvd	0		0
		25:20	Adapter Number	RO	Vendor Defined		VD
		28:26	Reserved	Rsvd	0		0
		29	HEC Error (HE)	R/Clr	0		0
		30	Flow Control Error (FCE)	R/Clr	0		0
		31	Shared Buffering Capable (SBC)	RO	Vendor Defined		VD
4	ADP_CS_4	9:0	Non-Flow Controlled Buffers	R/W	Vendor Defined		VD
		19:10	Reserved	Rsvd	0		0
		29:20	Total Buffers	RO	Vendor Defined		VD
		30	Plugged	RO	0		0
		31	Lock (LCK)	R/W	0		0
5	ADP_CS_5	10:0	Max Input HopID	RO	Vendor Defined		VD
		21:11	Max Output HopID	R/W	Vendor Defined		VD

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	Paired
		28:22	Link Credits Allocated	R/W	0	
		29	HEC Error Enable (HEE)	R/W	0	
		30	Flow Control Error Enable (FCEE)	R/W	0	
		31	Disable Hot Plug Events (DHP)	R/W	0	
6	ADP_CS_6	31:0	HEC Errors	W/Clr	0	
7	ADP_CS_7	31:0	Invalid HopID Errors	W/Clr	0	0
8	ADP_CS_8	31:0	ECC Errors	W/Clr	0	0

Table 2 – DP IN Adapter Configuration Capability Fields

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After Paired
0	ADP_DP_CS_0	7:0	Next Capability pointer	RO	Vendor Defined	VD
		15:8	Capability ID	RO	04h	04h
		26:16	Video HopID	RO	9	9h
		29:27	Reserved	Rsvd	0	0
		30	AUX enable (AE)	R/W	0	1
		31	Video Enable (VE)	R/W	0	1
1	ADP_DP_CS_1	10:0	AUX Tx HopID	RO	8	8
		21:11	AUX Rx HopID	RO	8	8
		31:22	Reserved	Rsvd	0	0
2	ADP_DP_CS_2	2:0	Reserved No_red Maximal Lane Count Similar to remote without BW reeducation by CM	Rsvd RW	0	0
		3	SW Link Init (SWLI)	R/W	0	0
		5:4	Reserved	RsvdZ	0	0
		6	HPD Status	RO	0	1

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After Paired
		31:7	Reserved	RW	0	0
		9:7	No red Maximal Link Rate Similar to remote without BW reeducation by CM			0
		10	Ack bits	R/W	0	0
		12:11	Granularity	R/W	0	0
		15:13	Group_ID	R/W	0	0
		19:16	CM_ID	R/W	0	0
		20	CM Mode support	R/W	0	0
		23:21	Reserved	Rsvd	0	0
		31:24	Estimate BW	R/W	0	0
3	ADP_DP_CS_3	8:0	Vendor Defined	VD	Vendor Defined	VD
		9	HPD Output Clear (HPDC)	R/W	0	0
		10	HPD Output Set (HPDS)	R/W	0	0
		31:11	Vendor Defined	VD	Vendor Defined	VD
4	DP_LOCAL_CAP	3:0	Protocol Adapter Version	RO	4	4
		7:4	Maximal DPCD Rev	RO	3	3
		11:8	Maximal Link Rate	RO	Vendor Defined	VD
		14:12	Maximal Lane Count	RO	Vendor Defined	VD
		15	MST Capability	RO	Vendor Defined	VD
		21:16	Reserved	Rsvd	0	0
		22	TPS3 Capability	RO	Vendor Defined	VD
		23	Reserved	Rsvd	1	1
		24	TPS4 Capability	RO	Vendor Defined	VD
		25	FEC Not Supported	RO	Vendor Defined	VD
		26	Secondary Split Capability	RO	Vendor Defined	VD

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After Paired
		27	LTTPR Not Supported	RO	Vendor Defined	VD
		28	Reserved	Rsvd	0	0
		29	DSC Not Supported	RO	Vendor Defined	VD
		31:30	Reserved	Rsvd	0	0
5	DP_REMOTE_CAP	3:0	Protocol Adapter Version	R/W	0	4
		7:4	Maximal DPCD Rev	R/W	0	3
		11:8	Maximal Link Rate	R/W	0	3
		14:12	Maximal Lane Count	R/W	0	2
		15	MST Capability	R/W	0	1
		21:16	Reserved	RsvdZ	0	0
		22	TPS3 Capability	R/W	0	1
		23	Reserved	VD	VD	VD
		24	TPS4 Capability	R/W	0	1
		25	FEC Not Supported	R/W	0	0
		26	Secondary Split Capability	R/W	0	1
		27	LTTPR Not Supported	R/W	0	0
		28	Reserved	RsvdZ	0	0
		29	DSC Not Supported	RO	0	0
		31:30	Reserved	RsvdZ	0	0
6	DP_STATUS	2:0	Lane Count	RO	0	NA (debug)
		7:3	Reserved	Rsvd	0	0
		11:8	Link Rate	RO	0	NA (debug)
		23:12	Reserved	Rsvd	0	0
		31:24	Allocate BW	R/W	0	0
7	DP_COMMON_CAP	3:0	Protocol Adapter Version	RO	0	4

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After Paired
		7:4	Maximal DPCD Rev	RO	0	3
		11:8	Maximal Link Rate	RO	0	= DP_Local_cap11:8
		14:12	Maximal Lane Count	RO	0	= DP_Local_cap14:12
		15	MST Capability	RO	0	= DP_Local_cap 15
		21:16	Reserved	Rsvd	0	0
		22	TPS3 Capability	RO	0	= DP_Local_cap 22
		23	Reserved	VD	VD	VD
		24	TPS4 Capability	RO	0	= DP_Local_cap 24
		25	FEC Not Supported	RO	0	= DP_Local_cap 25
		26	Secondary Split Capability	RO	0	= DP_Local_cap 26
		27	LTTPR Not Supported	RO	0	= DP_Local_cap 27
		28	Reserved	Rsvd	0	0
		29	DSC Not Supported	RO	0	= DP_Local_cap 29
		30	Reserved	Rsvd	0	0
		31	DPRX Capabilities Read Done	RO	0	1 within 5 Sec after Tunnel pair
8	ADP_DP_CS_8	31:0	Reserved	Rsvd	0	0
		7:0	Request/consume BW (uC address 0x24)	RO	0	0
		29:8	Reserved	Rsvd	0	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After Paired
		30	Mode Set Indicate GPU mode support (uC address 0x27 bit 6)	RO	0	0
		31	Request bit (uC address 0x27 bit 7)	RO	0	0

TD 10.002 DP IN Adapter DP CTS LL Test TD_DP IN_2

Note: This test does not use USB4 CV. It can be run with any software-based Connection Manager.

A. Purpose:

- Verify that the DP IN Adapter passes the compliance tests defined in the DP Link CTS

B. Asserts:

- 10#1
- 10#2
- 10.1.3#1

C. Setup:

- AN_HOST_DFP1—DPIN_01
- AN_DEV_UFP1—DPIN_03
- AN_HUB_UFP1—DPIN_05

D. Procedure:

- For AN_HOST_DFP1—DPIN_01 setup
    - The DP Link Layers tests to be executed are the ones marked as ‘Yes’ in the “DP Tunneling Subset” column for Source Testing in Table 5 to Table 9.
- For AN_DEV_UFP1—DPIN_03 setup
    - The DP Link Layers tests for Source Testing that are defined in Table 5 to Table 9 are executed. If the only method to utilize the DPTX is through DP Tunneling, then the executed tests are the ones marked as ‘Yes’ in the “DP Tunneling Only” column, otherwise the executed tests are the ones marked as ‘Yes’ in the “DP Tunneling Subset” column.

USB4 CV performs the following steps:

Part 1 – Source Device Services Test Procedures

1. Connect test setup
2. Run the tests in Table 5
3. Follow plug/unplug for pair/teardown the tunnel
4. Verify that the UUT passes all of the tests in Table 5

Part 2 – Source Device Link Services Test Procedures

5. Connect test setup
6. Run the tests in Table 6
7. Follow plug/unplug for pair/teardown the tunnel
8. Verify that the UUT passes all of the tests in Table 6

Part 3 – USB4 DP CTS Source Isochronous Transport Services Test Procedures

9. Connect test setup
10. Run the tests in Table 7
11. Follow plug/unplug for pair/teardown the tunnel
12. Verify that the UUT passes all of the tests in Table 7

Part 4 – USB4 DP CTS Source Devices FEC Test Procedures

13. Connect test setup
14. Run the tests in Table 8
15. Follow plug/unplug for pair/teardown the tunnel
16. Verify that the UUT passes all of the tests in Table 8

Part 5 – USB4 DP CTS Source Devices DSC Test Procedures

17. Connect test setup
18. Run the tests in Table 9
19. Follow plug/unplug for pair/teardown the tunnel
20. Verify that the UUT passes all of the tests in Table 9
    a. Run 4.6.1.3 with format 2k@120Hz, Reduced Blanking 2 (rb2)
    b. Run 4.6.1.3 with format 5k@30Hz, Reduced Blanking 1 (rb1)
    c. Run 4.6.1.7 with format 2k@30Hz, CTA

TD 10.003 DP IN Adapter LTTPR Test TD_DP IN_3

A. Purpose:

- Verify that the DP IN Adapter works in both LTTPR and Non-LTTPR modes

B. Asserts:

- TBD

C. Setup:

- AN_HOST_DFP1—DPIN_01
- AN_DEV_UFP1—DPIN_03
- AN_HUB_UFP1—DPIN_05

D. Procedure:

USB4 CV performs the following steps:

Part 1 – LTTPR Transparent/Non-Transparent Mode with Max Supported Lanes and Speed

1. Connect test setup
2. Configure the DP Reference Source to run LT with LTTPR functionality
3. Parse the AUX log at the DP Reference Sink in the Device Router and verify use of DPCD LTTPR as follows:
    a. Read of DPCD LTTPR Capability and ID (F0000h – F000Fh)
    b. If DPTX write F0003h PHY_REPEATER_MODE = AAh Non-transparent mode continue as non-transparent below:
        i. Write of DPCD LTTPR TRAINING_PATTERN_SET_PHY_REPEATER1 F0010h
        ii. Read of DPCD LTTPR TRAINING_AUX_RD_INTERVAL_PHY_REPEATER1 F0020h
        iii. Read of LTTPR LT status:
            a. LANE0_1_STATUS_PHY_REPEATER1 F0030h
            b. LANE2_3_STATUS_PHY_REPEATER1 F0031h
            c. LANE_ALIGN_STATUS_UPDATED_PHY_REPEATER1 F0032h
    c. Else if DPTX, keep F0003h PHY_REPEATER_MODE = 55h transparent mode continue as transparent below:
        i. Parse the AUX Log at the DP Reference Sink in the Device Router and verify LTTPR transparent functionality as follows:
            a. LT done by DPCD register 102h-107h, 202h-207h
            b. From writing DPCD 102h=0x01 till 102h=0x00 no access to any other DPCD register beside LT DPCD registers
        ii. Verify that the picture on the screen is stable

Part 2 – LTTPR Non-Transparent Mode with 2 Lanes and HBR Speed

4. Limit DP IN Adapter as follows:
    a. Read DP_LOCAL_CAP from DP OUT Adapter and record the values
    b. Set bits 14:12 to 001b (2 lanes) in the DP_LOCAL_CAP values read from the DP OUT Adapter
    c. Set bits 11:8 to 0001b (HBR) in the DP_LOCAL_CAP values read from the DP OUT Adapter
5. Copy the DP_LOCAL_CAP values (with bits 14:8 change) to the DP_REMOTE_CAP register in the DP IN Adapter
6. Connect the test setup
7. Configure DP Reference Source to run LT with LTTPR functionality
8. Parse the AUX Log at the DP Reference Sink in the Device Router use DPCD LTTPR as follows:
    a. Read of DPCD LTTPR Capability and ID
    b. If DPTX write F00003h PHY_REPEATER_MODE = AAh Non-transparent mode continue as non-transparent below:
        i. Write of DPCD LTTPR TRAINING_PATTERN_SET_PHY_REPEATER1 F0010h.
        ii. Read of DPCD LTTPR TRAINING_AUX_RD_INTERVAL_PHY_REPEATER1 F0020h.
        iii. Read of LTTPR LT status:
            a. LANE0_1_STATUS_PHY_REPEATER1 F0030h
            b. LANE2_3_STATUS_PHY_REPEATER1 F0031h
            c. LANE_ALIGN_STATUS_UPDATED_PHY_REPEATER1 F0032h
    c. Else if DPTX keep F00003h PHY_REPEATER_MODE = 55h transparent mode continue as transparent below:
        i. Parse the AUX Log at the DP Reference Sink in the Device Router and verify LTTPR transparent functionality as follows:
            a. No access to any DPCD LTTPR register besides LTTPR capability
            b. LT done by DPCD register 102h-107h, 202h-207h
            c. From writing DPCD 102h=0x01 till 102h=0x00 no access to any other DPCD register beside LT DPCD registers
        ii. Verify that the picture on the screen is stable with HBR and 2 lanes maximum

TD 10.004 DP IN Adapter MST Test TD_DP IN_4

A. Purpose:

- Verify DP IN Adapter DP MST functionality (if supported)

B. Asserts:

- TBD

C. Setup:

- AN_HOST_DFP1—DPIN_01
- AN_DEV_UFP1—DPIN_03
- AN_HUB_UFP1—DPIN_05

D. Repetitions:

- At each iteration repeat ‘Part 1’ - Configure the DP Reference Sink as MST with the following parameters:
  - Link: HBR2 x 4 Lanes ; Monitors: Two FHD (1080p)
  - Link: HBR3 x 4 Lanes ; Monitors: Two 4K 8 pbc
  - Link: HBR2 x 2 Lanes ; Monitors: One FHD (1080p)
  - Link: RBR x 4 Lanes ; Monitors: One FHD (1080p)
  - Link: HBR3 x 1 Lane ; Monitors: One FHD (1080p)

E. Procedure:

USB4 CV performs the following steps:

Part 1 – MST Check

1. Configure the DP Reference Sink as MST with the maximal Lane Count and Link Rate according to the iteration parameters.
2. Configure the DP Reference Sink to support the Monitors according to the iteration.
3. Verify that the streams were activated and are stable over the DP Reference Sink
4. For the cases of two monitors, Configure the Reference Sink to disconnect one of the monitors and verify that the other stream is stable over the DP Reference Sink.

Part 2 – Disable MST

5. Keep Reference Sink configured to the last iteration parameters and monitors
6. Tear down the DP Paths
7. While setting up the DP Path, disable MST function as follows:
   a. Read DP_LOCAL_CAP from DP OUT Adapter and record the values
   b. Set bits 15 to 0b (disable MST) in the DP_LOCAL_CAP values read from the DP OUT Adapter
   c. Copy the DP_LOCAL_CAP values (with bits 15 set to 0b) to the DP_REMOTE_CAP register in the DP IN Adapter
8. Verify that the DP IN Adapter and DP OUT Adapter pair without MST functionality

TD 10.005 DP IN Sink Count TD_DP IN_5

A. Purpose:

- Verify that the DP IN Adapter correctly follows sink_count

B. Asserts:

- 10.4.6.3#1
- 10.4.6.3#2

C. Setup:

- AN_HOST_DFP1—DPIN_02
- AN_DEV_UFP1—DPIN_04
- AN_HUB_UFP1—DPIN_06

D. Procedure:

USB4 CV performs the following steps:

Part 1 – Teardown Tunnel upon Sink Count Equal 0

1. Connect test setup without the monitor
2. Verify that DP IN Adapter and DP OUT Adapter are paired and Path is set up
3. Wait for the DP Reference Source to read DPCD 00200h with value 0
4. Verify that the path is torn down after reading the 0 value from DPCD 00200h

Part 2 – Pair upon Monitor Connect to DP Dongle

5. Connect the monitor to DP dongle
6. Wait for the HPD IRQ from the monitor connection
7. Verify that the picture on the monitor is stable

Part 3 – Teardown Tunnel when Sink Count Goes to 0

8. Disconnect the monitor from the DP dongle
9. Wait for DP Reference Source get HPD_IRQ and read DPCD 00200h with value 0
10. Verify that path is torn down immediately after reading the 0 value from DPCD 00200h

TD 10.006 DP IN MFDP TD_DP IN_6

A. Purpose:

- Verify that the DP IN Adapter reduces the number of lanes to 2 with MFDP

B. Asserts:

- TBD

C. Setup:

- AN_HOST_DFP1—DPIN_02
- AN_DEV_UFP1—DPIN_04
- AN_HUB_UFP1—DPIN_06

Note: DP LSPCON is a Multi-Function DP Dongle

D. Procedure:

USB4 CV performs the following steps:

Part 1 – Reduce Lanes to 2 with MFDP

1. Connect test setup
2. Verify that the DP IN Adapter and DP OUT Adapter are paired and Path is set up between them
3. Verify that the DP IN Adapter sends SET_CONFIG Packet of type SET_MFDP with *MFDP Enable* bit set to 0b.
4. Verify that the number of lanes is 2 by reading DP_STATUS.*Lane Count* (bits 2:0) in both DP Adapters. Value is set to 2h.
5. Verify that the picture on the monitor is stable

TD 10.007 Tunnel Specific DPCD Register TD_DP IN_7

A. Purpose:

- Verify that the DP IN Adapter reply to tunnel specific DPCD registers

B. Asserts:

- TBD

C. Setup:

- AN_HOST_DFP1—DPIN_01
- AN_DEV_UFP1—DPIN_03
- AN_HUB_UFP1—DPIN_05

D. Procedure:

USB4 CV performs the following steps:

6. Connect test setup
7. Verify that the picture on the monitor is stable
8. DP Reference Source reads DPCD 0xE0000 to 0xE000F and verifies the followings values:
    a. 0xE0002 – 0xE0000 IEEE_OUI = non zero
    b. 0xE0008 – 0xE0003 Device Identification String – non zero
    c. 0xE0009 – Hardware Revision – non zero
    d. 0xE000A – Firmware Major Revision – non Zero
    e. 0xE000B - Firmware Minor Revision – Don’t care
    f. 0xE000D – DP Tunneling and Panel Replay – Bit 0 must be set, all other shall be clear for this version.
    g. 0xE000E – 0xE000F – reserved read with value 0

TD 10.008 DP IN Adapter with HDCP TD_DP IN_8

A. Purpose:

- Verify that the DP IN Adapter passes DP HDCP CTS tests (if supported)

B. Asserts:

- TBD

C. Setup:

- AN_HOST_DFP1—DPIN_01
- AN_DEV_UFP1—DPIN_03
- AN_HUB_UFP1—DPIN_05

D. Procedure:

USB4 CV performs the following steps:

Part 1 – USB4 DP CTS HDCP Downstream Procedure with Receiver

1. Connect the setup
2. Run the tests 1A-XX Source Device HDCP Downstream procedure with Receiver define in HDCP CTS for DP reference above
3. Follow plug/unplug for pair/teardown the tunnel
4. Verify that the UUT passes all tests

Part 2 – USB4 DP CTS HDCP Downstream Procedure with Repeater

5. Connect the setup
6. Run the tests 1B-XX Source Device HDCP Downstream Procedure with Repeater define in HDCP CTS for DP reference above
7. Follow plug/unplug for pair/teardown the tunnel
8. Verify that the UUT passes all of the tests

DP OUT Adapter tests

TD 10.009 DP OUT Adapter Configuration Capability TD_DP OUT_1

A. Purpose:

- Verify that a DP OUT Adapter contains the correct values in the Adapter Configuration Space Basic and DP Configuration Capability

B. Asserts:

- 10.2.1#1
- 10.2.2#1
- 10.3.2.2#1
- 10.4.2.1#5
- 10.4.2.2#1
- 10.4.6.3#4
- 10.4.6.3#5
- 10.4.6.3#6

C. Setup:

- AN_HOST_DFP1—DPOUT_01
- AN_DEV_UFP1—DPOUT_02
- AN_DEV_UFP1—DPOUT_04
- AN_HUB_UFP1—DPOUT_06
- AN_HUB_UFP1—DPOUT_08

D. Procedure:

USB4 CV performs the following steps:

Part 1 – Verify Default Values

1. Connect the test setup. For AN_DEV_UFP1—DPOUT_02 do not connect the DP Reference Sink
2. Read the Adapter Configuration Space of the DP OUT Adapter on the UUT
3. Verify that the Basic Attributes have the values in Table 3
4. Verify that the DP Configuration Capability has the values in Table 4
5. For AN_DEV_UFP1—DPOUT_02, connect the DP Reference Sink to the DP OUT Adapter in the UUT
6. Configure DP path, after UUT sends a Hot Plug Event Packet for the DP OUT Adapter after detecting the connection, according to Universal Serial Bus 4 (USB4™) Connection Manager Guide section 5.4.
7. It is a test failure if the DPRX capabilities Read Done bit is not 1b within 5 sec.
8. Read the Adapter Configuration Space of the DP OUT Adapter on the UUT
9. Verify that the Basic Attributes has the values in Table 3
10. Verify that the DP Configuration Capability has the values in Table 4

Part 2 – USB4 Verify Specific Configuration Bits

11. Wait for the DP link to be stable

12. Set the SWLI bit to 1b in the DP OUT Adapter in the UUT
13. Verify that Link training was Re-initiated.
14. Wait for the DP link to be stable

Part 3 – Verify Default Values After Path Teardown

15. For AN_DEV_UFP1—DPOUT_02:
    a. Disconnect the DP Reference Sink from the KG Device Router
    b. After receiving a Hot Unplug Event Packet from the DP OUT Adapter continue to the next step
16. Tear down the DP Path as described in Section 5.4 of the Universal Serial Bus 4 (USB4™) Connection Manager Guide
17. Read the Adapter Configuration Space of the DP OUT Adapter in the UUT
18. Verify the that the Basic Attributes have the values described in Table 3
19. Verify that the DP Configuration Capability has the values described in Table 4

Table 3 – Adapter Configuration Space Basic Attributes

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value		Paired
0	ADP_CS_0	31:0	Vendor Defined	VD	Vendor Defined		VD
1	ADP_CS_1	7:0	Next Capability Pointer	RO	Vendor Defined		VD
		18:8	Max Counter Sets	RO	Vendor Defined		VD
		19	Counters Configuration Space (CCS) Flag	RO	Vendor Defined		VD
		31:20	Reserved	Rsvd	0		0
2	ADP_CS_2	7:0	Adapter Type Sub-type	RO	IN 01h	OUT 02h	01/02
		15:8	Adapter Type Version	RO	01h		01
		23:16	Adapter Type Protocol	RO	0Eh		0E
		31:24	Reserved	Rsvd	01h		01h
3	ADP_CS_3	19:0	Reserved	Rsvd	0		0
		25:20	Adapter Number	RO	Vendor Defined		VD
		28:26	Reserved	Rsvd	0		0
		29	HEC Error (HE)	R/Clr	0		0
		30	Flow Control Error (FCE)	R/Clr	0		0
		31	Shared Buffering Capable (SBC)	RO	Vendor Defined		VD
4	ADP_CS_4	9:0	Non-Flow Controlled Buffers	R/W	Vendor Defined		VD
		19:10	Reserved	Rsvd	0		0
		29:20	Total Buffers	RO	Vendor Defined		VD
		30	Plugged	RO	0		1
		31	Lock (LCK)	R/W	0		0
5	ADP_CS_5	10:0	Max Input HopID	RO	Vendor Defined		VD
		21:11	Max Output HopID	R/W	Vendor Defined		VD

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	Paired
		28:22	Link Credits Allocated	R/W	0	
		29	HEC Error Enable (HEE)	R/W	0	
		30	Flow Control Error Enable (FCEE)	R/W	0	
		31	Disable Hot Plug Events (DHP)	R/W	0	
6	ADP_CS_6	31:0	HEC Errors	W/Clr	0	
7	ADP_CS_7	31:0	Invalid HopID Errors	W/Clr	0	0
8	ADP_CS_8	31:0	ECC Errors	W/Clr	0	0

Table 4 – DP OUT Adapter Configuration Capability Fields

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After paired
0	ADP_DP_CS_0	7:0	Next Capability pointer	RO	Vendor Defined	VD
		15:8	Capability ID	RO	04h	04h
		26:16	Video HopID	RO	9	09h
		29:27	Reserved	Rsvd	0	0
		30	AUX enable (AE)	R/W	0	1
		31	Video Enable (VE)	R/W	0	1
1	ADP_DP_CS_1	10:0	AUX Tx HopID	RO	8	8
		21:11	AUX Rx HopID	RO	8	8
		31:22	Reserved	Rsvd	0	0
2	ADP_DP_CS_2	2:0	Reserved	Rsvd	0	0
		3	SW Link Init (SWLI)	R/W	0	0
		5:4	Reserved	RsvdZ	0	0
		6	HPD Status	RO	0	1

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After paired
		7	Reserved	Rsvd	0	0
		23:8	Maximum Accumulation Cycles	RO	Vendor Defined	VD
		31:24	Reserved	Rsvd	0	0
3	ADP_DP_CS_3	31:0	Vendor Defined	VD	Vendor Defined	VD
4	DP_LOCAL_CAP	3:0	Protocol Adapter Version	RO	4	4
		7:4	Maximal DPCD Rev	RO	Vendor Defined	VD
		11:8	Maximal Link Rate	RO	Vendor Defined	VD
		14:12	Maximal Lane Count	RO	Vendor Defined	VD
		15	MST Capability	RO	Vendor Defined	VD
		21:16	Reserved	Rsvd	0	0
		22	TPS3 Capability	RO	Vendor Defined	VD
		23	Reserved	Rsvd	1	1
		24	TPS4 Capability	RO	Vendor Defined	VD
		25	FEC Not Supported	RO	Vendor Defined	VD
		26	Secondary Split Capability	RO	Vendor Defined	VD
		27	LTTPR Not Supported	RO	Vendor Defined	VD
		28	Reserved	Rsvd	0	0
		29	DSC Not Supported	RO	Vendor Defined	VD
		31:30	Reserved	Rsvd	0	0
5	DP_REMOTE_CAP	3:0	Protocol Adapter Version	R/W	0	4
		7:4	Maximal DPCD Rev	R/W	0	3
		11:8	Maximal Link Rate	R/W	0	3
		14:12	Maximal Lane Count	R/W	0	2
		15	MST Capability	R/W	0	1

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After paired
		21:16	Reserved	RsvdZ	0	0
		22	TPS3 Capability	R/W	0	1
		23	Reserved	VD	VD	VD
		24	TPS4 Capability	R/W	0	1
		25	FEC Not Supported	R/W	0	0
		26	Secondary Split Capability	R/W	0	1
		27	LTTPR Not Supported	R/W	0	0
		28	Reserved	RsvdZ	0	0
		29	DSC Not Supported	RO	0	0
		31:30	Reserved	RsvdZ	0	0
6	DP_STATUS	2:0	Lane Count	RO	0	NA (Debug)
		7:3	Reserved	Rsvd	0	0
		11:8	Link Rate	RO	0	NA (Debug)
		24:12	Reserved	Rsvd	0	0
		25	CM Handshake (CMHS)	R/W	0	0
		26	DP IN Adapter USB4 Flag (UF)	R/W	0	1
		31:27	Reserved	Rsvd	0	0
7	DP_COMMON_CAP	3:0	Protocol Adapter Version	RO	0	4
		7:4	Maximal DPCD Rev	RO	0	3
		11:8	Maximal Link Rate	RO	0	= DP_Local
		14:12	Maximal Lane Count	RO	0	= DP_Local
		15	MST Capability	RO	0	= DP_Local
		21:16	Reserved	Rsvd	0	0
		22	TPS3 Capability	RO	0	= DP_Local
		23	Reserved	VD	VD	VD

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After paired
		24	TPS4 Capability	RO	0	= DP_Local
		25	FEC Not Supported	RO	0	= DP_Local
		26	Secondary Split Capability	RO	0	= DP_Local
		27	LTTPR Not Supported	RO	0	= DP_Local
		28	Reserved	Rsvd	0	0
		29	DSC Not Supported	RO	0	= DP_Local
		31:30	Reserved	Rsvd	0	0
8	ADP_DP_CS_8	31:0	Reserved	Rsvd	0	0

TD 10.010 DP OUT Adapter DP CTS LL Test TD_DP OUT_2

Note: This test does not use USB4 CV. It can be run with any software-based Connection Manager.

A. Purpose:

- Verify that the DP OUT Adapter passes the compliance tests defined in the DP Link CTS

B. Asserts:

- 10#3
- 10#4
- 10.1.3#1

C. Setup:

- AN_HOST_DFP1—DPOUT_01
- AN_DEV_UFP1—DPOUT_02
- AN_DEV_UFP1—DPOUT_04
- AN_DEV_UFP1—DPOUT_05
- AN_HUB_UFP1—DPOUT_06
- AN_HUB_UFP1—DPOUT_08
- AN_HUB_UFP1—DPOUT_09

D. Procedure:

- For a DP OUT Adapter with an exposed connector, both of the below setups shall be executed:
  - AN_DEV_UFP1—DPOUT_02 setup
    - The DP Link Layers tests to be executed are the ones marked as ‘Yes’ in the “DP OUT Adapter UUT” column for Source Testing in Table-5 to Table-9.
  - AN_DEV_UFP1—DPOUT_05 setup
    - The DP Link Layers tests to be executed are the ones marked as ‘Yes’ in the “DP Tunneling only” column for Sink Testing in Table-12.
    - The LTTPR tests to be executed are the ones marked as ‘Yes’ in the “Tested” column for LTTPR Testing in Table-15

- For the AN_DEV_UFP1—DPOUT_04 & AN_HOST_DFP1—DPOUT_01 setups
  - The DP Link Layers tests for Sink Testing that are defined in Table-10 to Table-14 are executed. If the only method to utilize the DPRX is through DP Tunneling, then the executed tests are the ones marked as ‘Yes’ in the “DP Tunneling Only” column, otherwise the executed tests are the ones marked as ‘Yes’ in the “DP Tunneling Subset” column.

USB4 CV performs the following steps:

Part 1 – Device Services Test Procedures

1. Connect test setup
2. Run the tests in Table 5/Table 10
3. Follow plug/unplug for pair/teardown the tunnel
4. Verify that the UUT passes all of the tests in Table 5/Table 10

Part 2 – Device Link Services Test Procedures

5. Connect test setup
6. Run the tests in Table 6/Table 11
7. Follow plug/unplug for pair/teardown the tunnel
8. Verify that the UUT passes all of the tests in Table 6/Table 11

Part 3 – USB4 DP CTS Isochronous Transport Services Test Procedures

9. Connect test setup
10. Run the tests in Table 7/Table 12
11. Follow plug/unplug for pair/teardown the tunnel
12. Verify that the UUT passes all of the tests in Table 7/Table 12

Part 4 – USB4 DP CTS Devices FEC Test Procedures

13. Connect test setup
14. Run the tests in Table 8/Table 13
15. Follow plug/unplug for pair/teardown the tunnel
16. Verify that the UUT passes all of the tests in Table 8/Table 13

Part 5 – USB4 DP CTS Devices DSC Test Procedures

17. Connect test setup
18. Run the tests in Table 9/Table 14
19. Follow plug/unplug for pair/teardown the tunnel
20. Verify that the UUT passes all of the tests in Table 9/Table 14

Part 6 – Sink Device Embedded LTTPR Test Procedures (For AN_DEV_UFP1—DPOUT_05 setup only)

21. Connect test setup
22. Run the tests in Table 15
23. Follow plug/unplug for pair/teardown the tunnel
24. Verify that the UUT passes all of the tests in Table 15

TD 10.011 DP OUT Adapter LTTPR test TD_DP OUT_3

A. Purpose:

- Verify that the DP OUT Adapter works in both LTTPR and Non-LTTPR modes

B. Asserts:

- TBD

C. Setup:

- AN_DEV_UFP1—DPOUT_02
- AN_HUB_UFP1—DPOUT_06

D. Procedure:

USB4 CV performs the following steps:

Part 1 – LTTPR Transparent/Non-Transparent Mode with Max Support Lanes and Speed

1. Connect test setup
2. Configure the DP Reference Source to run LT with LTTPR functionality
3. Parse the AUX Log at the DP Reference Sink in the UUT device and verify use of DPCD LTTPR as follows:
    a. Read of DPCD LTTPR Capability and ID (F0000h – F000Fh)
    b. If DPTX write F0003h PHY_REPEATER_MODE = AAh Non-transparent mode, continue as non-transparent below:
        i. Write of DPCD LTTPR TRAINING_PATTERN_SET_PHY_REPEATER1 F0010h
        ii. Write of DPCD LTTPR TRAINING_LANEx_SET_PHY_REPEATER1 F0011h-F0014h
        iii. Read of DPCD LTTPR TRAINING_AUX_RD_INTERVAL_PHY_REPEATER1 F0020h
        iv. Read of LTTPR LT status:
            a. LANE0_1_STATUS_PHY_REPEATER1 F0030h
            b. LANE2_3_STATUS_PHY_REPEATER1 F0031h
            c. LANE_ALIGN_STATUS_UPDATED_PHY_REPEATER1 F0032h
    c. Else, if DPTX keep F0003h PHY_REPEATER_MODE = 55h transparent mode, continue as transparent below:
        i. Parse the AUX Log at the DP Reference Sink in the Device Router and verify LTTPR transparent functionality as follows:
            a. No access to any DPCD LTTPR register besides LTTPR capability
            b. LT done by DPCD register 102h-106h, 202h-207h
            c. From writing DPCD 102h=0x01 till 102h=0x00 no access to any other DPCD register beside LT DPCD registers
        ii. Verify that the Picture on screen is stable

Part 2 – LTTPR Mode with 2 Lanes and HBR Speed

4. Configure the DP IN Adapter as follows:
    a. Set bits 14:12 in the DP_LOCAL_CAP register to 001b (2 Lanes)
    b. Set bits 11:8 in the DP_LOCAL_CAP register to 0001b (HBR)
5. Connect test setup
6. Configure the DP Reference Source to run LT with LTTPR functionality
7. Parse the AUX Log at the DP Reference Sink in the UUT device and verify use of DPCD LTTPR as follows:
    a. Read of DPCD LTTPR Capability and ID
    b. If DPTX write F0003h PHY_REPEATER_MODE = AAh Non-transparent mode continue as non-transparent below:
        i. Write of DPCD LTTPR TRAINING_PATTERN_SET_PHY_REPEATER1 F0010h
        ii. Read of DPCD LTTPR TRAINING_AUX_RD_INTERVAL_PHY_REPEATER1 F0020h
        iii. Read of LTTPR LT status:
            a. LANE0_1_STATUS_PHY_REPEATER1 F0030h
            b. LANE2_3_STATUS_PHY_REPEATER1 F0031h
            c. LANE_ALIGN_STATUS_UPDATED_PHY_REPEATER1 F0032h
    c. Else if DPTX, keep F0003h PHY_REPEATER_MODE = 55h transparent mode continue as transparent below:
        i. Parse the AUX Log at the DP Reference Sink in the Device Router and verify LTTPR transparent functionality as follows:
            a. LT done by DPCD register 102h-107h, 202h-207h
            b. From writing DPCD 102h=0x01 till 102h=0x00 no access to any other DPCD register beside LT DPCD registers
        ii. Verify that the Picture on screen is stable with HBR and 2 lanes maximum.

TD 10.012 DP OUT Adapter MST Test TD_DP OUT_4

A. Purpose:

- Verify DP OUT Adapter DP MST functionality (if supported)

B. Asserts:

- TBD

C. Setup:

- AN_DEV_UFP1—DPOUT_02
- AN_HUB_UFP1—DPOUT_06

D. Repetitions:

- At each iteration Configure the DP Reference Sink as MST with the following parameters:
  - Link: HBR2 x 4 Lanes ; Monitors: Two FHD (1080p)
  - Link: HBR3 x 4 Lanes ; Monitors: Two 4K 8 pbc
  - Link: HBR2 x 2 Lanes ; Monitors: One FHD (1080p)
  - Link: RBR x 4 Lanes ; Monitors: One FHD (1080p)
  - Link: HBR3 x 1 Lane ; Monitors: One FHD (1080p)

E. Procedure:

USB4 CV performs the following steps:

1. Configure the DP Reference Sink as MST with the maximal Lane Count and Link Rate according to the iteration parameters
2. Configure the DP Reference Sink to support the Monitors according to the iteration.
3. Verify that the streams were activated and are stable over the DP Reference Sink
4. For the cases of two monitors, configure the Reference Sink to disconnect one of the monitors and verify that the other stream is stable over the DP Reference Sink.

TD 10.013 DP OUT Sink count TD_DP OUT_5

A. Purpose:

- Verify that the DP OUT Adapter correctly follows sink_count

B. Asserts:

- 10.4.6.3#3
- 10.4.6.3#4
- 10.4.6.3#5
- 10.4.6.3#6

C. Setup:

- AN_DEV_UFP1—DPOUT_03
- AN_HUB_UFP1—DPOUT_07

D. Procedure:

USB4 CV performs the following steps:

Part 1 – Teardown Tunnel upon Sink Count Equal 0

1. Connect the setup without the monitor
2. Verify that the DP IN Adapter and the DP OUT Adapter are paired and a Path is set up
3. Wait for the GPU to read DPCD 00200h with value 0
4. Verify that the Path is torn down after reading the 0 value from DPCD 00200h

Part 2 – Pair upon Monitor Connect to Dongle

5. Connect monitor to the DP dongle
6. Wait for HPD IRQ from Monitor connection
7. Verify that the picture on the monitor is stable

Part 3 – Teardown Tunnel when Sink Count Goes to 0

8. Disconnect the monitor from the DP dongle
9. Verify that the path torn down after reading the 0 value from DPCD 00200h

TD 10.014 DP OUT MFDP TD_DP OUT_6

A. Purpose:

- Verify that the DP OUT Adapter reduces number of lanes to 2 with MFDP (if exposed connector is a USB Type-C connector)

B. Asserts:

- TBD

C. Setup:

- AN_DEV_UFP1—DPOUT_03
- AN_HUB_UFP1—DPOUT_07

Note: DP LSPCON is a Multi-Function DP Dongle

D. Procedure:

USB4 CV performs the following steps:

Part 1 – USB4 DP Teardown Tunnel upon Sink Count Equal 0

1. Connect the setup
2. Before setting up the DP Paths, read DP_LOCAL_CAP register from DP OUT Adapter and verify that *Maximal Lane Count* field is set to 1h (2 lanes).
3. Verify that the DP IN Adapter and DP OUT Adapter are paired and Path is set between them
4. Verify that the DP OUT Adapter sends SET_CONFIG Packet of type SET_MFDP with *MFDP Enable* bit set to 1b.
5. Verify that the number of lanes is 2 by reading DP_STATUS.*Lane Count* (bits 2:0) in both DP Adapters. Value is set to 2h.
6. Verify that the picture on the monitor is stable

TD 10.015 DP OUT Adapter with HDCP TD_DP OUT_7

A. Purpose:

- Verify that the DP OUT Adapter pass DP HDCP CTS tests (if supported)

B. Asserts:

- TBD

C. Setup:

- AN_DEV_UFP1—DPOUT_02
- AN_HUB_UFP1—DPOUT_06

D. Procedure:

USB4 CV performs the following steps:

Part 1 – USB4 DP CTS HDCP Downstream Procedure with Receiver

1. Connect the setup
2. Run the tests 1A-XX Source Device HDCP Downstream procedure with Receiver define in HDCP CTS for DP reference above
3. Follow plug/unplug for pair/teardown the tunnel
4. Verify that the UUT passes all tests

Part 2 – USB4 DP CTS HDCP Downstream Procedure with Repeater

5. Connect the setup
6. Run the tests 1B-XX Source Device HDCP Downstream Procedure with Repeater define in HDCP CTS for DP reference above
7. Follow plug/unplug for pair/teardown the tunnel
8. Verify that the UUT passes all of the tests

Part 3 – USB4 DP CTS HDCP Upstream procedure with Transmitter

9. Connect the setup
10. Run the tests 2C-XX Sink Device HDCP Upstream procedure with Transmitter define in HDCP CTS for DP reference above
11. Follow plug/unplug for pair/teardown the tunnel
12. Verify that the UUT passes all of the tests

TBT3-Compatibility Tests

TD 10.016 DP IN Adapter LTTPR Test TD_DP IN_3

A. Purpose:

- Verify that a TBT3-Compatible DP IN Adapter works with DP OUT Adapter that Only Supports Non-LTTPR Mode

B. Asserts:

- TBD

C. Setup:

- TBD

D. Procedure:

USB4 CV performs the following steps:

1. Disable LTTPR functionality as follows:
    a. Read DP_LOCAL_CAP from DP OUT Adapter and record the values
    b. Set bit 27 to 1b in the DP_LOCAL_CAP values read from the DP OUT Adapter
    c. Copy the DP_LOCAL_CAP values (with bit 27 = 1b) to the DP_REMOTE_CAP register in the DP IN Adapter
2. Connect test setup
3. Configure the DP Reference Source to run LT with LTTPR functionality
4. Parse the AUX Log at the DP Reference Sink in the Device Router and verify LTTPR functionality as follows:
    a. Read of DPCD LTTPR Capability and ID (F0000h – F000Fh):
        i. Parse the AUX log at the DP Reference Sink in the Device Router and verify that UUT did not try LT by LTTPR
        ii. No access to any DPCD LTTPR register besides LTTPR capability
        iii. No Access to F0010h-F02FFh
    b. Verify that the picture on the screen is stable

DP CTS Link Layer Tests

Below is the meaning of the tests classifications:

- Yes – The test is required to run as part of the Compliance certification.
- Skipped – The test is not required to run as part of the Compliance certification, but there should not be any technical barrier to execute it over DP Tunneling setup.
- NA – The test cannot be executed over DP Tunneling

Source Testing Tables

- For DP IN Adapter UUT:
    - If the DPTX can be tested in a manner other than DP Tunneling, then the full Source Testing according to VESA CTS shall be used in the alternative manner and the test to run as part of DP Tunneling CTS are the tests which states ‘Yes’ in the “DP Tunneling Subset” column, otherwise the tests to run are the tests which states ‘Yes’ in the “DP Tunneling Only”.
- For DP OUT Adapter UUT:
    - The test to run as part of DP Tunneling CTS are the tests which states ‘Yes’ in the “DP OUT Adapter UUT” column.

Table 5 – DP CTS Source Device Services Test Procedures

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.2.1 AUX Reads after HPD Plug Event				
4.2.1.1	Source DUT Retry on No-Reply During AUX Read after HPD Plug Event	Yes	Yes	Yes
4.2.1.2	Source Retry on Invalid Reply During AUX Read after HPD Plug Event	Skipped	Yes	Yes
4.2.1.3	Source Device HPD Event Pulse Length Test	Skipped	Yes	Yes
4.2.1.4	Source Device IRQ HPD Pulse Length Test	Skipped	Yes	Yes
4.2.1.5	Source Device Inactive HPD / Inactive AUX Test	Skipped	Yes	Yes
4.2.2 EDID and DPCD Reads				
4.2.2.1	DPCD Receiver Capability and EDID Read upon HPD Plug Event	Yes	Yes	Yes
4.2.2.2	DPCD Extended Receiver Capability and EDID Read upon HPD Plug Event	Yes	Yes	Yes
4.2.2.3	EDID Read	Yes	Yes	Yes
4.2.2.4	EDID Read Failure #1: I2C-Over-AUX NACK	Yes	Yes	Skipped
4.2.2.5	EDID Read Failure #2: I2C-Over-AUX DEFER	Yes	Yes	Skipped
4.2.2.6	EDID Corruption Detection	Skipped	Yes	Skipped
4.2.2.7	Branch Device Detection upon HPD Plug Event	Skipped	Yes	Skipped
4.2.2.8	EDID Read on IRQ HPD Event after Branch Device Detection	Yes	Yes	Yes
4.2.2.9	E-DDC Four Block EDID Read	Skipped	Yes	Skipped
4.2.2.10	Link Status/Adjust Request AUX read interval during Link Training	Yes	Yes	Yes

Table 6 – DP CTS Source Device Link Services Test Procedures

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.3.1 Link Training				
4.3.1.1	Successful Link Training at All Supported Lane Counts and Link Speeds	Yes	Yes	Yes
4.3.1.2	Successful Link Training Upon HPD Plug Event	Skipped	Yes	Skipped
4.3.1.3	Successful Link Training with Request of Higher Differential Voltage Swing during Clock Recovery Sequence	Skipped	Yes	Yes
4.3.1.4	Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing	Yes	Yes	Yes
4.3.1.5	Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing	Yes	Skipped	Yes
4.3.1.6	Successful Link Training with Request of a Higher Pre-emphasis Setting during Channel Equalization Sequence	Yes	Skipped	Yes
4.3.1.7	Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock during Channel Equalization Sequence	Yes	Yes	Yes
4.3.1.8	Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing	Yes	Yes	Yes
4.3.1.9	Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing	Yes	Yes	Yes
4.3.1.10	Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5)	Yes	Yes	Yes
4.3.1.11	Successful Link Training with Simultaneous Request for Differential Voltage Swing and Pre-emphasis during Clock Recovery Sequence	Yes	Yes	Yes
4.3.1.12	Source Device Link Training CR Fallback Test	Skipped	Yes	Yes
4.3.1.13	Source Device Link Training EQ Fallback Test	Skipped	Yes	Yes
4.3.2 Link Maintenance				
4.3.2.1	Successful Link Re-training after IRQ_HPD Pulse Due to Loss of Symbol Lock	Yes	Yes	Yes

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.3.2.2	Successful Link Re-training after IRQ_HPD Pulse Due to Loss of Clock Recovery Lock	Yes	Yes	Yes
4.3.2.3	Successful Link Re-training after IRQ_HPD Pulse Due to Loss of Inter-lane Alignment Lock	Yes	Yes	Yes
4.3.2.4	Handling of IRQ_HPD Pulse with No Error Status Bits Set	Skipped	Yes	Skipped
4.3.2.5	Lane Count Reduction	NA	NA	NA
4.3.3 Video Time Stamp Generation				
4.3.3.1	Video Time Stamp Generation	Yes*	Yes*	Yes*

* Not include empty TU: VIC=1 over HBR3*4L, HBR3*2L, HBR2*4L

Table 7 – Source Isochronous Transport Services Test Procedures

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.4.1 Main Stream Data Mapping				
4.4.1.1	Pixel Data Packing and Steering	Yes	Yes	Yes
4.4.1.2	Main Stream Data Packing and Stuffing– Least Packed TU	Yes*	Yes*	Yes
4.4.1.3	Main Stream Data Packing and Stuffing – Most Packed TU	Yes	Yes	Yes
4.4.2	Main Video Stream Format Change Handling	Yes	Yes	Yes
4.4.3	Power Management	NA	NA	NA
4.4.4 Audio Stream Transmission over Secondary Packets				
4.4.4.1	Configuring Video and Audio Parameters	Skipped	Yes*	Skipped
4.4.4.2	Audio Stream Header Synchronization	Skipped	Yes*	Skipped
4.4.4.3	Audio Time Stamp Generation	Yes*	Yes*	Yes
4.4.4.4	Audio INFOFRAME Packet	Skipped	Yes*	Skipped
4.4.4.5	Audio Stream Transmission	Yes*	Yes*	Yes

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.4.4.6	Audio Start Sequence	Skipped	Yes*	Yes

Table 8 – Source Device FEC Test Procedures

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.5.1 Source FEC Protocol				
4.5.1.1	FEC Enable Verification for All Supported Lane Count and Link Speed	Yes	Yes	Yes
4.5.1.2	FEC Ready Verification for Non FEC Capable Sink	Skipped	Yes	Skipped

Table 9 – Source Device DSC Test Procedures

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.6.1 Source DSC Protocol				
4.6.1.1	DSC enable sequence verification	Skipped	Yes	Yes
4.6.1.2	DSC PPS block prediction flag verification	Skipped	Yes	Yes
4.6.1.3	DSC PPS convert RGB flag verification	Yes	Yes	Yes
4.6.1.4	DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification	Skipped	Yes	Yes
4.6.1.5	DSC PPS Simple 4:2:2 flag verification	Skipped	Yes	Yes
4.6.1.6	DSC PPS Native 4:2:2 flag verification	Skipped	Yes	Yes
4.6.1.7	DSC PPS Native 4:2:0 flag verification	Yes	Yes	Yes
4.6.1.8	DSC PPS convert RGB flag verification for DSC Algorithm Revision 1.1	Skipped	Yes	Yes
4.6.1.9	DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification for DSC Algorithm Revision 1.1	Skipped	Yes	Yes

Sink Testing Tables

If the DPRX can be tested in a manner other than DP Tunneling, then the full Sink Testing according to VESA CTS shall be used in the alternative manner and the test to run as part of DP Tunneling CTS are the tests which states 'Yes' in the "DP Tunneling Subset" column, otherwise the tests to run are the tests which states 'Yes' in the "DP Tunneling Only".

Table 10 – DP CTS Sink Device Services Test Procedures

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only
5.2.1 AUX_CH Protocol			
5.2.1.1	Read One Byte from Valid DPCD Address	Skipped	Skipped
5.2.1.2	DPCD Receiver Capability Read (Read 12 Bytes from Valid DPCD Address)	Skipped	Skipped
5.2.1.3	Write One Byte to Valid DPCD Address	Skipped	Skipped
5.2.1.4	Write Nine Bytes to Valid DPCD Addresses	Skipped	Skipped
5.2.1.5	Write EDID Offset (One Byte I2C-over-AUX Write)	Skipped	Skipped
5.2.1.6	Read One EDID Byte (One Byte I2C-over-AUX Read)	Skipped	Skipped
5.2.1.7	EDID Read (1 Byte I2C -over-AUX Segment Write, 1 Byte I2C-over-AUX Offset Write, 128 Byte I2C-over-AUX Read)	Skipped	Skipped
5.2.1.8	Illegal AUX Request Syntax	Skipped	Skipped
5.2.1.9	Glitch Rejection	Skipped	Skipped
5.2.1.10	Interleaved EDID and DPCD Receiver Capability Read	Yes	Yes
5.2.1.11	Downstream Stop on MOT Reset	Skipped	Yes
5.2.1.12	Downstream Stop on Timeout	Skipped	Yes
5.2.2 Sink Device DPCD Field Implementation			
5.2.2.1	Sink Organizationally Unique Identifier (OUI)	Skipped	Yes
5.2.2.2	Sink Count	Skipped	Yes
5.2.2.3	Sink Status	Skipped	Yes
5.2.2.4	Sink Error Count (Deprecated)	Skipped	Yes

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only
5.2.2.5	DPCD Address Range	Skipped	Yes
5.2.2.6	Number of Receiver Ports	Skipped	Yes
5.2.2.7	Main-Link Channel Coding	Skipped	Yes
5.2.2.8	ESI Field Mapping	Skipped	Yes
5.2.2.9	Sink Device Symbol Error Count	Skipped	Yes

Table 11 – DP CTS Sink Device Link Services Test Procedures

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only
5.3.1 Link Training			
5.3.1.1	Successful Link Training at All Supported Lane Counts and Link Speeds	Yes	Yes
5.3.1.2	Successful Link Training with Request of Higher Differential Voltage Swing during Clock Recovery Sequence	NA	NA
5.3.1.3	Successful Link Training to a Lower Link Rate Due to Clock Recovery Lock Failure during Clock Recovery Sequence	NA	NA
5.3.1.4	Successful Link Training with Request of a Change to Pre-Emphasis and/or Voltage Swing Setting during Channel Equalization Sequence	NA	NA
5.3.1.5	Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock during Channel Equalization Sequence	Skipped	Skipped
5.3.1.6	Lane Count Reduction	NA	NA
5.3.1.7	Lane Count Increase	NA	NA
5.3.1.8	Sink Device 2-Lane Link Training CR/EQ Fallback Test	Skipped	Skipped

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only
5.3.1.9	Sink Device 1-Lane Link Training CR/EQ Fallback Test	Skipped	Skipped
5.3.2 Link Maintenance			
5.3.2.1	IRQ_HPD Pulse Due to Loss of Symbol Lock and Clock Recovery Lock	Yes	Yes
5.3.2.2	IRQ_HPD Pulse Due to Loss of Inter-lane Alignment Lock	NA	NA

Table 12 – Sink Isochronous Transport Services Test Procedures

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only
5.4.1 Main Video Stream Reconstruction			
5.4.1.1	Pixel Data Reconstruction	Yes	Yes
5.4.1.2	Main Stream Data Unpacking and Unstuffing – Least Packed TU	Yes	Yes
5.4.1.3	Main Stream Data Unpacking and Unstuffing – Most Packed TU	Yes	Yes
5.4.1.4	Pixel Clock Recovery	Yes	Yes
5.4.2	Main Video Stream Format Change Handling	Yes	Yes
5.4.3 Power Management			
5.4.3.1	Entering and Exiting Power Save Mode	Yes	Yes
5.4.3.2	Resumption of Main-Link Activity after Extended Idle	Yes	Yes
5.4.4 Main Audio Stream Reconstruction			
5.4.4.1	Audio Test Patterns	Yes	Yes
5.4.4.2	Audio Startup and Format Change	Yes	Yes
5.4.4.3	RS Error Correction	Yes	Yes

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only
5.4.4.4	Audio INFOFRAME Packet	Yes	Yes
5.4.4.5	Audio Clock Recovery	Yes	Yes
5.4.4.6	Audio Stream Reception	Yes	Yes

Table 13 – Sink Device FEC Test Procedures

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only
5.5.1 Sink FEC Protocol			
5.5.1.1	Sink Device FEC Capability Verification	Skipped	Skipped
5.5.1.2	Successful Link Training at All Supported Lane Counts and Link Rates with FEC Enable	Yes	Yes
5.5.1.3	Uncorrectable Block Error Count	Skipped	Skipped
5.5.1.4	Correctable Block Error Count	Skipped	Skipped
5.5.1.5	Correctable Bit Error Count	Skipped	Skipped
5.5.1.6	Correctable Parity Block Error Count	Skipped	Skipped
5.5.1.7	Correctable Parity Bit Error Count	Skipped	Skipped

Table 14 – Sink Device DSC Test Procedures

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only
5.6.1 Sink DSC Protocol			
5.6.1.1	DSC capability verification	Skipped	Yes
5.6.1.2	DSC RGB Color Depth Test	Skipped	Yes
5.6.1.3	DSC RGB Block Prediction Test	Skipped	Yes
5.6.1.4	DSC RGB bits-per-pixel Test	Yes	Yes

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only
5.6.1.5	DSC RGB slice Test	Yes	Yes
5.6.1.6	DSC RGB lane Test	Yes	Yes
5.6.1.7	DSC YCbCr 4:4:4 Color Depth Test	Skipped	Yes
5.6.1.8	DSC YCbCr 4:4:4 Block Prediction Test	Skipped	Yes
5.6.1.9	DSC YCbCr 4:4:4 bits-per-pixel Test	Skipped	Yes
5.6.1.10	DSC YCbCr 4:4:4 slice Test	Skipped	Yes
5.6.1.11	DSC YCbCr 4:4:4 lane Test	Skipped	Yes
5.6.1.12	DSC Simple 4:2:2 Color Depth Test	Skipped	Yes
5.6.1.13	DSC Simple 4:2:2 Block Prediction Test	Skipped	Yes
5.6.1.14	DSC Simple 4:2:2 bits-per-pixel Test	Skipped	Yes
5.6.1.15	DSC Simple 4:2:2 slice Test	Skipped	Yes
5.6.1.16	DSC Simple 4:2:2 lane Test	Skipped	Yes
5.6.1.17	DSC Native 4:2:2 Color Depth Test	Skipped	Yes
5.6.1.18	DSC Native 4:2:2 Block Prediction Test	Skipped	Yes
5.6.1.19	DSC Native 4:2:2 bits-per-pixel Test	Yes	Yes
5.6.1.20	DSC Native 4:2:2 slice Test	Yes	Yes
5.6.1.21	DSC Native 4:2:2 lane Test	Yes	Yes
5.6.1.22	DSC Native 4:2:0 Color Depth Test	Skipped	Yes
5.6.1.23	DSC Native 4:2:0 Block Prediction Test	Skipped	Yes
5.6.1.24	DSC Native 4:2:0 bits-per-pixel Test	Yes	Yes
5.6.1.25	DSC Native 4:2:0 slice Test	Yes	Yes
5.6.1.26	DSC Native 4:2:0 lane Test	Yes	Yes

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only
5.6.2 Sink DSC Protocol Extension			
5.6.2.1	DSC Height Test	Skipped	Yes
5.6.2.2	DSC Padding Test	Yes	Yes
5.6.2.3	DSC RGB min and max bits-per-pixel Test	Yes	Yes
5.6.2.4	DSC YCbCr 4:4:4 min and max bits-per-pixel Test	Skipped	Yes
5.6.2.5	DSC Simple 4:2:2 min and max bits-per-pixel Test	Skipped	Yes
5.6.2.6	DSC Native 4:2:2 min and max bits-per-pixel Test	Yes	Yes
5.6.2.7	DSC Native 4:2:0 min and max bits-per-pixel Test	Yes	Yes
5.6.2.8	DSC RGB most pack Test	Yes	Yes
5.6.2.9	DSC Native 4:2:2 most pack Test	Yes	Yes
5.6.2.10	DSC Native 4:2:0 most pack Test	Yes	Yes
5.6.2.11	DSC one corrupt slice Test	Skipped	Yes
5.6.2.12	DSC interrupt test for Chunk Length error	Skipped	Yes
5.6.2.13	DSC interrupt test for RC buffer under-run error	Skipped	Yes
5.6.2.14	DSC interrupt test for RC buffer overflow error	Skipped	Yes

LTTPR Testing Table

Table 15 – Sink Device Embedded LTTPR Test Procedures

DP CTS Test Number	Test Name	Tested
5.9.1 Sink Embedded LTTPR protocol		
5.9.1.1	LTTPR global configuration verification	Skipped
5.9.1.2	LTTPR configuration and status field verification	Skipped
5.9.1.3	LTTPR AUX read/write reply time budget verification	Skipped
5.9.1.4	LTTPR 8b10b transparent link training for lane count and link rate	Yes
5.9.1.5	LTTPR 8b10b non-transparent link training for lane count and link rate	Yes
5.9.1.6	LTTPR 128b132b non-transparent link training for lane count and link rate	Skipped
5.9.1.7	LTTPR 8b10b transparent successful Link Training (Higher Differential Voltage Swing during Clock Recovery)	Skipped
5.9.1.8	LTTPR 8b10b non-transparent successful Link Training (Higher Differential Voltage Swing during Clock Recovery)	Skipped
5.9.1.9	LTTPR 8b10b transparent successful Link Training (Lower Link bandwidth During Clock Recovery)	Skipped
5.9.1.10	LTTPR 8b10b non-transparent successful Link Training (Lower Link bandwidth During Clock Recovery)	Skipped
5.9.1.11	LTTPR 8b10b transparent successful Link Training (Lower Link Bandwidth Channel Equalization)	Skipped
5.9.1.12	LTTPR 8b10b non-transparent successful Link Training (Lower Link Bandwidth Channel Equalization)	Skipped
5.9.1.13	LTTPR 128b132b non-transparent successful Link Training to Lower Link Rate, due to failure in EQ Phase of UHBR	Skipped
5.9.1.14	LTTPR 128b132b non-transparent successful Link Training to Lower Link Rate, due to failure in CDS Phase of UHBR	Skipped
5.9.1.15	LTTPR 128b132b non-transparent successful Link Training to lower bandwidth, due to no start of CDS sequence Phase of UHBR Link Training	Skipped

Known Good GPU(s) Capabilities

The test coverage provided by DP Link Layer Compliance Tests executed in Test Setups that make use of a Known Good (KG) GPU highly depends on the capabilities of the KG GPU(s) (or DP Source). The KG GPU(s) (or DP Source) used for testing shall support the capabilities outlined in Table 16.

Table 16 – Known Good GPU(s) or DP Source Capabilities Requirements

Capability	Support Level
Maximum Supported Lane Count	4 (Lanes 0, 1, 2, 3)
Maximum Supported Link Rate	8.1Gbps/lane (HBR3)
Device Test Automation DPCD extension	Yes
Spread-spectrum Clocking (SSC)	Yes
Video format change without link retraining	Yes
Supported Pixel Encoding/Colorimetry Formats	RGB YCbCr 4:4:4 YCbCr 4:2:2 YCbCr 4:2:0
Maximum bits per component (bpc)	16 bpc
FEC	Yes
Audio Transmission with Video	Yes
Audio Sample Rates Supported	32 kHz 44.1 kHz 48 kHz 88.2 kHz 96 kHz 176.4 kHz 192 kHz
DSC Support	Yes

Capability	Support Level
DSC Colorimetry	RGB YCbCr 4:4:4 Simple 4:2:2 Native 4:2:2 Native 4:2:0
DSC Maximum BPC	12
HDCP and CP_IRQ	Yes