

# USB4™ DP Tunneling

## Compliance Test Specification

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Revision: 2.2

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## Revision History:

Revision	Issue Date	Comments
1.0	January 2021	First Release
1.1	October 2021	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.2	December 2021	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.3	March 2022	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.4	October 2022	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.5	December 2022	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021 and includes additional ECN through October 2022.
Revision 2 0.71	May 2023	Updated existing tests to USB4 Version 2 Added new tests for DP IN (10.100, 10.101, 10.102 & 10.103) Added new test for DP OUT (10.120)
Revision 2 0.8	July 2023	Added Window Count Calculation section Updated Source testing tables
Revision 2 0.81	July 2023	Updated Sink testing tables Added LTTTPR testing table, and referenced 10.003 and 10.011 to use the new table
Revision 2 0.85	Aug 2023	Added ACT check for TD 10.102 Added Secondary Data check for TD 10.102 Added a DP IN setup with two monitors
Revision 2.0		Revision that unites USB4 Version 1 and Version 2. Added Source testing 4.3.3.2, 4.4.1.4-6, 4.4.2.2

		LTTPR tests 7.1.1 will be executed for DP OUT Adapter as well
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## Introduction

The tests in this specification verify that a USB4 Product is compliant with Chapter 10 of the USB4™ Specification.

## Reference Documents

- Universal Serial Bus 4 (USB4™) Specification Version 2.0 with Errata and ECN through June 29, 2023 ([USB4 Specification](#))
- VESA DisplayPort (DP) Standard Version 2.1a December 18 2023 ([DP Specification](#))
- VESA DisplayPort v2.1 Link Layer Compliance Test Specification Revision 1.0 November 13 2023 ([DP Link CTS](#))
- High-bandwidth Digital Content Protection Revision 2.3 on DisplayPort Compliance Test Specification Revision 1.1 4 March 2019 ([HDCP CTS for DP](#))
- Universal Serial Bus 4 (USB4™) Connection Manager Guide Ver. 2.0, November 2022

## Assertions

Compliance criteria are provided as a list of assertions that describe specific characteristics or behaviors that must be met. Each assertion provides a reference to the USB4 specification or other documents from which the assertion was derived. In addition, each assertion provides a reference to the specific test description(s) where the assertion is tested.

Each test assertion is formatted as follows:

Assertion #	Test #	Assertion Description
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**Assertion#:** Unique identifier for each spec requirement. The identifier is in the form USB4\_SPEC\_SECTION\_NUMBER#X, where X is a unique integer for a requirement in that section.

**Assertion Description:** Specific requirement from the specification

**Test #:** A label for a specific test description in this specification that tests this requirement. Test # can have one of the following values:

- NT        This item is not explicitly tested in a test description. Items can be labeled NT for several reasons – including items that are not testable, not important to test for interoperability, or are indirectly tested by other operations performed by the compliance test.
- X.X       This item is covered by the test described in test description X.X in this specification.
- IOP       This assertion is verified by the USB4 Interoperability Test Suite.

Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

## Ver. 1 Assertions

### Chapter 10 Assertions

The following Table presents the USB4 Specification Chapter 10 asserts.

Assertion #	How to Test	Assertion Description
<b>10 DisplayPort Tunneling</b>		
10#1	TD 10.002	A USB4 host shall support DP tunneling.
10#2	TD 10.002	A Host Router shall contain at least one DP IN Adapter and may optionally contain one or more DP OUT Adapters.
10#3	TD 10.002	A USB4 hub shall support DP Tunneling.
10#4	TD 10.002	A USB4 Hub shall contain at least one DP OUT Adapter and may optionally contain one or more DP IN Adapters.
10#5	NT	If a USB4 peripheral device supports DP Tunneling, it shall contain at least one DP Adapter.

<b>10.1 DP Adapter Port Protocol Stack</b>		
<b>10.1.1 Transport Layer</b>		
<b>10.1.2 Protocol Adapter Layer</b>		
<b>10.1.3 DP Physical Layer</b>		
10.1.3#1	TD 10.002 TD 10.002	A DP Adapter Port shall either implement the DisplayPort Physical Layer as defined in the DisplayPort 1.4a Specification or shall implement its functional equivalent (e.g. DP Adapter Port is connected to a DPRX or a DPTX as part of an SoC).
10.1.3#2	NT	A DP IN Adapter Port which does not implement a Physical Layer shall generate a stream of DisplayPort Tunneled packets as if a Physical Layer exists.
<b>10.2 DP Adapter States</b>		
<b>10.2.1 Reset</b>		
10.2.1#1	TD 10.002 TD 10.002	While in the Reset state, a DP Adapter shall set all Configuration Spaces to their default values.
10.2.1#2	NT	A DP IN Adapter shall drive HPD signal low.
10.2.1#3	NT	A DP OUT Adapter shall not apply DP_PWR.
<b>10.2.2 Present</b>		
10.2.2#1	TD 10.002 TD 10.002	While in the Present state, a DP Adapter shall set all Configuration Spaces to their default values.
10.2.2#2	NT	A DP IN Adapter Port shall drive HPD signal low.
10.2.2#3	NT	A DP OUT Adapter Port shall not apply DP_PWR.
<b>10.2.3 Plugged</b>		
10.2.3#1	NT	While in the Plugged state, a DP IN Adapter shall drive HPD signal low.

<b>10.2.4 Paired</b>		
<b>10.3 Interfaces</b>		
<b>10.3.1 DisplayPort</b>		
10.3.1#1	NT	A DP Adapter shall support three modes of operation: <u>LTTPR Non-Transparent</u> – LT-tunable PHY Repeater (Non-Transparent Mode); <u>LTTPR Transparent</u> – LT-tunable PHY Repeater (Transparent Mode); <u>Non-LTTPR</u> – Non-LT-tunable PHY Repeater.
10.3.1#2	NT	After reset, a DP Adapter shall operate in Non-LTTPR mode.
10.3.1#3	NT	A DP Adapter shall transition between the three modes as described in Section 10.4.6.1.
10.3.1#4	NT	A DP Adapter shall transition to Non-LTTPR mode upon exit from the Paired state.
<b>10.3.1.1 LTTPR Non-Transparent</b>		
10.3.1.1#1	NT	A DP IN Adapter shall implement LTTPR UFP.
10.3.1.1#2	NT	A DP OUT Adapter shall implement LTTPR DFP.
<b>10.3.1.2 Non-LTTPR</b>		
10.3.1.2#1	NT	A DP IN Adapter shall implement Non-LTTPR Non-Transparent UFP.
10.3.1.2#2	NT	A DP OUT Adapter shall implement Non-LTTPR Non-Transparent DFP.
<b>10.3.1.3 LTTPR Transparent</b>		
<b>10.3.2 Programming Model</b>		
<b>10.3.2.1 Adapter Configuration Space</b>		
<b>10.3.2.2 Path Configuration Space</b>		
10.3.2.2#1	TD 10.002 TD 10.002	A DP Adapter shall implement a Path Configuration Space as defined in Section 8.2.3.
10.3.2.2#2	NT	A DP Adapter shall support one MAIN-Link Path, one AUX Ingress Path, and one AUX Egress Path.

<b>10.3.3 Hot Plug and Hot Removal Events</b>		
<b>10.3.3.1 DP OUT Adapters</b>		
10.3.3.1#1	NT	When a DP OUT Adapter detects a Plug Event (as defined in the DisplayPort 1.4a Specification), it shall: Send a Hot Plug Event Packet with the UPG bit set to 0b as described in Section 6.8 within tDPPlug.
10.3.3.1#2	NT	When a DP OUT Adapter detects a Plug Event (as defined in the DisplayPort 1.4a Specification), it shall: Set the Plugged bit to 1b.
10.3.3.1#3	NT	When a DP OUT Adapter detects an Unplug Event (as defined in the DisplayPort 1.4a Specification), it shall: Send a Hot Plug Event Packet with the UPG bit set to 1b as described in Section 6.8 within tDPPlug.
10.3.3.1#4	NT	When a DP OUT Adapter detects an Unplug Event (as defined in the DisplayPort 1.4a Specification), it shall: Set the Plugged bit to 0b
<b>10.3.3.2 DP IN Adapters</b>		
10.3.3.2#1	NT	A Router shall send a Hot Plug Event Packet as described in Section 6.8 within tDPPlug of when both of the following are true: A DP IN Adapter detects a Source (as defined in the DisplayPort 1.4a Specification); The DP IN Adapter that detected the Plug Event has sufficient DP stream resources available to support a DP stream.
10.3.3.2#2	NT	A Router shall send a Hot Plug Event Packet with the <i>UPG</i> bit set to 1b as described in Section 6.8 within tDPPlug of when either of the following are true: A DP IN Adapter detects the removal of a Source (as defined in the DisplayPort 1.4a Specification); The Router has freed the DP stream resources allocated to the DP IN Adapter such that the DP IN Adapter can no longer support a DP stream.
<b>10.3.3.2.1 DP Stream Resource Allocation</b>		
10.3.3.2.1#1	NT	A Router shall support the DP Stream Resource Commands listed in Table 10-3 (QUERY_DP_RESOURCE, ALLOCATE_DP_RESOURCE, DEALLOCATE_DP_RESOURCE)
<b>10.3.4 DisplayPort Over USB4 Fabric</b>		
<b>10.3.4.1 DisplayPort Data Packet Types</b>		
10.3.4.1#1	NT	The Tunneled Packets types defined in Table 10-4 shall only be used for the AUX Path.
10.3.4.1#2	NT	The Tunneled Packet Types defined in Table 10-5 shall only be used for the Main-Link Path.
10.3.4.1#3	NT	If a DP Adapter receives a Tunneled Packet on the AUX Path with a PDF value other than 0 to 3, it shall discard the Tunneled Packet and shall not send any Packets in response.

10.3.4.1#4	NT	If a DP OUT Adapter receives a Tunneled Packet on the Main-Link Path with a PDF value other than 1 to 7, it shall discard the Tunneled Packet and shall not send any Packets in response.
<b>10.3.4.2 AUX Path Packets</b>		
10.3.4.2#1	NT	When generating an AUX Path Packet, a DP Adapter Layer shall put the value in the <i>AUX Tx HopID</i> field into the <i>HopID</i> field of the Tunneled Packet header.
10.3.4.2#2	NT	When a DP Adapter Layer receives a Tunneled Packet with a HopID that is equal to the <i>AUX Rx HopID</i> field, it shall treat that packet as an AUX Path Packet.
<b>10.3.4.2.1 AUX Packets</b>		
10.3.4.2.1#1	NT	An AUX Packet shall have the format shown in Table 10-7.
10.3.4.2.1#2	NT	The Tunneled Packet Header for an AUX Packet shall have the <i>PDF</i> field set to 0.
10.3.4.2.1#3	NT	AUX Packet payload shall contain the following: <b>CRC</b> : See Section 10.3.4.2.1.1.
10.3.4.2.1#4	NT	AUX Packet payload shall contain the following: <b>AUX Payload</b> : Shall contain the bytes contained between the <SYNC> and <STOP> framing bytes of a DisplayPort AUX transaction. The number of bytes in this field varies between 1 and 20.
10.3.4.2.1#5	NT	AUX Packet payload shall contain the following: <b>Reserved</b> : Shall be one byte set to 00h.
<b>10.3.4.2.1.1 CRC</b>		
10.3.4.2.1.1#1	NT	The CRC32 computation in an AUX Packet shall be based on the following CRC: Width: 32 Poly: 1EDC 6F41h Init: FFFF FFFFh RefIn: True RefOut: True XorOut: FFFF FFFFh
10.3.4.2.1.1#2	NT	If the AUX Payload is less than 21 bytes in length, a DP Adapter shall add the required number of zero-padding bytes for the computation of the CRC.
10.3.4.2.1.1#3	NT	The padding bytes shall not be transmitted in the AUX Packet.

10.3.4.2.1.1#4	NT	The CRC32 shall be generated by the DP Adapter that creates the AUX Packet and shall be checked by the DP Adapter that receives the AUX Packet
10.3.4.2.1.1#5	NT	A DP Adapter that receives an AUX Packet with a CRC error shall drop that packet.
<b>10.3.4.2.2 HPD Packets</b>		
10.3.4.2.2#1	NT	An HPD Packet shall have the format shown in Figure 10-8.
10.3.4.2.2#2	NT	The <i>PDF</i> field in the header shall be set to 1 and the <i>Length</i> field shall be 4.
10.3.4.2.2#3	NT	HPD Packet payload shall contain the following: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the HPD Packet payload.
10.3.4.2.2#4	NT	HPD Packet payload shall contain the following: <b>Reserved [30:8]</b> : Shall be set to 0.
10.3.4.2.2#5	NT	HPD Packet payload shall contain the following: <b>Plug (P) Flag [Bit 31]</b> : Shall be set to 0 if the HPD signal is low for more than 2 ms. Shall be set to 1 if the HPD signal is high.
10.3.4.2.2#6	NT	When a DP IN Adapter receives an HPD Packet, it shall check the <i>ECC</i> field of the packet payload.
10.3.4.2.2#7	NT	The DP IN Adapter shall correct single-bit errors in the HPD Tunneled Packet payload.
10.3.4.2.2#8	NT	If an uncorrectable error is detected, the HPD Packet shall be dropped.
10.3.4.2.2#9	NT	Otherwise the DP IN Adapter shall: Generate a Plug/Re-plug HPD event if the P Flag in the HPD Packet payload is set to 1b.
10.3.4.2.2#10	NT	Otherwise the DP IN Adapter shall: Generate an Unplug HPD event if the <i>P Flag</i> in the HPD Packet payload is set to 0b.
10.3.4.2.2#11	NT	Otherwise the DP IN Adapter shall: Acknowledge the HPD Packet by sending an ACK Packet to the DP OUT Adapter within tDPAckResponse of receiving the HPD Packet.
<b>10.3.4.2.3 SET_CONFIG Packet</b>		
10.3.4.2.3#1	NT	A SET_CONFIG Packet shall have the format shown in Figure 10-9.
10.3.4.2.3#2	NT	The <i>PDF</i> field in the header shall be set to 2 and the <i>Length</i> field shall be 4.

10.3.4.2.3#3	NT	SET_CONFIG Packet payload shall contain the following: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the SET_CONFIG Packet payload.
10.3.4.2.3#4	NT	SET_CONFIG Packet payload shall contain the following: <b>Link Rate 0 (LR0) [8]</b> .
10.3.4.2.3#5	NT	SET_CONFIG Packet payload shall contain the following: <b>Lane Count (LC) [11:9]</b> .
10.3.4.2.3#6	NT	SET_CONFIG Packet payload shall contain the following: <b>Reserved [12]</b> : This field shall be set to 1b by sender and ignored by receiver.
10.3.4.2.3#7	NT	SET_CONFIG Packet payload shall contain the following: <b>Link Rate 1 (LR1) [13]</b> .
10.3.4.2.3#8	NT	SET_CONFIG Packet payload shall contain the following: <b>Training Pattern Support (TPS) [15:14]</b> : This field shall specify the supported TPS which can be used in EQ Phase in Non-LTTPR and LTTPR Transparent link training.
10.3.4.2.3#9	NT	SET_CONFIG Packet payload shall contain the following: <b>TPS3 Support [14]</b> .
10.3.4.2.3#10	NT	SET_CONFIG Packet payload shall contain the following: <b>TPS4 Support [15]</b> .
10.3.4.2.3#11	NT	SET_CONFIG Packet payload shall contain the following: <b>MSG Data [31:24]</b> .
10.3.4.2.3#12	NT	SET_CONFIG Packet payload shall contain the following: <b>MSG Data [31:24]</b> .
10.3.4.2.3#13	NT	The MSG Data shall match the MSG Type of the packet as set forth in Table 10-5.
10.3.4.2.3#14	NT	A DP IN Adapter shall set the <i>LC</i> and <i>LR</i> fields in all SET_CONFIG Packets to be the same as the last SET_LINK SET_CONFIG Packet it sent.
10.3.4.2.3#15	NT	A DP OUT Adapter shall set the <i>LC</i> and <i>LR</i> fields in all SET_CONFIG Packets to be the same as the last SET_LINK SET_CONFIG Packet it received.
10.3.4.2.3#16	NT	After a DP Adapter sends a SET_CONFIG Packet, it shall wait for an ACK Packet with the <i>Type</i> field equal to 0h.
10.3.4.2.3#17	NT	After receiving an ACK Packet with the <i>Type</i> field set to 0h, the DP Adapter shall wait tDPSetConfigGap before sending the next SET_CONFIG Packet.
10.3.4.2.3#18	NT	When a DP Adapter receives a SET_CONFIG Packet, it shall check the <i>ECC</i> field of the packet payload.



10.3.4.2.3#19	NT	The DP Adapter shall correct single-bit errors in the SET_CONFIG Packet payload.
10.3.4.2.3#20	NT	If an uncorrectable error is detected, the SET_CONFIG Packet shall be dropped.
10.3.4.2.3#21	NT	Otherwise, the DP Adapter shall respond with an ACK Packet with the <i>Type</i> field equal to 0h.
10.3.4.2.3#22	NT	The ACK Packet shall be sent within tDPAckResponse of receiving the SET_CONFIG Packet.
10.3.4.2.3#23	NT	A DP Adapter that receives a SET_CONFIG Packet with a value in the <i>Type</i> field that is not listed in Table 10-5 shall respond with an ACK packet with the <i>Type</i> field equal to 0h.
<b>10.3.4.2.4 ACK Packet</b>		
10.3.4.2.4#1	NT	An ACK Packet shall have the format shown in Figure 10-10.
10.3.4.2.4#2	NT	The <i>PDF</i> field in the header shall be set to 3 and the <i>Length</i> field shall be 4.
10.3.4.2.4#3	NT	ACK Packet payload shall contain the following: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the ACK Packet payload.
10.3.4.2.4#4	NT	ACK Packet payload shall contain the following: <b>Reserved [27:8]</b> : Shall be set to 0.
10.3.4.2.4#5	NT	ACK Packet payload shall contain the following: Type [31:28]: Shall be set to 8h to acknowledge the receipt of a HPD Packet. Shall be set to 0h to acknowledge the receipt of a SET_CONFIG Packet. All other values are reserved.
<b>10.3.4.3 MAIN-Link Path Packet Formats</b>		
10.3.4.3#1	NT	When generating a Main-Link Path Packet, a DP IN Adapter Layer shall put the value in the <i>Video HopID</i> field into the <i>HopID</i> field of the Tunneled Packet header.
10.3.4.3#2	NT	When a DP OUT Adapter Layer receives a Tunneled Packet with a HopID that is equal to the <i>Video HopID</i> field, it shall treat that packet as a Main-Link Path Packet.

<b>10.4 System Flows</b>		
<b>10.4.1 Connection Manager Discovery</b>		
<b>10.4.2 Path Configuration</b>		
<b>10.4.2.1 Setup</b>		
10.4.2.1#1	NT	A DP OUT Adapter shall poll the DP_STATUS.CMHS field and DP_REMOTE_CAP.Protocol Adapter Version field for as long as the values in those fields are both 0.
10.4.2.1#2	NT	When either DP_STATUS.CMHS = 1 or DP_REMOTE_CAP.Protocol Adapter Version > 0, the DP OUT Adapter shall do the following: If DP_REMOTE_CAP.Protocol Adapter Version was set to non-zero value while DP_STATUS_CTRL.CMHS remained zero, a DP OUT Adapter shall conclude it is a TBT3 Connection Manager and shall continue the flow as defined in Section 13.8.3.
10.4.2.1#3	NT	When either DP_STATUS.CMHS = 1 or DP_REMOTE_CAP.Protocol Adapter Version > 0, the DP OUT Adapter shall do the following: If DP_STATUS_CTRL.CMHS is set to 1 and DP_STATUS_CTRL.UF is zero, a DP OUT Adapter shall conclude it is a TBT3 DP IN Adapter and shall continue the flow as defined in Section 13.8.3.
10.4.2.1#4	NT	When either DP_STATUS.CMHS = 1 or DP_REMOTE_CAP.Protocol Adapter Version > 0, the DP OUT Adapter shall do the following: If DP_STATUS_CTRL.CMHS is set to 1 and DP_STATUS_CTRL.UF is set to one, a DP OUT Adapter shall reset DP_STATUS_CTRL.CMHS to zero.
10.4.2.1#5	TD 10.1 TD 10.9	A DP Adapter shall set the DP_COMMON_CAP register, to reflect the lowest common capability between DP_LOCAL_CAP and DP_REMOTE_CAP fields.
<b>10.4.2.2 Tear-down</b>		
10.4.2.2#1	TD 10.1 TD 10.9	When the ADP_DP_CS_0.AE bit and the ADP_DP_CS_0.VE bit are both set to 0, a DP Adapter shall set all the fields in its DP Adapter Configuration Capability to their default values.
<b>10.4.3 HPD Event Propagation</b>		
<b>10.4.3.1 HPD Plug</b>		
10.4.3.1#1	NT	After a Path is setup between a DP OUT Adapter and a DP IN Adapter per 10.4.2.1, the DP OUT Adapter shall send an HPD Packet with the <i>P Flag</i> set to 1b.
10.4.3.1#2	NT	Upon receiving an HPD Packet with the <i>P Flag</i> set to 1b, the DP IN Adapter shall respond with an ACK Packet, execute the DP Adapter Init flow as defined in Section 10.4.5, and then drive HPD signal high on the DisplayPort interface

10.4.3.1#3	NT	After the DP IN Adapter drives HPD high, both DP Adapters shall be ready to handle AUX transactions.
<b>10.4.3.2 HPD Unplug</b>		
10.4.3.2#1	NT	Upon unplug detection, the DP OUT Adapter shall send an HPD Packet with the <i>P Flag</i> set to 0b to the DP IN Adapter.
10.4.3.2#2	NT	The DP IN Adapter shall respond with an ACK Packet and drive the HPD signal low.
10.4.3.2#3	NT	When the HPD signal is low, a DP IN Adapter may disable its DP Link receiver.
<b>10.4.3.3 IRQ</b>		
10.4.3.3#1	NT	Upon IRQ detection, a DP OUT Adapter shall send a SET_CONFIG Packet of MSG type IRQ to the DP IN Adapter.
10.4.3.3#2	NT	A DP IN Adapter that receives a SET_CONFIG Packet of MSG type IRQ shall respond with an ACK Packet and drive the IRQ event (according to the DisplayPort 1.4a Specification) towards the DPTX.
10.4.3.3#3	NT	However, if Link training is in process or it just ended, a DP OUT Adapter shall wait tIRQDelay after it sent a SET_CONFIG Packet to the DP IN Adapter (reporting that Link training is completion) before sending the IRQ SET_CONFIG Packet.
<b>10.4.3.4 HPD Delay Requirements</b>		
10.4.3.4#1	NT	Table 10-7 defines the maximum propagation delay through the DP Adapters that shall be used for HPD Events.
10.4.3.4#2	NT	The propagation delay through the DP OUT Adapter shall be measured from when the event is detected by the DP OUT Adapter to when the last bit of the corresponding packet, SET_CONFIG or HPD, is sent over the AUX Path.
10.4.3.4#3	NT	The propagation delay through the DP IN Adapter shall be measured from when the last bit of an HPD Event Packet, SET_CONFIG or HPD, arrives at the DP IN Adapter to when event is driven on the HPD signal.
10.4.3.4#4	NT	A DP OUT Adapter shall send HPD packet with the <i>P Flag</i> set to 1b within tDPPlug of transitioning to the Paired state.
<b>10.4.3.5 Manual HPD Control</b>		
10.4.3.5#1	TD 10.002	When HPDC transitions from 0b to 1b, a DP IN Adapter shall drive the DisplayPort HPD signal low.
10.4.3.5#2	TD 10.002	When HPDS transitions from 0b to 1b, a DP IN Adapter shall drive the DisplayPort HPD signal high.

10.4.3.5#3	TD 10.002	The DisplayPort HPD signal level shall be set according to the most recent event, whether it is HPDS set, HPDC set, IRQ SET_CONFIG Packet or HPD Packet.
<b>10.4.4 AUX Request and Response Handling</b>		
<b>10.4.4.1 LTTPR Non-Transparent Mode</b>		
<b>10.4.4.1.1 DP IN Adapter Requirements</b>		
10.4.4.1.1#1	NT	Upon reception of a DisplayPort AUX request, a DP IN Adapter shall send an AUX Packet containing the request over the AUX Path.
10.4.4.1.1#2	NT	The AUX request coming from the DPTX shall not be modified by the DP IN Adapter.
10.4.4.1.1#3	NT	For Target transactions, the DP IN Adapter shall set the AUX_PEND flag as defined in the DisplayPort 1.4a Specification – Section 3.6.5.3.2, and take the appropriate action when the request comes back according to the DisplayPort 1.4a Specification – Section 3.6.5.3.2.
10.4.4.1.1#4	NT	When a DP IN Adapter updates the DP OUT Adapter as the results of a Snoop or Target transaction, it shall perform the update only after receiving an AUX ACK response for all cases beside SET_CONFIG Packet of type SET_VSPE.
10.4.4.1.1#5	NT	The update shall be done by sending SET_CONFIG Packets to the DP OUT Adapter.
<b>10.4.4.1.2 DP OUT Adapter Requirements</b>		
10.4.4.1.2#1	TD 10.005	A DP OUT Adapter shall convert an incoming AUX Packet received from the USB4 Fabric into a DisplayPort AUX request.
10.4.4.1.2#2	TD 10.005	The content of the request shall not be modified by the DP OUT Adapter.
10.4.4.1.2#3	TD 10.005	A DP OUT Adapter shall convert an incoming DisplayPort AUX response into an AUX Packet and send it on the AUX Path.
10.4.4.1.2#4	TD 10.005	The content of the response shall not be changed by the DP OUT Adapter.
<b>10.4.4.2 Non-LTTPR Mode</b>		
10.4.4.2#1	TD 10.004	A DP IN Adapter shall implement AUX Replier.
10.4.4.2#2	TD 10.004	A DP OUT Adapter shall implement AUX Requester.
<b>10.4.4.2.1 AUX Timeout Timers</b>		
10.4.4.2.1#1	TD 10.004	The AUX Response Timeout timer in a DP IN Adapter shall be set to 300μs.

10.4.4.2.1#2	TD 10.004	The AUX Reply Timeout timer in a DP OUT Adapter shall be set to 400 $\mu$ s.
<b>10.4.4.2.2 DP IN Adapter Port Requirements</b>		
10.4.4.2.2#1	TD 10.004	A DP IN Adapter that receives an AUX Request shall classify the AUX Transaction as one of the three following types: 1) Internal AUX Transaction – AUX Request which targets only DPCD addresses that are defined as internal in Table 10-8; 2) External AUX Transaction – AUX Request which targets only DPCD addresses that are not defined as internal in Table 10-8; 3) Combined AUX Transaction – AUX Request which targets both Internal and External DPCD addresses. The AUX Response is initially generated by the DPRX and altered by the DP IN Adapter.
10.4.4.2.2#2	TD 10.004	For Internal AUX Transactions, a DP IN Adapter shall not send the AUX Request downstream and shall self-generate the AUX Response.
10.4.4.2.2#3	TD 10.004	For External and Combined AUX Transactions, a DP IN Adapter shall send the AUX Request downstream to the DP OUT Adapter.
10.4.4.2.2#4	TD 10.004	The DP IN Adapter shall generate an AUX DEFER if the Response timer expires while waiting for the AUX Response.
10.4.4.2.2#5	TD 10.004	A DP IN Adapter shall not send an AUX Request to a DP OUT Adapter while the AUX Reply to the preceding AUX Request is outstanding.
10.4.4.2.2#6	TD 10.004	DP IN Adapter shall increment AUX_REQ_CNTR by 1 on every received AUX request from DPTX and shall reset to zero on transition to IDLE state.
10.4.4.2.2#7	TD 10.004	Table 10-10: DP IN Adapter Port AUX Handling State Machine
<b>10.4.4.2.3 DP OUT Adapter Requirements</b>		
10.4.4.2.3#1	TD 10.004	A DP OUT Adapter that receives a DPTX initiated AUX Request while handling a DP OUT Adapter Initiated AUX Transaction, shall send the DPTX initiated AUX Request as soon as it is in Talk Mode.
<b>10.4.4.2.3.1 DPTX Initiated AUX Transactions</b>		
10.4.4.2.3.1#1	TD 10.004	A DP OUT Adapter that receives an AUX Request from a DP IN Adapter shall initiate the AUX Request as soon as it is in Talk Mode.
10.4.4.2.3.1#2	TD 10.004	A DP OUT Adapter that receives an AUX Response shall send the AUX Response over the AUX Path to the DP IN Adapter.
10.4.4.2.3.1#3	TD 10.004	If the AUX Reply Timer expires before an AUX Response is received, a DP OUT Adapter shall send a SET_CONFIG of type SET_AUX_INIT and shall not retry the AUX Request.

<b>10.4.4.2.3.2 DP OUT Adapter Initiated AUX Transactions</b>		
<b>10.4.4.3 LTTTPR Transparent Mode</b>		
10.4.4.3#1	NT	A DP IN Adapter shall implement AUX Replier.
10.4.4.3#2	NT	A DP OUT Adapter shall implement AUX Requester.
<b>10.4.4.3.1 AUX Timeout Timers</b>		
10.4.4.3.1#1	NT	The AUX Response Timeout timer in a DP IN Adapter shall not be activated.
10.4.4.3.1#2	NT	The AUX Reply Timeout timer in a DP OUT Adapter shall be set to 3.2ms.
<b>10.4.4.3.2 DP IN Adapter Requirements</b>		
10.4.4.3.2#1	NT	A DP IN Adapter that receives an AUX Request shall classify the AUX Transaction as one of the following types: Internal AUX Transaction – AUX Request which targets only DPCD addresses that are defined as internal in Table 10-9; External AUX Transaction – AUX Request which targets only DPCD addresses that are not defined as internal in Table 10-9; Combined AUX Transaction – AUX Request which targets both Internal and External DPCD addresses. The AUX Response is initially generated by the DPRX and altered by the DP IN Adapter.
10.4.4.3.2#2	NT	For External and Combined AUX Transactions, a DP IN Adapter shall send the AUX Request downstream to the DP OUT Adapter.
10.4.4.3.2#3	NT	A DP IN Adapter shall not: Generate AUX DEFER; Gate any External or Combined AUX Request sent by the DPTX; Gate any AUX Response sent by the DPRX.
<b>10.4.4.3.3 DP OUT Adapter Requirements</b>		
10.4.4.3.3#1	NT	A DP OUT Adapter that receives a DPTX initiated AUX Request while handling a DP OUT Adapter Initiated AUX Transaction, shall send the DPTX initiated AUX Request as soon as it is in Talk Mode.
<b>10.4.4.3.3.1 DP TX Initiated AUX Transactions</b>		
10.4.4.3.3.1#1	NT	A DP OUT Adapter that receives an AUX Request from a DP IN Adapter shall initiate the AUX Request as soon as it is in Talk Mode.
10.4.4.3.3.1#2	NT	A DP OUT Adapter that receives an AUX Response shall send the AUX Response over the AUX Path to the DP IN Adapter.
10.4.4.3.3.1#3	NT	If the AUX Reply Timer expires before an AUX Response is received, a DP OUT Adapter shall send a SET_CONFIG of type SET_AUX_INIT and shall not retry the AUX Request.

<b>10.4.4.3.3.2 DP OUT Adapter Initiated AUX Transactions</b>		
<b>10.4.4.4 AUX Delay Requirements</b>		
10.4.4.4#1	TD 10.004	The DP-to-USB4 Fabric delay shall be measured from the time the last bit arrives at the DP Adapter from the DisplayPort interface to the time when the first bit is sent to the USB4 Fabric.
10.4.4.4#2	TD 10.004	USB4 Fabric-to-DP delay shall be measured from the time when the last bit of the AUX Packet arrives at the DP Adapter to the time when the first bit is sent to the DisplayPort Interface, assuming the DP Adapter is in Talk Mode.
<b>10.4.4.5 Aggregation DisplayPort Capabilities</b>		
10.4.4.5#1	TD 10.002 TD 10.004	A DP IN Adapter shall update its DP_LOCAL_CAP and DP_COMMON_CAP registers if it receives an AUX Read Response that has lower parameter values than the registers currently contain.
10.4.4.5#2	TD 10.002 TD 10.004	Before transmitting the AUX Read Response, the DP IN Adapter shall update the AUX Read Response to reflect the aggregated DisplayPort Capabilities as shown in Table 10-11.
<b>10.4.4.6 DPCD DP Tunneling over USB4</b>		
10.4.4.6#1	NT	When a DP IN Adapter receives an AUX Request targeting the DP Tunneling over USB4 Field DPCDs, it shall respond with its internal data.
10.4.4.6#2	NT	A DP IN Adapter shall set the <i>DP Tunneling Support</i> bit to 1b in the DP TUNNELING_CAPABILITIES DPCD (Address E000Dh bit offset 0).
<b>10.4.5 DP Adapters Init Flow</b>		
10.4.5#1	TD 10.007	A DP IN Adapter in the Paired state shall do the following after receiving a first HPD Packet with the <i>P flag</i> set to 1b: Update MFDP Mode inner variable according to Section 10.4.5.1.
10.4.5#2	TD 10.007	A DP IN Adapter in the Paired state shall do the following after receiving a first HPD Packet with the <i>P flag</i> set to 1b: Send a SET_CONFIG Packet of type SET_AUX_INIT.
10.4.5#3	TD 10.007	The DP IN Adapter shall not drive HPD high on the DisplayPort Interface until after it performs the steps above.
<b>10.4.5.1 Multi-Function DP</b>		
10.4.5.1#1	TD 10.007	If a DP IN Adapter is not connected as part of a Multi-Function (as defined in the DisplayPort Alt Mode Specification), it shall send a SET_CONFIG Packet of type SET_MFDP with the MFDP Enable bit set to 0b.

10.4.5.1#2	TD 10.007	A DP OUT Adapter which receives a SET_CONFIG Packet of type SET_MFDP shall respond with a SET_CONFIG Packet of type SET_MFDP within tDPInit.
10.4.5.1#3	TD 10.007	If the DP OUT Adapter is connected as part of Multi-Function as defined in the DisplayPort 1.4a Specification, then the MFDP Enable bit shall be set to 1b, otherwise it shall be set to 0b.
<b>10.4.6 DP Source Discovery</b>		
<b>10.4.6.1 LTTPR Recognition and Modes Change</b>		
10.4.6.1#1	NT	A DP IN Adapter shall modify the resulting AUX read response as defined in Section 10.4.4.5.
10.4.6.1#2	NT	If DP_COMMON_CAP.LTTPR <i>Not Supported</i> is set to 1b, a DP Adapter shall operate only in Non-LTTPR mode.
10.4.6.1#3	NT	A DP IN Adapter shall do the following before transitioning to LTTPR Transparent mode: Complete the AUX Transaction according to the current operation mode; Send a SET_CONFIG Packet of type SET_LTTPR_MODE with LTTPR_Mode set to 0b.
10.4.6.1#4	NT	A DP IN Adapter shall do the following before transitioning to LTTPR Non-Transparent mode: Complete the AUX Transaction according to the current operation mode; Send a SET_CONFIG Packet of type SET_LTTPR_MODE with LTTPR_Mode set to 1b.
<b>10.4.6.2 DPRX Capabilities Read</b>		
10.4.6.2#1	NT	The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall: 1) Snoop the read response and record the values of the DPCD_REV, MAX_LINK_RATE, MAX_LANE_COUNT, TPS3_SUPPORTED and TPS4_SUPPORTED fields located at DPCD addresses 00000h, 00001h, 00002h and 00003h respectively.
10.4.6.2#2	NT	The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall: 2) Update the Maximal DPCD Rev, Maximal Link Rate, Maximal Lane Count, TPS3 Capability and TPS4 Capability fields in the DP_LOCAL_CAP and DP_COMMON_CAP registers to reflect the lowest common capabilities between the existing values of those registers and the recorded values from step 1.
10.4.6.2#3	NT	The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall: 3) Send a SET_CONFIG Packet of type SET_CMN_DPRX with MSG Data equal to the snooped DPCD_REV which reflects the DPRX DPCD_REV.



10.4.6.2#4	NT	The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall: 4) Set the <i>DPRX Capabilities Read Done</i> field in the DP_COMMON_CAP register to 1b. Note that this field is set to 1b regardless of whether or not the values in the <i>Maximal Link Rate</i> and <i>Maximal Lane Count</i> fields in Step 2 were changed.
<b>10.4.6.3 Sink Count Read</b>		
10.4.6.3#1	TD 10.002	When DPCD addresses 00200h or 02002h are read by the DPTX, a DP IN Adapter shall snoop the read response and record the value of the SINK_COUNT.
10.4.6.3#2	TD 10.002	When the recorded SINK_COUNT value is zero, the DP IN Adapter shall send a SET_CONFIG Packet of type SET_SINK_COUNT, reflecting the recorded value.
10.4.6.3#3	TD 10.002	When a DP OUT Adapter receives a SET_CONFIG Packet of type SET_SINK_COUNT with the SINK_COUNT value equal to zero, the DP OUT Adapter shall: Report an Unplug event as defined in Section 10.3.3.
10.4.6.3#4	TD 10.002 TD 10.004	When a DP OUT Adapter receives a SET_CONFIG Packet of type SET_SINK_COUNT with the SINK_COUNT value equal to zero, the DP OUT Adapter shall: Set the ADP_DP_CS_2.HPD Status to 0b in the <i>DP OUT Adapter Configuration Capability</i> Field.
10.4.6.3#5	TD 10.002 TD 10.004	While a DP OUT Adapter is Unplugged and has the ADP_DP_CS_2.HPD Status set to 0b in the <i>DP OUT Adapter Configuration Capability</i> Field, it shall do the following upon IRQ detection: Report a Plug event as defined in Section 10.3.3.
10.4.6.3#6	TD 10.002 TD 10.004	While a DP OUT Adapter is Unplugged and has the ADP_DP_CS_2.HPD Status set to 0b in the <i>DP OUT Adapter Configuration Capability</i> Field, it shall do the following upon IRQ detection: Set the ADP_DP_CS_2.HPD Status to 1b in the <i>DP OUT Adapter Configuration Capability</i> Field.
<b>10.4.7 Down-Spread Control</b>		
10.4.7#1	NT	When DPCD address 00107h is written by a DPTX, a DP IN Adapter, operating in Non-LTTPR or LTTPR Transparent Modes, shall respond with AUX ACK and shall send a SET_CONFIG Packet of type SET_DOWNSPREAD.
10.4.7#2	NT	The <i>MSG Data</i> field in the SET_CONFIG Packet shall be equal to the value written by the DPTX.
10.4.7#3	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of type SET_DOWNSPREAD shall initiate an AUX write request to DPCD address 00107h with the value received in the MSG Data of the SET_CONFIG Packet.

10.4.8 Stream Mode Set		
10.4.8#1	NT	If the DPTX writes to DPCD address 00111h, a DP IN Adapter shall snoop the write request and record the value of the MST_EN bit.
10.4.8#2	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_STREAM_MODE, reflecting the recorded value of the MST_EN bit when a new recorded MST_EN value is different than the previous value
10.4.8#3	NT	The MST_EN default value at the DP Adapters shall be as defined in the DisplayPort 1.4a Specification.
10.4.8#4	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of type SET_STREAM_MODE shall respond with a SET_CONFIG Packet of type SET_STREAM_MODE, to signify the acknowledgment of the mode change.
10.4.8#5	NT	The value of the <i>MSG Data</i> field in the return packet has no meaning and shall be ignored by the DP IN Adapter.
10.4.9 DSC and FEC Enable		
10.4.9#1	NT	If the DPTX writes to DPCD address 00120h, a DP IN Adapter shall snoop the write request and record the values of the <i>FEC_READY</i> , <i>FEC_ERROR_COUNT_SEL</i> and <i>LANE_SELECT</i> fields.
10.4.9#2	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_FEC_READY, reflecting the recorded value of the FEC_READY bit when a new recorded FEC_READY value is different than the previous value.
10.4.9#	NT	The FEC_READY default value at the DP Adapters shall be as defined in the DisplayPort 1.4a Specification.
10.4.9#	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of type SET_FEC_READY shall respond with a SET_CONFIG Packet of type SET_FEC_READY within tDPInit, to signify the acknowledgment of the mode change.
10.4.9#	NT	The value of the <i>MSG Data</i> field in the return packet has no meaning and shall be ignored by the DP IN Adapter.

10.4.10 DP Link Training		
10.4.10.1 LTTTPR		
10.4.10.1#1	NT	The DP IN and DP OUT Adapters shall follow the LTTTPR Non-Transparent link training as defined in the DisplayPort 1.4a Specification while noting the following points: <u>DP IN as UFP and DFP</u> – As described in Section 10.4.4, the DP IN Adapter serves as UFP and DFP for AUX handling, therefore it updates the DP OUT Adapter with the different stages of the LTTTPR Non-Transparent link training through SET_CONFIG Packets; <u>Training Patterns</u> – Training Patterns are not carried over the USB4 Fabric.
10.4.10.1.1 DP IN Adapter Requirements		
10.4.10.1.1#1	NT	After DP Link training is finished on the UFP, a DP IN Adapter shall maintain symbol lock and lane alignment in its receiver while DPTX trains the rest of downstream DP Links
10.4.10.1.1#2	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_LINK after DPTX writes TPS1 to the DP IN Adapter TRAINING_PATTERN_SET_PHY_REPEATERx DPCD register.
10.4.10.1.1#3	NT	The SET_CONFIG packet shall have the following values: LC = LANE_COUNT_SET value written by DPTX; LR = LINK_BW_SET value written by the DPTX; MSG Data = 1b, representing DP Link Training Mode = LTTTPR Non-Transparent.
10.4.10.1.1#4	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_TRAINING with TS = 0xFF after DPTX writes 0x0 to the DP IN Adapter TRAINING_PATTERN_SET_PHY_REPEATERx DPCD register.
10.4.10.1.1#5	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_TRAINING with TS = 0x0 after DPTX writes 0x0 to the DPRX TRAINING_PATTERN_SET DPCD register.
10.4.10.1.1#6	NT	After DP Link training is finished on the UFP, a DP IN Adapter shall detect a Training pattern on its receiver.
10.4.10.1.1#7	NT	After detecting the Training pattern, the DP IN Adapter shall send a single corresponding SET_CONFIG Packet of type SET_TRAINING for every change in Training pattern.
10.4.10.1.1#8	NT	The TS field shall be equal to the detected Training pattern as defined in Table 10-5.
10.4.10.1.1#9	NT	A DP IN Adapter shall send SET_CONFIG Packet of Type SET_VSPE when DPTX writes the TRAINING_LANE0_SET or TRAINING_LANE0_SET_PHY_REPEATERx DPCD register of the next downstream receiver.
10.4.10.1.1#10	NT	The MSG Data field shall carry the value in the write request.

10.4.10.1.1#11	NT	The SET_VSPE SET_CONFIG Packet shall be sent by the DP IN Adapter before sending the AUX Request Packet.
10.4.10.1.1#12	NT	A DP Adapter shall have higher priority generating and parsing SET_CONFIG packets over AUX Transaction.
10.4.10.1.1#13	NT	A DP IN Adapter shall respond to a DPTX that link training has ended successfully only when all the following are true: The DP IN Adapter internal status indicates link training has ended successfully; The DP IN Adapter sent at least nine DP Clock Sync Packets after it sent the SET_CONFIG Packet of type SET_LINK.
<b>10.4.10.1.2 DP OUT Adapter Requirements</b>		
10.4.10.1.2#1	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of Type SET_LINK with the DP Link Training Mode bit set to 1b shall start its internal Symbol clock PLL according to the <i>Link Rate</i> field, and start the Lifetime Counter as defined in Section 10.6.1.2.
10.4.10.1.2#2	NT	Deprecated.
10.4.10.1.2#3	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of Type SET_TRAINING with <i>TS</i> field equal to 0 shall transmit IDLE pattern according to the DisplayPort 1.4a Specification.
10.4.10.1.2#4	NT	A DP OUT Adapter shall set its Voltage Swing (VS) and Pre-Emphasis (PE) levels for all enabled lanes upon receiving a SET_CONFIG Packet of type SET_VSPE. The VS and PE levels shall be according to the MSG Data. The DP OUT Adapter shall transition on the 10-bit symbol boundary when: Transitioning from one training pattern to another training pattern; Transitioning to IDLE sequence after DP Link training is done.
<b>10.4.10.1.3 DP Link Training Example</b>		
<b>10.4.10.1.3.1 LTTTPR - CR_DONE Phase</b>		
<b>10.4.10.1.3.2 LTTTPR - EQ Phase</b>		
<b>10.4.10.1.3.3 DPRX - CR_DONE Phase</b>		
<b>10.4.10.1.3.4 DPRX - EQ Phase</b>		
<b>10.4.10.2 Non-LTTTPR and LTTTPR Transparent</b>		
10.4.10.2#1	NT	A DP Adapter shall perform DisplayPort link training according to the DisplayPort 1.4a Specification with the modifications and requirements defined in Section 10.4.10.2.1 and Section 10.4.10.2.2

10.4.10.2.1 DP IN Adapter Requirements		
10.4.10.2.1#1	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_LINK after DPTX writes TPS1 to the DP RX TRAINING_PATTERN_SET DPCD register.
10.4.10.2.1#2	NT	The SET_CONFIG packet shall have the following values: LC = LANE_COUNT_SET value written by DPTX; LR = LINK_BW_SET value written by the DPTX; TPS = Reflects TPS3 and TPS4 support as indicated in the DP_COMMON_CAP register; MSG Data = 0b, representing DP Link Training Mode = Non-LTTPR and LTTPR Transparent modes.
10.4.10.2.1#3	NT	A DP IN Adapter shall respond to a status read of LANEx_CR_DONE as follows: If a SET_CONFIG Packet of type STATUS_CR_DONE was not received since link training started, set the LANEx_CR_DONE bits to 0b.
10.4.10.2.1#4	NT	A DP IN Adapter shall respond to a status read of LANEx_CR_DONE as follows: If a SET_CONFIG Packet of type STATUS_CR_DONE was received since link training started, set the LANEx_CR_DONE bits to be the internal DP IN Adapter status for a lane ANDed with the relevant bit present in the last received SET_CONFIG MSG Data.
10.4.10.2.1#5	NT	A DP IN Adapter shall respond to a DPTX that link training has ended successfully only when all the following are true: The DP IN Adapter internal status indicates link training has ended successfully; The DP IN Adapter received a SET_CONFIG Packet of type SET_LINK, carrying the same LC and LR fields that it sent to the DP OUT Adapter when link training was initiated; The DP IN Adapter sent at least nine DP Clock Sync Packets after it received a SET_CONFIG Packet of type STATUS_CR_DONE.
10.4.10.2.1#6	NT	While the conditions (as defined in this section) for successful link training are not met, a DP IN Adapter shall respond to a status read of INTERLANE_ALIGN_DONE, LANEx_CHANNEL_EQ_DONE and LANEx_SYMBOL_LOCKED as follows: If a SET_CONFIG Packet of type STATUS_TRAINING_FAIL was received since link training started, set the following bits: INTERLANE_ALIGN_DONE shall be set to 0b. LANEx_CHANNEL_EQ_DONE is equal to the DP IN internal status ANDed with LANEx_CHANNEL_EQ_DONE that was received as MSG Data by the STATUS_TRAINING_FAIL. LANEx_SYMBOL_LOCKED is equal to the DP IN internal status ANDed with LANEx_SYMBOL_LOCKED that was received as MSG Data by the STATUS_TRAINING_FAIL.
10.4.10.2.1#7	NT	Else, a DP IN Adapter shall use one or more of the methods below to indicate to DPTX that link training has not completed successfully yet: Set INTERLANE_ALIGN_DONE to 0b; Set LANEx_CHANNEL_EQ_DONE to 0b for any of the active lanes; Set LANEx_SYMBOL_LOCKED to 0b for any of the active lanes.

10.4.10.2.2 DP OUT Adapter Requirement		
10.4.10.2.2#1	NT	A DP OUT Adapter receiving a SET_CONFIG Packet of type SET_LINK, with <i>LC</i> field other than 0h shall: Initiate link training with the target Link Rate and Lane Count received from the SET_LINK Packet.
10.4.10.2.2#2	NT	A DP OUT Adapter receiving a SET_CONFIG Packet of type SET_LINK, with <i>LC</i> field other than 0h shall: Link training proceeds according to the DisplayPort 1.4a spec except that a DP OUT Adapter that concludes that it needs to either reduce the Link Rate or Lane Count shall treat it as link training failure and shall not reduce the Link Rate or Lane Count.
10.4.10.2.2#3	NT	A DP OUT Adapter which finishes the Clock Recovery Sequence (as defined in the DisplayPort 1.4a Specification) shall send a SET_CONFIG Packet of type STATUS_CR_DONE, reflecting the LANEx_CR_DONE statuses of the active lanes.
10.4.10.2.2#4	NT	The <i>Phase</i> field shall be set to 0b.
10.4.10.2.2#5	NT	A DP OUT Adapter in EQ phase which detects that the DP receiver has lost Clock Recovery on one or more of the active lanes shall conclude that link training has failed and shall send a SET_CONFIG Packet of type STATUS_CR_DONE, reflecting the new LANEx_CR_DONE statuses of the active lanes.
10.4.10.2.2#6	NT	The <i>Phase</i> field shall be set to 1b.
10.4.10.2.2#7	NT	If link training fails for a reason other than lost Clock Recovery, a DP OUT Adapter shall send a SET_CONFIG Packet of type STATUS_TRAINING_FAIL.
10.4.10.2.2#8	NT	If link training finishes successfully, a DP OUT Adapter shall send a SET_CONFIG Packet of type SET_LINK, with the same <i>LC</i> and <i>LR</i> fields it received from the DP IN Adapter when link training was initiated.
10.4.10.2.2#9	NT	Deprecated.
10.4.10.2.2#10	NT	The MSG Data shall be set as follows: LANEx_CHANNEL_EQ_DONE is equal to the value of the last read from LANEx_CHANNEL_EQ_DONE field in DPRX. LANEx_SYMBOL_LOCKED is equal to the value of the last read from LANEx_SYMBOL_LOCKED field in DPRX.
10.4.10.3 Transition to High Speed Tunnel		
10.4.10.3#1	NT	A DP IN Adapter shall start converting DisplayPort Main-Link Symbols into Tunneled Packets and sending those Packets over the Main-Link Path when all of the following are true: Link Training has completed successfully; The DP IN Adapter received an SR.

<b>10.4.11 Power States Set</b>		
10.4.11#1	NT	When DPTX writes to DPCD address 00600h, a DP IN Adapter shall snoop the write request and record the value of the <i>SET_POWER_STATE</i> field.
10.4.11#2	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_POWER, reflecting the recorded value in the following cases: A first DPCD write of address 00600h after an HPD Plug event.
10.4.11#3	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_POWER, reflecting the recorded value in the following cases: The new recorded SET_POWER_STATE is different than the previous value.
<b>10.4.12 DP Main-Link Disable</b>		
10.4.12#1	NT	DP OUT Adapter which receives a Main-Link disable message shall disable its transmitters.
<b>10.4.13 Link-Init</b>		
10.4.13#1	NT	Upon Link-Init activation, a DP IN Adapter shall turn off its DisplayPort receivers and stop any transmission of Tunneled Packets over the Main-Link Path until the end of the next successful Link training, as defined in Section 10.4.10.3.
10.4.13#2	NT	Upon Link-Init activation, a DP OUT Adapter shall turn off its DisplayPort transmitters.
<b>10.4.14 DP PHY Testability</b>		
<b>10.4.14.1 DP IN Adapter PHY Layer Testing</b>		
10.4.14.1#1	NT	The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Before entering DP IN PHY Test Mode: Connect a Router with a DP OUT Adapter and a DPRX. Both the DP OUT Adapter and the DPRX need to support the Link Rate and Lane Count required by the test; Verify that a DP Link is established.
10.4.14.1#2	NT	The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Entering DP IN PHY Test Mode: The DP IN Adapter shall enter DP IN PHY Test Mode when the DPTX writes a non-zero value to LINK_QUAL_LANE <sub>Ex</sub> _SET in the DPCD registers.
10.4.14.1#3	NT	The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: While in DP IN PHY Test Mode: The DP IN Adapter shall keep the Hot Plug Detect signal high; The DP IN Adapter shall respond to all AUX transactions related to the PHY layer testing.

10.4.14.1#4	NT	The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Exiting DP IN PHY Test Mode: The DP IN Adapter shall exit DP IN PHY Test Mode when the DPTX initiates DP Link Training.
<b>10.4.14.2 DP OUT Adapter PHY Layer Testing</b>		
10.4.14.2#1	NT	The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Before entering DP OUT PHY Test Mode: Connect a Router with a DP IN Adapter and a DPTX. Both the DP IN Adapter and the DPTX need to support the test required Link Rate and Lane Count; Verify that a DP Link is established.
10.4.14.2#2	NT	The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Entering DP OUT PHY Test Mode: When the DPTX reads the following sequence, the DP IN Adapter shall send a SET_CONFIG Packet of Type SET_PHY_TEST_MODE and enter DP OUT PHY Test Mode: AUTOMATED_TEST_REQUEST is set to 1b (DPCD 00201h or 02003h bit 1); PHY_TEST_PATTERN is set to 1b (DPCD 00218h bit 3). The DP OUT Adapter shall enter DP OUT PHY Test Mode when it receives a SET_CONFIG Packet of type SET_PHY_TEST_MODE.
10.4.14.2#3	NT	The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: While in DP OUT PHY Test Mode: The DP OUT Adapter shall act as the DPTX under test; The DP OUT Adapter shall send HPD Packet with Plug Flag set to 0b; The DP IN Adapter shall not forward any AUX Transactions to the DP OUT Adapter.
10.4.14.2#4	NT	The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Exiting DP OUT PHY Test Mode: Upon a DPRX HPD signal de-assertion: The DP OUT Adapter shall exit DP OUT PHY Test Mode; The Connection Manager tears down the DP Paths, causing both of the DP Adapters to enter the Present State.
<b>10.5 High Speed Tunneling</b>		
<b>10.5.1 SST Tunneling</b>		
<b>10.5.1.1 Video Data Packet</b>		
<b>10.5.1.1.1 Transfer Unit Set</b>		
10.5.1.1.1#1	NT	A DP IN Adapter shall pack the active pixel data of a TU into either one or two TU Sets.
10.5.1.1.1#2	NT	When EOC control link symbols are present in a TU, a DP IN Adapter shall pack the EOC symbols using the same scheme as for active pixel symbols.



10.5.1.1.1#	NT	The EOC symbols shall be packed in their 8-bit value representation (DCh).
10.5.1.1.1#	NT	Each TU Set shall be prepended with a TU Set Header.
10.5.1.1.1#	NT	The header in Figure 10-26(A) shall be used for a TU Set that contains a TU with no EOC Symbol.
10.5.1.1.1#	NT	The header in Figure 10-26(B) shall be used for a TU Set that contains a TU with an EOC symbol.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the TU Set Header.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: <b>Video Count [13:8]</b> : This field shall contain the number of active video symbols per lane. A value of zero represents 64. The total number of active video symbols in the TU Set is equal to (Video Count * Number of Lanes).
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: <b>(No EOC) Fill Count [27:14]</b> : This field shall have the value as defined in 10.5.1.5.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: <b>(EOC) Fill Count [21:14]</b> : This field shall have the value as defined in 10.5.1.5.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: <b>(EOC) EOC Index [27:22]</b> : This field shall contain the index of the EOC symbol inside the TU Set. Symbols within a TU Set are indexed starting with zero (for the first symbol) and ending with (Video Count – 1) for the last symbol.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: <b>L [Bit 28]</b> : Last TU Flag. This flag shall be set to 1b if the TU is the last TU Set of a line. Otherwise shall be set to 0b.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: <b>RSV [30:29]</b> : Reserved.
10.5.1.1.1#	NT	The fields forming the TU Set Header shall be as defined below: <b>RSV [30:29]</b> : Reserved.
<b>10.5.1.1.2 Packet Format</b>		
10.5.1.1.2#1	NT	A Video Data Packet shall have the format shown in Figure 10-28.
10.5.1.1.2#2	NT	All TU Set headers within the Video Data Packet payload shall be aligned to 32-bits by adding padding bytes at the end of the TU set payload if necessary.

10.5.1.1.2#3	NT	A DP IN Adapter shall follow the rules below when constructing a Video Data Packet: A Video Data Packet shall contain at least 1 TU Set and no more than 16 TU Sets. If a TU cannot fit within a single Video Data Packet, it shall be split into two TU sets.
10.5.1.1.2#4	NT	A DP IN Adapter shall follow the rules below when constructing a Video Data Packet: When a TU is split into two TU Sets, the remainder of the active pixel symbols shall be sent in the first TU Set in the next Video Data Packet. The <i>Fill Count</i> field in the TU Set Header of the second Video Data Packet for a TU that is split into multiple Video Data Packets shall be set to 0.
10.5.1.1.2#5	NT	A DP IN Adapter shall follow the rules below when constructing a Video Data Packet: The length of all TU Set Padding is included when calculating the <i>Length</i> field in the Tunneled Packet header.
<b>10.5.1.2 Main Stream Attribute Packet</b>		
10.5.1.2#1	NT	A Main Stream Attribute Packet shall consist of an MSA header followed by packet payload.
10.5.1.2#2	NT	The packet payload shall contain the encoding of the 36-byte attribute information following the <SS, SS> control symbol pair.
10.5.1.2#3	NT	The fields forming an MSA Header shall be as defined below: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the MSA Header.
10.5.1.2#	NT	The fields forming an MSA Header shall be as defined below: <b>Fill Count [24:8]</b> : This field shall contain the fill count as defined in Section 10.5.1.5.
10.5.1.2#	NT	The fields forming an MSA Header shall be as defined below: <b>Reserved [31:25]</b> : Reserved.
10.5.1.2#	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Verify the <i>ECC</i> field in the MSA header. If an uncorrectable error has occurred, the Main Stream Attribute Packet shall be dropped and ignored.
10.5.1.2#	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Send Fill Count number of Stuffing Symbols on all lanes of the DP Main-Link according to Section 10.5.1.5.
10.5.1.2#	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Send the control symbol pair <SS, SS> on all lanes of the DP Main-Link.
10.5.1.2#	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Send the stream attribute information contained in the first 36 bytes of the payload of the Main Stream Attribute Packet by steering bytes from the payload onto the lanes of the DP Main-Link in a round robin fashion starting with lane 0.

10.5.1.2#	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Send the control symbol <SE> on all lanes of the DP Main-Link.
<b>10.5.1.3 Blank Start Packet</b>		
10.5.1.3#1	NT	A Blank Start Packet shall consist of a Blank Start header followed by packet payload.
10.5.1.3#2	NT	The packet payload shall contain the encoding of all 4 sets of <VB-ID, Mvid 7:0, Maud 7:0>.
10.5.1.3#3	NT	The fields forming the Blank Start header shall be as defined below: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the Blank Start Header.
10.5.1.3#4	NT	The fields forming the Blank Start header shall be as defined below: <b>Fill Count [24:8]</b> : This field shall have the value as defined in Section 10.5.1.5.
10.5.1.3#5	NT	The fields forming the Blank Start header shall be as defined below: <b>Reserved [29:25]</b> : Reserved.
10.5.1.3#6	NT	The fields forming the Blank Start header shall be as defined below: <b>CP [30]</b> : Content Protection Flag shall be set to 1b if Blank Start DP Control Link Symbols sequence were <BS,CP,CP,BS> or <SR,CP,CP,SR>.
10.5.1.3#7	NT	The fields forming the Blank Start header shall be as defined below: <b>SR [31]</b> : Scrambler Reset Flag shall be set to 1b if Blank Start DP Control Link Symbols sequence were <SR,BF,BF,SR> or <SR,CP,CP,SR>.
10.5.1.3#8	NT	Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations: 1) Verify the <i>ECC</i> field at the Blank Start Header. If an uncorrectable error has occurred, the Blank Start Packet shall be dropped.
10.5.1.3#9	NT	Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations: 2) Generate Stuffing Symbols on each lane of the DP Main-Link according to the <i>Fill Count</i> field in the Blank Start Header and Section 10.5.1.5.
10.5.1.3#10	NT	Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations: 3) Generate control symbols on each lane of the DP Main-Link marking the start of the blanking period based on the <i>SR Flag</i> and <i>CP Flag</i> as shown in Table 10-12.
10.5.1.3#11	NT	Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations: 4) Steer the three double-words of Blank Start Packet payload starting with the second double-word onto the Main-Link by interleaving a byte at a time onto the lanes of the DP Main-Link starting with lane 0.

10.5.1.4 Secondary Data Packet		
10.5.1.4.1 Secondary Transfer Unit		
10.5.1.4.1#1	NT	A DP IN Adapter shall pack secondary data into one or more Secondary Tus.
10.5.1.4.1#	NT	Each Secondary TU shall be prepended with a Secondary TU Header.
10.5.1.4.1#	NT	The fields forming the Secondary TU Header shall be as defined below: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the Secondary TU Header.
10.5.1.4.1#5	NT	The fields forming the Secondary TU Header shall be as defined below: <b>Secondary Count [13:8]</b> : This field shall contain the number of secondary data symbols per lane. A value of zero represent 64 if ND bit equals 0. The total number of secondary data symbols in the Secondary TU is equal to (Secondary Count * Number of Lanes).
10.5.1.4.1#6	NT	The fields forming the Secondary TU Header shall be as defined below: <b>Fill Count [27:14]</b> : This field shall have the value as defined in Section 10.5.1.5. When both the <i>NSS</i> and <i>NSE</i> fields are 0b, the <i>Fill Count</i> field is extended by one bit and is constructed as {EFC, Fill Count} where EFC is the most significant bit.
10.5.1.4.1#7	NT	The fields forming the Secondary TU Header shall be as defined below: <b>L [Bit 28]</b> : Last TU Flag. This flag shall be set to 1b if the Secondary TU is either the last TU before a split or the TU represents the Secondary End Symbol. Otherwise it shall be set to 0b.
10.5.1.4.1#8	NT	The fields forming the Secondary TU Header shall be as defined below: <b>NSE [Bit 29]</b> : No Secondary End. This bit shall be set to 1b if Last TU Flag is set to 1b and a Secondary End Control symbol is not present at the DP Main-link. Otherwise it shall be set to 0b.
10.5.1.4.1#9	NT	The fields forming the Secondary TU Header shall be as defined below: <b>NSS [Bit 30]</b> : No Secondary Start. This bit shall be set to 1b if this is the first Secondary TU after a non-Secondary Tunneled Packet and a Secondary Start Control symbol is not present at the DP Main-Link. Otherwise it shall be set to 0b.
10.5.1.4.1#10	NT	The fields forming the Secondary TU Header shall be as defined below: <b>EFC/ND [31]</b> : Extended Fill Count/No Data. This bit shall be set to 1b if the Secondary TU does not have any Secondary data.
10.5.1.4.1#11	NT	The fields forming the Secondary TU Header shall be as defined below: <b>EFC</b> : When both the <i>NSS</i> and <i>NSE</i> fields are 0b, this bit is used as an extension to the Fill Count field.

10.5.1.4.1#12	NT	The fields forming the Secondary TU Header shall be as defined below: <b>ND:</b> When either the <i>NSS</i> or <i>NSE</i> fields are 1b, this bit is used to indicate whether or not the Secondary TU has any Secondary data. This bit shall be set to 1b if the Secondary TU does not contain Secondary data. If the Secondary TU contains Secondary data, this bit shall be set to 0b.
10.5.1.4.1#13	NT	A DP IN Adapter shall start packing secondary data into a Secondary TU in the following cases: A single Secondary Start Control symbol <SS> is present on the DP Main-link.
10.5.1.4.1#14	NT	A DP IN Adapter shall start packing secondary data into a Secondary TU in the following cases: The previous Secondary TU has reached the maximum capacity and the secondary data continues.
10.5.1.4.1#15	NT	A DP IN Adapter shall start packing secondary data into a Secondary TU in the following cases: The secondary data is split (as defined by the DisplayPort 1.4a Specification) by a non-Secondary Data Packet and this packet has now ended.
10.5.1.4.1#16	NT	A DP IN Adapter shall stop packing secondary data into a Secondary TU upon one of the following cases: Secondary End Control symbol <SE> is present on the DP Main-link.
10.5.1.4.1#17	NT	A DP IN Adapter shall stop packing secondary data into a Secondary TU upon one of the following cases: Maximum capacity is reached: For 1-Lane and 2-Lanes links: maximum capacity is reached when the <i>Secondary Count</i> field is 64; For 4-Lane links: maximum capacity is reached when the <i>Secondary Count</i> field is 62.
10.5.1.4.1#18	NT	A DP IN Adapter shall stop packing secondary data into a Secondary TU upon one of the following cases: Secondary data stream was split by MSA, BS or Active video as defined in the DisplayPort 1.4a Specification.
10.5.1.4.1#19	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 1) Verify the <i>ECC</i> field in the Secondary TU Header. If an uncorrectable error has occurred, the whole Secondary TU and the subsequent TUs within that packet shall be dropped and ignored.
10.5.1.4.1#20	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 2) Send Fill Count number of Stuffing Symbols on all lanes of the DP Main-Link according to Section 10.5.1.5.
10.5.1.4.1#21	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 3) If this Secondary TU is the first Secondary TU to follow a non-Secondary Data Packet and the <i>NSS</i> bit is not set in the Secondary TU Header, send the control symbol <SS> on all lanes of the DP Main-Link.

10.5.1.4.1#22	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 4) Send the secondary data contained in the Secondary TU. The number of cycles of data shall be as according to the <i>Secondary Count</i> field in the Secondary TU Header. The secondary data shall be sent on the DP Main-Link by steering bytes from the payload onto the lanes in a round robin fashion starting with lane 0.
10.5.1.4.1#23	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 5) If the <i>L Flag</i> is set and the <i>NSE</i> bit is not set in the Secondary TU header, send the control symbol <SE> on all lanes of the DP Main-Link.
<b>10.5.1.4.2 Packet Format</b>		
10.5.1.4.2#1	NT	A Tunneled Secondary Data Packet shall have the format shown in Figure 10-34.
10.5.1.4.2#2	NT	A Tunneled Secondary Data Packet shall not include Secondary TUs from more than one DisplayPort SDP.
10.5.1.4.2#3	NT	All Secondary TU Headers within the Tunneled Secondary Data Packet payload shall be aligned to 32-bits by adding Secondary TU Padding bytes at the end of the Secondary TU payload if necessary.
<b>10.5.1.4.3 Secondary Data to Secondary TU Mapping Examples</b>		
<b>10.5.1.5 Fill Count</b>		
10.5.1.5#1	NT	DP IN Adapter shall calculate the <i>Fill Count</i> field according to the following formula: <i>Fill Count</i> field = Act_Fill_Count + DP_K_Prev_Pkt – Prev_Factor
10.5.1.5#2	NT	The following cycles shall be counted as the Act_Fill_Count: Stuffing Symbols; BE - Blanking End; FS - Filling Start; FE - Filling End.
10.5.1.5#3	NT	A DP OUT Adapter shall use the following formula to calculate the actual number of Stuffing Symbols to be driven over the DP link: Act_Fill_Count = <i>Fill Count</i> field + Prev_Factor – DP_K_Prev_Pkt
10.5.1.5#4	NT	A DP OUT Adapter shall ignore the <i>Fill Count</i> field in the first Tunneled Packet sent on the Main-Link Path after DP link training.
<b>10.5.2 MST Tunneling</b>		
<b>10.5.2.1 Sub-MTP TU</b>		
10.5.2.1#1	NT	A Sub-MTP TU Header shall have the format shown in Figure 10-38.
10.5.2.1#2	NT	The fields forming the Sub-MTP TU Header shall be as defined below: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [23:8] of the Sub-MTP TU Header.

10.5.2.1#3	NT	The fields forming the Sub-MTP TU Header shall be as defined below: <b>Data Count[13:8]</b> : This field shall contain the number of Data symbols per lane. The total number of Data symbols in the Sub-MTP TU is equal to ( <i>Data Count</i> * Number of Lanes).
10.5.2.1#4	NT	The fields forming the Sub-MTP TU Header shall be as defined below: <b>Type[17:14]</b> : This field shall contain the Type encoding of the Sub-MTP TU.
10.5.2.1#5	NT	The fields forming the Sub-MTP TU Header shall be as defined below: <b>Slot Number[23:18]</b> : This field shall contain the first slot number in the MTP which this Sub-MTP TU Header is describing.
10.5.2.1#6	NT	A DP IN Adapter that receives an MST stream shall perform the DisplayPort PHY layer and De-scrambler functions defined in the DisplayPort 1.4a Specification.
10.5.2.1#7	NT	Upon reception of the first SR after link training completion, a DP IN Adapter shall: Track the total number of allocated MST slots by snooping any DPCD AUX transactions that configure the VC Payload ID Table.
10.5.2.1#8	NT	Upon reception of the first SR after link training completion, a DP IN Adapter shall: Start mapping MTP from the DP Main-Link into Sub-MTP TUs.
10.5.2.1#9	NT	When a Parameter includes a Data byte, the DP IN Adapter shall append the de-scrambled Data byte as the Parameter.
10.5.2.1#10	NT	A DP IN Adapter shall pack the Data bytes by selecting a byte from each Lane of the Main-Link in a cyclic way, starting with lane 0.
10.5.2.1#11	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: A Sub-MTP TU is byte-aligned.
10.5.2.1#12	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: The total length of a Sub-MTP TU (Header + Parameter Bytes + Data Bytes) does not exceed 252 Bytes.
10.5.2.1#13	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: Slot 0 always starts a new Sub-MTP TU.
10.5.2.1#14	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: A Sub-MTP TU includes data from one MTP only.
10.5.2.1#15	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: A DP IN Adapter shall map an MTP into the minimum possible number of Sub-MTP TU.
10.5.2.1#16	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: A Sub-MTP TU shall be split into 2 Sub-MTP TUs if it does not fit into an MTP packet according to Section 10.5.2.3.

10.5.2.2 MTP to Sub-MTP TU Examples		
10.5.2.2.2 Shifting SR		
10.5.2.2.2#1	NT	Upon detecting a sequence of four consecutive SR with 216 time-slot intervals, a DP IN Adapter shall switch to the new SR location.
10.5.2.2.2#2	NT	The first three SR that are not at Slot Zero's original location shall be mapped to a non-zero Slot Type 8 (1 K-Symbol), for the case of 1-lane, carrying Parameter byte = 8 (as defined in Table 10-17).
10.5.2.2.2#3	NT	The fourth SR shall be mapped to a non-zero Slot Type 1 (Shifting SR) forcing the next slot to be slot number 1.
10.5.2.2.2#4	NT	For the case of 2-Lane DP links, the first three SR shall be mapped to Type 9 (2 K-Symbols).
10.5.2.2.2#5	NT	For the case of and 4-Lane DP links, the first three SR shall be mapped to Type 11 (4 K-Symbols).
10.5.2.2.3 ACT		
10.5.2.2.4 SF and VCPF		
10.5.2.2.4#1	NT	A DP IN Adapter shall not map a SF sequence into a Sub-MTP TU unless the SF sequence comes immediately after a VCPF sequence.
10.5.2.3 MST Packet Format		
10.5.2.3#1	NT	An MST Packet shall have the format shown in Figure 10-46.
10.5.2.3#2	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: The first 3 bytes of the MST Packet payload contains the first Sub-MTP TU Header.
10.5.2.3#3	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: When concatenating two Sub-MTP TUs, the first TU is not be padded.
10.5.2.3#4	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: The maximum number of MTPs packed into one MST Packet does not exceed 17.
10.5.2.3#5	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: The <i>Length</i> field in the Tunneled Packet Header does not include padding bytes.
10.5.2.3#6	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: The Payload of the Tunneled Packet shall be between 230 and 252 Bytes (inclusive), unless the Payload contains at least 16 MTPs.



<b>10.5.2.4 MST Packets to DP MTP</b>		
10.5.2.4#1	NT	A DP OUT Adapter shall analyze each Sub-MTP TU Header and recreate the MTP K-Code and data bytes according to Table 10-16 (for slot zero) or Table 10-17 (for non-zero slots).
10.5.2.4#2	NT	If a DP OUT Adapter has a slot for which it lacks sufficient information to recreate the MTP K-Code and/or data bytes, it shall follow the rules below: If the last Sub-MTP TU Header was VCPF, insert VCPF.
10.5.2.4#3	NT	If a DP OUT Adapter has a slot for which it lacks sufficient information to recreate the MTP K-Code and/or data bytes, it shall follow the rules below: If the last Sub-MTP TU Header was Unallocated, insert unallocated (data bytes equal zero).
10.5.2.4#4	NT	If a DP OUT Adapter has a slot for which it lacks sufficient information to recreate the MTP K-Code and/or data bytes, it shall follow the rules below: For all other cases, insert SF.
10.5.2.4#5	NT	After creating the MTPs, the DP OUT Adapter shall follow all the PHY Layer functions required functions by the DisplayPort 1.4a Specification.
<b>10.5.3 FEC</b>		
<b>10.5.3.1 SR Count</b>		
10.5.3.1#1	NT	A DP Adapter shall implement the SR Count counter, which counts the number of cycles that have elapsed since the last SR.
10.5.3.1#2	NT	A DP IN Adapter shall initiate the SR Count at the first cycle after receiving an SR.
10.5.3.1#3	NT	A DP OUT Adapter shall initiate the SR Count at the first cycle after transmitting an SR.
<b>10.5.3.2 DP IN Adapter Requirements</b>		
10.5.3.2#1	NT	A DP IN Adapter shall: Implement FEC Decoding as defined in the DisplayPort 1.4a Specification.
10.5.3.2#2	NT	A DP IN Adapter shall: Construct an FEC_DECODE Packet as defined in Section 10.5.3.4 upon FEC_DECODE_EN or FEC_DECODE_DIS sequence detection.
10.5.3.2#3	NT	A DP IN Adapter shall: The Adapter Layer shall prioritize the FEC_DECODE Packet over all other Main-Link Path packets when pass it to the Transport Layer.
10.5.3.2#4	NT	A DP IN Adapter shall not: Tunnel any FEC-related symbols including FEC_PARITY_MARKER, FEC_DECODE & FEC_PARITY_PH.

10.5.3.2#5	NT	A DP IN Adapter shall not: Count the Link cycles of FEC Symbols for fill count purposes.
<b>10.5.3.3 DP OUT Adapter Requirements</b>		
10.5.3.3#1	NT	A DP OUT Adapter shall: Implement FEC Encoding as defined in the DisplayPort 1.4a Specification.
10.5.3.3#2	NT	A DP OUT Adapter shall: Apply majority voting for the repeated fields with in the FEC_DECODE Packet: SR Count; FEN; FDS.
10.5.3.3#3	NT	A DP OUT Adapter shall: Generate FEC_DECODE_EN and FEC_DECODE_DIS upon reception of a FEC_DECODE Packet.
10.5.3.3#4	NT	FEC_DECODE_EN sequence shall be generated if <i>FEN</i> field in the FEC_DECODE Packet is 1b.
10.5.3.3#5	NT	FEC_DECODE_DIS sequence shall be generated if <i>FDS</i> fields in the FEC_DECODE Packet is 1b.
10.5.3.3#6	NT	The first symbol of the FEC_DECODE_EN and FEC_DECODE_DIS sequences shall be transmitted according to the <i>SR Count</i> field of the FEC_DECODE Packet, i.e. the FEC_DECODE_EN and FEC_DECODE_DIS sequence shall be transmitted <i>SR Count</i> link clock cycles after the most recently transmitted SR.
10.5.3.3#7	NT	When a FEC_DECODE Packet is received, a DP OUT Adapter compares the Packet SR Count and the Counter SR Count as follows: If Packet SR Count > Counter SR Count the DP OUT Adapter waits for the Counter SR Count to be equal to Packet SR Count then generate the FEC sequence.
10.5.3.3#8	NT	When a FEC_DECODE Packet is received, a DP OUT Adapter compares the Packet SR Count and the Counter SR Count as follows: Else, a DP OUT Adapter waits for next SR to be transmitted, then waits for the Counter SR Count to be equal to Packet SR Count then generate the FEC sequence.
10.5.3.3#9	NT	A DP OUT Adapter shall not: Count the Link cycles of FEC Symbols for fill count purposes.
<b>10.5.3.4 FEC_DECODE Packet</b>		
10.5.3.4#1	NT	A FEC_DECODE Packet shall have the format shown in Figure 10-47.
10.5.3.4#2	NT	The <i>PDF</i> field in the header shall be set to 7 and the <i>Length</i> field shall be 14h.
10.5.3.4#3	NT	An FEC Command shall have the format defined in Figure 10-48.
10.5.3.4#4	NT	The three FEC Commands in an FEC_DECODE Packet shall be identical to each other.

10.5.3.4#5	NT	The fields in an FEC Command shall contain the following: <b>SR Count [29:0]</b> : This field contains the number of DP Link clock cycles between the last received SR and the first FEC_DECODE_EN or FEC_DECODE_DIS sequences. The minimum value for this field is 1h. (occurs when SR is immediately followed by FEC_DECODE sequence).
10.5.3.4#6	NT	The fields in an FEC Command shall contain the following: <b>FEC DISABLE (FDS) [30]</b> : This field shall be set to 1b if a FEC_DECODE_DIS sequence was detected. In all other cases it shall be set to 0b.
10.5.3.4#7	NT	The fields in an FEC Command shall contain the following: <b>FEC ENABLE (FEN) [31]</b> : This field shall be set to 1b if a FEC_DECODE_EN sequence was detected. In all other cases it shall be set to 0b.
<b>10.5.4 DP OUT Adapter Buffer</b>		
10.5.4#1	NT	A DP OUT Adapter shall implement a buffer that can be used to compensate for the jitter in the latency of the received Tunneled Packets.
10.5.4#2	NT	Deprecated.
10.5.4#3	NT	The DP OUT Adapter transitions from sending self-generated idle pattern to reconstructing the DP Main-Link from the Tunneled Packets after completing the following steps: 1) The DP OUT Adapter shall adjust the PLL frequency at least once as a result of an Adjust PLL event as described in Section 10.6.
10.5.4#4	NT	The DP OUT Adapter transitions from sending self-generated idle pattern to reconstructing the DP Main-Link from the Tunneled Packets after completing the following steps: 2) The DP OUT Adapter ensures, in an implementation specific manner, that within eight PLL frequency adjustments the link symbol clock frequency difference between its own and the DPTX is such that buffer overflow and buffer underrun is avoided.
10.5.4#5	NT	The DP OUT Adapter transitions from sending self-generated idle pattern to reconstructing the DP Main-Link from the Tunneled Packets after completing the following steps: 3) The DP OUT Adapter shall wait to receive an SR from the DP IN Adapter.
10.5.4#6	NT	All Main-Link Path Tunneled Packets, besides DP Clock Sync Packets, are dropped by the DP OUT Adapter until reception of the SR.
10.5.4#7	NT	After the next step is completed, the received SR, shall be the first symbol driven by the DP OUT Adapter as the reconstructed Main-link.
10.5.4#8	NT	The DP OUT Adapter transitions from sending self-generated idle pattern to reconstructing the DP Main-Link from the tunneled packets after completing the following steps: 4) The DP OUT Adapter delays sending the SR in Step 3 for a number of Accumulation Cycles.

10.5.4#9	NT	During the delay, the DP OUT Adapter shall accumulate the DP Main-Link traffic from the DP IN Adapter.
<b>10.5.4.1 Buffer Operation</b>		
10.5.4.1#1	NT	If the buffer becomes empty, a DP OUT Adapter shall continue to drive Dummy Symbols on the DP Main Link, assuming that the next Main-Link Path Tunneled Packet holds a Fill Count value larger than the driven Dummy Cycles.
<b>10.5.4.2 Accumulation Cycles</b>		
10.5.4.2#1	NT	A DP OUT Adapter shall report the Maximum Accumulation Cycles it performs.
<b>10.5.5 HDCP</b>		
10.5.5#1	NT	A DP IN Adapter shall not perform HDCP decryption.
10.5.5#2	NT	It shall not drop or modify an AUX Request or AUX Response associated with HDCP functionality.
10.5.5#3	NT	A DP OUT Adapter shall not perform HDCP encryption.
<b>10.6 DP Link Clock Sync</b>		
<b>10.6.1 Synchronization Method</b>		
<b>10.6.1.1 Events</b>		
<b>10.6.1.1.1 Measuring Events</b>		
<b>10.6.1.1.2 Adjust PLL Event</b>		
<b>10.6.1.2 Lifetime Counter</b>		
10.6.1.2#1	NT	A DP OUT Adapter shall start counting as soon as Link Symbol clock is stable for starting link training with DPRX.
10.6.1.2#2	NT	A DP IN Adapter shall start counting as soon as it completed its equalization process.
10.6.1.2#3	NT	In order to filter out the variation introduced by spread-spectrum modulation, the LC shall be filtered using a first order IIR filter.
10.6.1.2#4	NT	The filtering operation shall be done with 8-bit truncation at the fraction part to assure reproducible result.
10.6.1.2#5	NT	All operands of IIR filter shall have the same format of 64 bits of integer followed by 8 bits of fraction.

10.6.1.3 DP Clock Sync Packet		
10.6.1.3#1	NT	A DP Clock Sync Packet shall have the format shown in Figure 10-53.
10.6.1.3#2	NT	The fields forming a DP Clock Sync Packet shall be as defined below: <b>Reserved:</b> This field is reserved and shall be set to 0.
10.6.1.3#3	NT	The fields forming a DP Clock Sync Packet shall be as defined below: <b>Window Count:</b> This field is defined in Section 10.6.2.1. The <i>Window Count</i> field structure is shown in Figure 10-52(A).
10.6.1.3#4	NT	The fields forming a DP Clock Sync Packet shall be as defined below: <b>FLC:</b> This field contains the snapshot of the Filtered Lifetime Counter at the time the Window Measured Event occurred.
10.6.1.3#5	NT	The fields forming a DP Clock Sync Packet shall be as defined below: <b>CRC32:</b> This field contains a CRC32 computed over the entire payload using the following DW order: DW1, DW3, DW2, DW7, DW6, DW5, DW4. The following CRC shall be used: Width: 32; Poly: 1EDC 6F41h; Init: FFFF FFFFh; RefIn: True; RefOut: True; XorOut: FFFF FFFFh.
10.6.2 DP Adapter Requirements		
10.6.2.1 DP IN Adapter Requirements		
10.6.2.1#1	NT	A DP IN Adapter shall: Implement a Lifetime Counter as described in Section 10.6.1.1.2.
10.6.2.1#2	NT	A DP IN Adapter shall: Implement the logic to perform the LC filtering.
10.6.2.1#3	NT	A DP IN Adapter shall: Update FLC upon an Update Counter Event.
10.6.2.1#4	NT	A DP IN Adapter shall: Upon the first Measure Window Event: Capture the current FLC; Store the current captured FLC to be used as previous captured FLC at the next Measure Window Even.
10.6.2.1#5	NT	A DP IN Adapter shall: Upon each subsequent Measure Window Event: Capture the current FLC; Compute the Window Count by calculating the current captured FLC minus the FLC that was captured at the previous Measure Event; Construct a DP Clock Sync Packet and send it over the Main-Link Path within tDPClockSync after the Measure Window Event; Store the current captured FLC to be used as previous captured FLC at the next Measure Window Event.
10.6.2.2 DP OUT Adapter Requirements		
10.6.2.2#1	NT	A DP OUT Adapter shall: Implement a Lifetime Counter as described in Section 10.6.1.2.
10.6.2.2#2	NT	A DP OUT Adapter shall: Implement the logic to perform the LC filtering.
10.6.2.2#3	NT	A DP OUT Adapter shall: Update FLC upon an Update Counter Event.

10.6.2.2#4	NT	A DP OUT Adapter shall: Upon a Measure Window Event: Capture the current FLC; Compute the Window Count as described in Section 10.6.1.3.
10.6.2.2#5	NT	A DP OUT Adapter shall: Upon receiving a DP Clock Sync Packet after the Measure Window Event and before the PLL Adjust Event, compute the PLL frequency adjustment. The method for computing the PLL frequency adjustment is outside the scope of this specification.
10.6.2.2#6	NT	A DP OUT Adapter shall: Upon an Adjust PLL Event, adjust the PLL frequency based on the computation performed at the Measure Window Event.
10.6.2.2#7	NT	If a DP OUT Adapter receives a DP Clock Sync Packet after an Adjust PLL Event but before the next Measure Window Event, it shall not adjust the PLL and shall silently discard the packet.
10.6.2.2#8	NT	If a DP OUT Adapter receives a DP Clock Sync Packet before it computed the first Window Count, it shall not adjust the PLL and shall silently discard the packet.
10.6.2.2#9	NT	When a DP OUT Adapter changes the DisplayPort Main-Link transmitter frequency as a result of adjusting the PLL frequency, it shall adhere to the DisplayPort 1.4a Specification.
10.6.2.2#10	NT	The PLL frequency adjustment shall be completed within tDPPLLAdjust after the Adjust PLL Event.
<b>10.7 DP BW Allocation Mode</b>		
10.7#1		If a DP IN Adapter supports DP BW Allocation Mode, it shall do so as defined in this section.
<b>10.7.1 DP BW Allocation Mode Enablement</b>		
10.7.1#1		If a DP IN Adapter supports DP BW Allocation Mode, it shall: Set the DP_LOCAL_CAP.DP_IN_BW_Allocation Mode Support bit to 1b.
10.7.1#2		If a DP IN Adapter supports DP BW Allocation Mode, it shall: Update the AUX Response for DPCD DP TUNNELING and PANEL REPLAY OPTIMIZATION SUPPORT. DP_IN_BW_Allocation_Mode_Support (E000Dh, bit 7) to 1b.
10.7.1#3		If a DP IN Adapter supports DP BW Allocation Mode, it shall: Update the AUX Response for DPCD USB4_DRIVER_BW_CAPABILITY.USB4_Driver_BW Allocation Mode Support (E0020h, bit 7) to have the same value as ADP_DP_CS_2.CM BW Allocation Mode Support.

10.7.1#4		When a Connection Manager changes ADP_DP_CS_2.CM BW Allocation Mode Support bit, a DP IN Adapter shall: Set the BW_Allocation_Capability_Changed field to 1b in DP_TUNNELING_STATUS DPCD register.
10.7.1#5		When a Connection Manager changes ADP_DP_CS_2.CM BW Allocation Mode Support bit, a DP IN Adapter shall: Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h)
10.7.1#6		When a Connection Manager changes ADP_DP_CS_2.CM BW Allocation Mode Support bit, a DP IN Adapter shall: If Unmask_BW_Allocation_IRQ is 1b, generate an IRQ_HPDP.
10.7.1#7		When DPTX sets DPTX_BW_ALLOCATION_MODE_CONTROL.DP_Display_Driver_BW_Allocation_Mode_Enable (E0030h, bit 7) to 1b, a DP IN Adapter shall: Enable DP BW Allocation Mode.
10.7.1#8		When DPTX sets DPTX_BW_ALLOCATION_MODE_CONTROL.DP_Display_Driver_BW_Allocation_Mode_Enable (E0030h, bit 7) to 1b, a DP IN Adapter shall: Send the Connection Manager a Notification Packet with Event Code = DP_BW as defined in Table 6-11.
<b>10.7.2 Interaction with DPTX</b>		
10.7.2#1		When a DP IN Adapter receives a DPCD AUX Write transaction that targets a DPCD register within Table 10-23, and the targeted DPCD field Type is Read/Write, it shall update the corresponding field in Adapter configuration space with the value of the write transaction.
10.7.2#2		When a DP IN Adapter receives a DPCD AUX Read transaction that targets a DPCD register within Table 10-23, and the targeted DPCD field Type is Read Only, it shall update the read transaction with the value in the corresponding field in Adapter Configuration Space.
10.7.2#3		When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW register, a DP IN Adapter shall: Store the current Allocated BW in an internal variable.
10.7.2#4		When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW register, a DP IN Adapter shall: If the recovery timer is advancing, stop and reset it.
10.7.2#5		When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW register, a DP IN Adapter shall: Initiate a bandwidth request handshake with the Connection Manager as defined in Section 10.7.3.

10.7.2#6		When a Connection Manager writes a value to the Allocated BW field that is equal to or greater than the Requested BW, a DP IN Adapter shall: Set the BW Request Succeeded field to 1b in DP_TUNNELING_STATUS DPCD register.
10.7.2#7		When a Connection Manager writes a value to the Allocated BW field that is equal to or greater than the Requested BW, a DP IN Adapter shall: Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h).
10.7.2#8		When a Connection Manager writes a value to the Allocated BW field that is equal to or greater than the Requested BW, a DP IN Adapter shall: If Unmask_BW_Allocation_IRQ is 1b, generate an IRQ_HPDP.
10.7.2#9		When a Connection Manager writes a value to the Allocated BW field that is equal to or greater than the Requested BW, a DP IN Adapter shall: If the ESTIMATED_BW field was locked for updates due to bandwidth request failure, unlock it.
10.7.2#10		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: Set the ESTIMATED_BW field to the Allocated BW, and lock its value (i.e. ignore any changes in the Estimated_BW field).
10.7.2#11		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: Set the BW Request Failed to 1b in DP_TUNNELING_STATUS DPCD register.
10.7.2#12		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h).
10.7.2#13		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: If Unmask_BW_Allocation_IRQ is 1b, generate an IRQ_HPDP.
10.7.2#14		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: Start the recovery timer.
10.7.2#15		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: If the recovery timer has reached tDPBWRecoveryTimeout, the DP IN Adapter initiates a bandwidth allocation request. The DP BW that a DP IN Adapter requests shall be the same bandwidth as before the failed bandwidth allocation (i.e. the same value as in the Allocated BW field before the DPTX last updated the DPCD Requested BW register).



<b>10.7.2.1 Estimated Bandwidth</b>		
10.7.2.1#1		Upon a change in the Estimated BW field, a DP IN adapter shall: Set Estimated BW Changed bit in the DPCD DP_TUNNELING_STATUS register to 1b.
10.7.2.1#2		Upon a change in the Estimated BW field, a DP IN adapter shall: Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_
10.7.2.1#3		Upon a change in the Estimated BW field, a DP IN adapter shall: If Unmask_BW_Allocation_IRQ is 1b, generate an IRQ_HPD.
<b>10.7.3 Interaction with the Connection Manager</b>		
10.7.3#1		When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW field, a DP IN Adapter shall: 1)Set the ADP_DP_CS_8.DPTX Req field to 1b; 2) Send the Connection Manager a Notification Packet with Event Code = DP_BW as defined in Table 6-11; 3)Wait for the Connection Manager to set the ADP_DP_CS_2.CM Ack bit to 1b; 4) Set the ADP_DP_CS_8.DPTX Req field to 0b.
<b>10.8 Timing Parameters</b>		

## Chapter 13 Assertions

Assertion #	How to Test	Assertion Description
<b>13 TBT3 Compatibility</b>		
<b>13.8.1.1 DP IN Adapter Requirements</b>		
13.8.1.1#1	TBD	A DP IN Adapter operating in TBT3-Compatible mode follows the requirements listed in Section 10.4.4.2.1 except the following: The Link Status DPCD registers, as defined in Table 10-9, shall be mapped statically as Internal registers.
13.8.1.1#2	TBD	A DP IN Adapter operating in TBT3-Compatible mode follows the requirements listed in Section 10.4.4.2.1 except the following: DPCD address 00600h is mapped as Internal register.
13.8.1.1#3	TBD	A DP IN Adapter operating in TBT3-Compatible mode follows the requirements listed in Section 10.4.4.2.1 except the following: An AUX Read Transaction to the LTTPR DPCD Field, addresses F0000h-F02FFh, are mapped as Internal registers. A DP IN Adapter shall set the data of the AUX Response to 0h.
13.8.1.1#4	TBD	A DP IN Adapter operating in TBT3-compatible mode follows the requirements listed in Section 10.4.4.5 except the following: DSC Support field in the DSC SUPPORT DPCD register shall always be set to 0b.
13.8.1.1#5	TBD	A DP IN Adapter operating in TBT3-compatible mode follows the requirements listed in Section 10.4.4.5 except the following: FEC_CAPABLE field in FEC_CAPABILITY DPCD register shall always be set to 0b.

## Ver. 2 Assertions

### Chapter 10 Assertions

The following Table presents the USB4 Specification Chapter 10 asserts.

Assertion #	How to Test	Assertion Description
<b>10 DisplayPort Tunneling</b>		
10#1	TD 10.002	A USB4 host shall support DP tunneling.
10#2	TD 10.002	A Host Router shall contain at least one DP IN Adapter and may optionally contain one or more DP OUT Adapters.
10#3	TD 10.002	A USB4 hub shall support DP Tunneling.
10#4	TD 10.002	A USB4 Hub shall contain at least one DP OUT Adapter and may optionally contain one or more DP IN Adapters.
10#5	NT	If a USB4 peripheral device supports DP Tunneling, it shall contain at least one DP Adapter.
<b>10.1 DP Adapter Port Protocol Stack</b>		
<b>10.1.1 Transport Layer</b>		
<b>10.1.2 Protocol Adapter Layer</b>		
<b>10.1.3 DP Physical Layer</b>		
10.1.3#1	TD 10.002 TD 10.002	A DP Adapter Port shall either implement the DisplayPort Physical Layer as defined in the DisplayPort 1.4a Specification or shall implement its functional equivalent (e.g. DP Adapter Port is connected to a DPRX or a DPTX as part of an SoC).
10.1.3#2	NT	A DP IN Adapter Port which does not implement a Physical Layer shall generate a stream of DisplayPort Tunneled packets as if a Physical Layer exists.
<b>10.2 DP Adapter States</b>		
<b>10.2.1 Reset</b>		
10.2.1#1	TD 10.002 TD 10.002	While in the Reset state, a DP Adapter shall set all Configuration Spaces to their default values.
10.2.1#2	NT	A DP IN Adapter shall drive HPD signal low.
10.2.1#3	NT	A DP OUT Adapter shall not apply DP_PWR.

<b>10.2.2 Present</b>		
10.2.2#1	TD 10.002 TD 10.002	While in the Present state, a DP Adapter shall set its Adapter Configuration Spaces to their default values.
10.2.2#2	NT	A DP IN Adapter Port shall drive HPD signal low.
10.2.2#3	NT	A DP OUT Adapter Port shall not apply DP_PWR.
<b>10.2.3 Plugged</b>		
10.2.3#1	NT	While in the Plugged state, a DP IN Adapter shall drive HPD signal low.
<b>10.2.4 Paired</b>		
10.2.4#1		When a DP Adapter exit this state, it shall set its Adapter Configuration Spaces to their default values.
<b>10.2.5 DPTX Discovery (DP IN Adapter Only)</b>		
10.2.5#1		A DP IN Adapter that supports DPTX Discovery exits this state when the DPTX Discovery Mode bit is set to 0b: If the DP Paths are enabled (AE bit is 1b and VE bit is 1b), the DP Adapter shall transition to Paired state.
10.2.5#2		A DP IN Adapter that supports DPTX Discovery exits this state when the DPTX Discovery Mode bit is set to 0b: If the DP Paths are disabled (AE bit is 0b or VE bit is 0b), the DP Adapter shall transition to Plugged state.
<b>10.3 Interfaces</b>		
<b>10.3.1 DisplayPort</b>		
10.3.1#1	NT	A DP Adapter shall support three modes of operation: <u>LTTPR Non-Transparent</u> – LT-tunable PHY Repeater (Non-Transparent Mode); <u>LTTPR Transparent</u> – LT-tunable PHY Repeater (Transparent Mode); <u>Non-LTTPR</u> – Non-LT-tunable PHY Repeater.
10.3.1#2	NT	After reset, a DP Adapter shall operate in Non-LTTPR mode.
10.3.1#3	NT	A DP Adapter shall transition between the three modes as described in Section 10.4.6.1.
10.3.1#4	NT	A DP Adapter shall transition to Non-LTTPR mode upon exit from the Paired state.
<b>10.3.1.1 LTTPR Non-Transparent</b>		
10.3.1.1#1	NT	A DP IN Adapter shall implement LTTPR UFP.
10.3.1.1#2	NT	A DP OUT Adapter shall implement LTTPR DFP.

<b>10.3.1.2 Non-LTTPR</b>		
10.3.1.2#1	NT	A DP IN Adapter shall implement Non-LTTPR Non-Transparent UFP.
10.3.1.2#2	NT	A DP OUT Adapter shall implement Non-LTTPR Non-Transparent DFP.
<b>10.3.1.3 LTTPR Transparent</b>		
<b>10.3.2 Programming Model</b>		
<b>10.3.2.1 Adapter Configuration Space</b>		
<b>10.3.2.2 Path Configuration Space</b>		
10.3.2.2#1	TD 10.002 TD 10.002	A DP Adapter shall implement a Path Configuration Space as defined in Section 8.2.3.
10.3.2.2#2	NT	A DP Adapter shall support one MAIN-Link Path, one AUX Ingress Path, and one AUX Egress Path.
<b>10.3.3 Hot Plug and Hot Removal Events</b>		
<b>10.3.3.1 DP OUT Adapters</b>		
10.3.3.1#1	NT	When a DP OUT Adapter detects a Plug Event (as defined in the DisplayPort 1.4a Specification), it shall: Send a Hot Plug Event Packet with the UPG bit set to 0b as described in Section 6.8 within tDPPlug.
10.3.3.1#2	NT	When a DP OUT Adapter detects a Plug Event (as defined in the DisplayPort 1.4a Specification), it shall: Set the Plugged bit to 1b.
10.3.3.1#3	NT	When a DP OUT Adapter detects an Unplug Event (as defined in the DisplayPort 1.4a Specification), it shall: Send a Hot Plug Event Packet with the UPG bit set to 1b as described in Section 6.8 within tDPPlug.
10.3.3.1#4	NT	When a DP OUT Adapter detects an Unplug Event (as defined in the DisplayPort 1.4a Specification), it shall: Set the Plugged bit to 0b
<b>10.3.3.2 DP IN Adapters</b>		
10.3.3.2#1	NT	A Router shall send a Hot Plug Event Packet as described in Section 6.8 within tDPPlug of when both of the following are true: A DP IN Adapter detects a Source (as defined in the DisplayPort 1.4a Specification); The DP IN Adapter that detected the Plug Event has sufficient DP stream resources available to support a DP stream.

10.3.3.2#2	NT	A Router shall send a Hot Plug Event Packet with the <i>UPG</i> bit set to 1b as described in Section 6.8 within tDPPlug of when either of the following are true: A DP IN Adapter detects the removal of a Source (as defined in the DisplayPort 1.4a Specification); The Router has freed the DP stream resources allocated to the DP IN Adapter such that the DP IN Adapter can no longer support a DP stream.
<b>10.3.3.2.1 DP Stream Resource Allocation</b>		
10.3.3.2.1#1	NT	A Router shall support the DP Stream Resource Commands listed in Table 10-3 (QUERY_DP_RESOURCE, ALLOCATE_DP_RESOURCE, DEALLOCATE_DP_RESOURCE)
<b>10.3.4 DisplayPort Over USB4 Fabric</b>		
<b>10.3.4.1 DisplayPort Data Packet Types</b>		
10.3.4.1#1	NT	The Tunneled Packets types defined in Table 10-4 shall only be used for the AUX Path.
10.3.4.1#2	NT	The Tunneled Packet Types defined in Table 10-5 shall only be used for the Main-Link Path.
10.3.4.1#3	NT	If a DP Adapter receives a Tunneled Packet on the AUX Path with a PDF value other than 0 to 3, it shall discard the Tunneled Packet and shall not send any Packets in response.
10.3.4.1#4	NT	If a DP OUT Adapter receives a Tunneled Packet on the Main-Link Path with a PDF value other than 1 to Bh, it shall discard the Tunneled Packet and shall not send any Packets in response.
<b>10.3.4.2 AUX Path Packets</b>		
10.3.4.2#1	NT	When generating an AUX Path Packet, a DP Adapter Layer shall put the value in the <i>AUX Tx HopID</i> field into the <i>HopID</i> field of the Tunneled Packet header.
10.3.4.2#2	NT	When a DP Adapter Layer receives a Tunneled Packet with a HopID that is equal to the <i>AUX Rx HopID</i> field, it shall treat that packet as an AUX Path Packet.
<b>10.3.4.2.1 AUX Packets</b>		
10.3.4.2.1#1	NT	An AUX Packet shall have the format shown in Figure 10-6.
10.3.4.2.1#2	NT	The Tunneled Packet Header for an AUX Packet shall have the <i>PDF</i> field set to 0.
10.3.4.2.1#3	NT	AUX Packet payload shall contain the following: <b>CRC</b> : See Section 10.3.4.2.1.1.

10.3.4.2.1#4	NT	AUX Packet payload shall contain the following: <b>AUX Payload</b> : Shall contain the bytes contained between the <SYNC> and <STOP> framing bytes of a DisplayPort AUX transaction. The number of bytes in this field varies between 1 and 20.
10.3.4.2.1#5	NT	AUX Packet payload shall contain the following: <b>Reserved</b> : Shall be one byte set to 00h.
<b>10.3.4.2.1.1 CRC</b>		
10.3.4.2.1.1#1	NT	The CRC32 computation in an AUX Packet shall be based on the following CRC: Width: 32 Poly: 1EDC 6F41h Init: FFFF FFFFh RefIn: True RefOut: True XorOut: FFFF FFFFh
10.3.4.2.1.1#2	NT	If the AUX Payload is less than 21 bytes in length, a DP Adapter shall add the required number of zero-padding bytes for the computation of the CRC.
10.3.4.2.1.1#3	NT	The padding bytes shall not be transmitted in the AUX Packet.
10.3.4.2.1.1#4	NT	The CRC32 shall be generated by the DP Adapter that creates the AUX Packet and shall be checked by the DP Adapter that receives the AUX Packet
10.3.4.2.1.1#5	NT	A DP Adapter that receives an AUX Packet with a CRC error shall drop that packet.
<b>10.3.4.2.2 HPD Packets</b>		
10.3.4.2.2#1	NT	An HPD Packet shall have the format shown in Figure 10-8.
10.3.4.2.2#2	NT	The <i>PDF</i> field in the header shall be set to 1 and the <i>Length</i> field shall be 4.
10.3.4.2.2#3	NT	HPD Packet payload shall contain the following: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the HPD Packet payload.
10.3.4.2.2#4	NT	HPD Packet payload shall contain the following: <b>Reserved [30:8]</b> : Shall be set to 0.
10.3.4.2.2#5	NT	HPD Packet payload shall contain the following: <b>Plug (P) Flag [Bit 31]</b> : Shall be set to 0 if the HPD signal is low for more than 2 ms. Shall be set to 1 if the HPD signal is high.

10.3.4.2.2#6	NT	When a DP IN Adapter receives an HPD Packet, it shall check the <i>ECC</i> field of the packet payload.
10.3.4.2.2#7	NT	The DP IN Adapter shall correct single-bit errors in the HPD Tunneled Packet payload.
10.3.4.2.2#8	NT	If an uncorrectable error is detected, the HPD Packet shall be dropped.
10.3.4.2.2#9	NT	Otherwise the DP IN Adapter shall: Generate a Plug/Re-plug HPD event if the <i>P</i> Flag in the HPD Packet payload is set to 1b.
10.3.4.2.2#10	NT	Otherwise the DP IN Adapter shall: Generate an Unplug HPD event if the <i>P</i> Flag in the HPD Packet payload is set to 0b.
10.3.4.2.2#11	NT	Otherwise the DP IN Adapter shall: Acknowledge the HPD Packet by sending an ACK Packet to the DP OUT Adapter within tDPackResponse of receiving the HPD Packet.
<b>10.3.4.2.3 SET_CONFIG Packet</b>		
10.3.4.2.3#1	NT	If both DP Adapters support Version 2 of the USB4 Specification (DP_COMMON_CAP.Protocol Adapter Version is 5h), then the DP Adapters shall use the Version 2 SET_CONFIG Packet. Otherwise, the DP Adapters shall use the Version 1 SET_CONFIG Packet.
10.3.4.2.3#2	NT	The <i>PDF</i> field in the header shall be set to 2 and the <i>Length</i> field shall be 4.
<b>10.3.4.2.3.1 Version 1 SET_CONFIG Packet</b>		
10.3.4.2.3.1#1		A Version 1 SET_CONFIG Packet shall have the format show in Figure 10-9.
10.3.4.2.3.1#2		A Version 1 SET_CONFIG Packet payload shall contain the following: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the SET_CONFIG Packet payload.
10.3.4.2.3.1#3		A Version 1 SET_CONFIG Packet payload shall contain the following: <b>Link Rate 0 (LR0) [8]</b> : This field is used in combination with the <i>Link Rate 1 (LR1)</i> field as defined below.
10.3.4.2.3.1#4		A Version 1 SET_CONFIG Packet payload shall contain the following: <b>Lane Count (LC) [11:9]</b> : This field shall specify the selected lane count according to the following encodings: 000b: Link Down; 001b: 1 Lane; 010b: 2 Lanes; 100b: 4 Lanes; All other values are reserved.
10.3.4.2.3.1#5		A Version 1 SET_CONFIG Packet payload shall contain the following: <b>Reserved [12]</b> : This field shall be set to 1b by sender and ignored by receiver.



10.3.4.2.3.1#6		A Version 1 SET_CONFIG Packet payload shall contain the following: <b>Link Rate 1 (LR1) [13]</b> : This field is used in combination with the <i>Link Rate 0 (LR0)</i> field where LR = {LR1,LR0}. The LR value shall specify the selected Link rate according to the following encodings: 00b: 1.62 Gbps/lane; 01b: 2.70 Gbps/lane; 10b: 5.40 Gbps/lane; 11b: 8.10 Gbps/lane; This field is only valid when the <i>Lane Count</i> field is greater than 000b.
10.3.4.2.3.1#7		A Version 1 SET_CONFIG Packet payload shall contain the following: <b>Training Pattern Support (TPS) [15:14]</b> : This field shall specify the supported TPS which can be used in EQ Phase in Non-LTTPR and LTTPR Transparent link training.
10.3.4.2.3.1#8		A Version 1 SET_CONFIG Packet payload shall contain the following: <b>MSG Type [22:16]</b> : This field specifies the MSG type of the SET_CONFIG Packet. This field shall carry one of the MSG Type values listed in Table 10-6.
10.3.4.2.3.1#9		A Version 1 SET_CONFIG Packet payload shall contain the following: <b>Version 2(V2) [23]</b> : This bit specifies the format of the SET_CONFIG Packet. This bit shall be set to 0b.
10.3.4.2.3.1#10		A Version 1 SET_CONFIG Packet payload shall contain the following: <b>MSG Data [31:24]</b> : This field holds the MSG Data value that is associated with the specific MSG Type. The MSG Data shall match the MSG Type of the packet as set forth in Table 10-6.
10.3.4.2.3.1#11		A DP IN Adapter shall set the LC and LR fields in all Version 1 SET_CONFIG Packets to be the same as the last SET_LINK SET_CONFIG Packet it sent. The exception to this rule is a SET_LINK SET_CONFIG Packet, which may alter those values as defined in Section 10.4.10.1.1 and Section 10.4.10.2.1.
10.3.4.2.3.1#12		A DP OUT Adapter shall set the LC and LR fields in all Version 1 SET_CONFIG Packets to the same values as in the last SET_LINK SET_CONFIG Packet it received
<b>10.3.4.2.3.2 Version 2 SET_CONFIG Packet</b>		
10.3.4.2.3.2#1		A Version 2 SET_CONFIG Packet shall have the format show in Figure 10-10.
10.3.4.2.3.2#2		A Version 2 SET_CONFIG Packet payload shall contain the following: <b>MSG Data [22:0]</b> : This field holds the MSG Data value that is associated with the specific MSG Type. The MSG Data shall match the MSG Type of the packet as set forth in Table 10-6.
10.3.4.2.3.2#3		A Version 2 SET_CONFIG Packet payload shall contain the following: <b>Version 2(V2) [23]</b> : This bit specifies the format of the SET_CONFIG Packet. This bit shall be set to 1b.

10.3.4.2.3.2#4		A Version 2 SET_CONFIG Packet payload shall contain the following: MSG Type [31:24]: This field specifies the MSG type of the SET_CONFIG Packet. This field shall carry one of the MSG Type values listed in Table 10-6.
<b>10.3.4.2.3.3 SET_CONFIG Packet Processing</b>		
10.3.4.2.3.3#1		After a DP Adapter sends a SET_CONFIG Packet, it shall wait for an ACK Packet with the Type field equal to 0h.
10.3.4.2.3.3#2		After receiving an ACK Packet with the Type field set to 0h, the DP Adapter shall wait tDPSetConfigGap before sending the next SET_CONFIG Packet.
10.3.4.2.3.3#3		When a DP Adapter receives a Version 1 SET_CONFIG Packet, it shall check the ECC field of the packet payload.
10.3.4.2.3.3#4		The DP Adapter shall correct single-bit errors in the Version 1 SET_CONFIG Packet payload.
10.3.4.2.3.3#5		If an uncorrectable error is detected, the Version 1 SET_CONFIG Packet shall be dropped.
10.3.4.2.3.3#6		Otherwise, the DP Adapter shall respond with an ACK Packet with the Type field equal to 0h.
10.3.4.2.3.3#7		The ACK Packet shall be sent within tDPAckResponse of receiving the SET_CONFIG Packet.
<b>10.3.4.2.4 ACK Packet</b>		
10.3.4.2.4#1	NT	An ACK Packet shall have the format shown in Figure 10-10.
10.3.4.2.4#2	NT	The <i>PDF</i> field in the header shall be set to 3 and the <i>Length</i> field shall be 4.
10.3.4.2.4#3	NT	ACK Packet payload shall contain the following: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the ACK Packet payload.
10.3.4.2.4#4	NT	ACK Packet payload shall contain the following: <b>Reserved [27:8]</b> : Shall be set to 0.
10.3.4.2.4#5	NT	ACK Packet payload shall contain the following: Type [31:28]: Shall be set to 8h to acknowledge the receipt of a HPD Packet. Shall be set to 0h to acknowledge the receipt of a SET_CONFIG Packet. All other values are reserved.

10.3.4.3 MAIN-Link Path Packets		
10.3.4.3#1	NT	When generating a Main-Link Path Packet, a DP IN Adapter Layer shall put the value in the <i>Video HopID</i> field into the <i>HopID</i> field of the Tunneled Packet header.
10.3.4.3#2	NT	When a DP OUT Adapter Layer receives a Tunneled Packet with a HopID that is equal to the <i>Video HopID</i> field, it shall treat that packet as a Main-Link Path Packet.
10.3.4.3.1 DP Link Control Packet		
10.3.4.3.1#1		A DP Link Control Packet shall have the format shown in Figure 10-12.
10.3.4.3.1#2		The PDF field in the header shall be set to 11.
10.3.4.3.1#3		A DP Link Control Packet payload shall contain the following: Type (DW 0 [31:24]): This field specifies the type of the DP Link Control Packet. This field shall carry one of the Type values listed in Table 10-7
10.4 System Flows		
10.4.1 Connection Manager Discovery		
10.4.2 Path Configuration		
10.4.2.1 Setup		
10.4.2.1#1	NT	A DP OUT Adapter shall poll the DP_STATUS.CMHS field and DP_REMOTE_CAP.Protocol Adapter Version field for as long as the values in those fields are both 0.
10.4.2.1#2	NT	When either DP_STATUS.CMHS = 1 or DP_REMOTE_CAP.Protocol Adapter Version > 0, the DP OUT Adapter shall do the following: If DP_REMOTE_CAP.Protocol Adapter Version was set to non-zero value while DP_STATUS_CTRL.CMHS remained zero, a DP OUT Adapter shall conclude it is a TBT3 Connection Manager and shall continue the flow as defined in Section 13.8.3.
10.4.2.1#3	NT	When either DP_STATUS.CMHS = 1 or DP_REMOTE_CAP.Protocol Adapter Version > 0, the DP OUT Adapter shall do the following: If DP_STATUS_CTRL.CMHS is set to 1 and DP_STATUS_CTRL.UF is zero, a DP OUT Adapter shall conclude it is a TBT3 DP IN Adapter and shall continue the flow as defined in Section 13.8.3.
10.4.2.1#4	NT	When either DP_STATUS.CMHS = 1 or DP_REMOTE_CAP.Protocol Adapter Version > 0, the DP OUT Adapter shall do the following: If DP_STATUS_CTRL.CMHS is set to 1 and DP_STATUS_CTRL.UF is set to one, a DP OUT Adapter shall reset DP_STATUS_CTRL.CMHS to zero.
10.4.2.1#5	TD 10.1 TD 10.9	A DP Adapter shall set the DP_COMMON_CAP register, to reflect the lowest common capability between DP_LOCAL_CAP and DP_REMOTE_CAP fields.

10.4.2.1#6		A Router shall set DP_STATUS_CTRL.CMHS to 0b within tCMHSClear time after DP_STATUS_CTRL.CMHS is set to 1b.
<b>10.4.2.2 Tear-down</b>		
10.4.2.2#1	TD 10.1 TD 10.9	When the ADP_DP_CS_0.AE bit and the ADP_DP_CS_0.VE bit are both set to 0, a DP Adapter shall set all the fields in its DP Adapter Configuration Capability to their default values.
<b>10.4.3 HPD Event Propagation</b>		
<b>10.4.3.1 HPD Plug</b>		
10.4.3.1#1	NT	After a Path is setup between a DP OUT Adapter and a DP IN Adapter per 10.4.2.1, the DP OUT Adapter shall send an HPD Packet with the <i>P Flag</i> set to 1b.
10.4.3.1#2	NT	Upon receiving an HPD Packet with the <i>P Flag</i> set to 1b, the DP IN Adapter shall respond with an ACK Packet, execute the DP Adapter Init flow as defined in Section 10.4.5, and then drive HPD signal high on the DisplayPort interface
10.4.3.1#3	NT	After the DP IN Adapter drives HPD high, both DP Adapters shall be ready to handle AUX transactions.
<b>10.4.3.2 HPD Unplug</b>		
10.4.3.2#1	NT	Upon unplug detection, the DP OUT Adapter shall send an HPD Packet with the <i>P Flag</i> set to 0b to the DP IN Adapter.
10.4.3.2#2	NT	The DP IN Adapter shall respond with an ACK Packet and drive the HPD signal low.
10.4.3.2#3	NT	When the HPD signal is low, a DP IN Adapter may disable its DP Link receiver.
<b>10.4.3.3 IRQ</b>		
10.4.3.3#1	NT	Upon IRQ detection, a DP OUT Adapter shall send a SET_CONFIG Packet of MSG type IRQ to the DP IN Adapter.
10.4.3.3#2	NT	A DP IN Adapter that receives a SET_CONFIG Packet of MSG type IRQ shall respond with an ACK Packet and drive the IRQ event (according to the DisplayPort 1.4a Specification) towards the DPTX.
10.4.3.3#3	NT	However, if Link training is in process or it just ended, a DP OUT Adapter shall wait tIRQDelay after it sent a SET_CONFIG Packet to the DP IN Adapter (reporting that Link training is completion) before sending the IRQ SET_CONFIG Packet.

10.4.3.4 HPD Delay Requirements		
10.4.3.4#1	NT	Table 10-7 defines the maximum propagation delay through the DP Adapters that shall be used for HPD Events.
10.4.3.4#2	NT	The propagation delay through the DP OUT Adapter shall be measured from when the event is detected by the DP OUT Adapter to when the last bit of the corresponding packet, SET_CONFIG or HPD, is sent over the AUX Path.
10.4.3.4#3	NT	The propagation delay through the DP IN Adapter shall be measured from when the last bit of an HPD Event Packet, SET_CONFIG or HPD, arrives at the DP IN Adapter to when event is driven on the HPD signal.
10.4.3.4#4	NT	A DP OUT Adapter shall send HPD packet with the <i>P Flag</i> set to 1b within tDPPlug of transitioning to the Paired state.
10.4.3.5 Manual HPD Control		
10.4.3.5#1	TD 10.002	When HPDC transitions from 0b to 1b, a DP IN Adapter shall drive the DisplayPort HPD signal low.
10.4.3.5#2	TD 10.002	When HPDS transitions from 0b to 1b, a DP IN Adapter shall drive the DisplayPort HPD signal high.
10.4.3.5#3	TD 10.002	The DisplayPort HPD signal level shall be set according to the most recent event, whether it is HPDS set, HPDC set, IRQ SET_CONFIG Packet or HPD Packet.
10.4.4 AUX Request and Response Handling		
10.4.4.1 LTTPR Non-Transparent Mode		
10.4.4.1#1		During 128b/132b DisplayPort link training, a DP Adapter shall operate in AUX Intra-Hop mode as defined in the DisplayPort 1.4a Specification.
10.4.4.1#2		Otherwise, a DP IN Adapter shall operate as defined in Section 10.4.4.1.1 and a DP OUT Adapter shall operate as defined in Section 10.4.4.1.2.
10.4.4.1.1 DP IN Adapter Requirements		
10.4.4.1.1#1	NT	Upon reception of a DisplayPort AUX request, a DP IN Adapter shall send an AUX Packet containing the request over the AUX Path.
10.4.4.1.1#2	NT	The AUX request coming from the DPTX shall not be modified by the DP IN Adapter.
10.4.4.1.1#3	NT	For Target transactions, the DP IN Adapter shall set the AUX_PEND flag as defined in the DisplayPort 1.4a Specification – Section 3.6.5.3.2, and take the appropriate action when the request comes back according to the DisplayPort 1.4a Specification – Section 3.6.5.3.2.

10.4.4.1.1#4	NT	When a DP IN Adapter updates the DP OUT Adapter as the results of a Snoop or Target transaction, it shall perform the update only after receiving an AUX Response and before sending the AUX ACK response to the DPTX. This rule applies for all cases except a SET_CONFIG Packet of type SET_VSPE.
10.4.4.1.1#5	NT	Updating the DP OUT Adapter shall be done by sending SET_CONFIG Packets to the DP OUT Adapter.
<b>10.4.4.1.2 DP OUT Adapter Requirements</b>		
10.4.4.1.2#1	TD 10.005	A DP OUT Adapter shall convert an incoming AUX Packet received from the USB4 Fabric into a DisplayPort AUX request.
10.4.4.1.2#2	TD 10.005	The content of the request shall not be modified by the DP OUT Adapter.
10.4.4.1.2#3	TD 10.005	A DP OUT Adapter shall convert an incoming DisplayPort AUX response into an AUX Packet and send it on the AUX Path.
10.4.4.1.2#4	TD 10.005	The content of the response shall not be changed by the DP OUT Adapter.
<b>10.4.4.2 Non-LTTPR Mode</b>		
10.4.4.2#1	TD 10.004	A DP IN Adapter shall implement AUX Replier.
10.4.4.2#2	TD 10.004	A DP OUT Adapter shall implement AUX Requester.
<b>10.4.4.2.1 AUX Timeout Timers</b>		
10.4.4.2.1#1	TD 10.004	The AUX Response Timeout timer in a DP IN Adapter shall be set to 300µs.
10.4.4.2.1#2	TD 10.004	The AUX Reply Timeout timer in a DP OUT Adapter shall be set to 400µs.
<b>10.4.4.2.2 DP IN Adapter Port Requirements</b>		
10.4.4.2.2#1	TD 10.004	A DP IN Adapter that receives an AUX Request shall classify the AUX Transaction as one of the three following types: 1) Internal AUX Transaction – AUX Request which targets only DPCD addresses that are defined as internal in Table 10-8; 2) External AUX Transaction – AUX Request which targets only DPCD addresses that are not defined as internal in Table 10-8; 3) Combined AUX Transaction – AUX Request which targets both Internal and External DPCD addresses. The AUX Response is initially generated by the DPRX and altered by the DP IN Adapter.
10.4.4.2.2#2	TD 10.004	For Internal AUX Transactions, a DP IN Adapter shall not send the AUX Request downstream and shall self-generate the AUX Response.
10.4.4.2.2#3	TD 10.004	For External and Combined AUX Transactions, a DP IN Adapter shall send the AUX Request downstream to the DP OUT Adapter.

10.4.4.2.2#4	TD 10.004	If the AUX Response does not arrive on time, the DP IN Adapter shall generate an AUX DEFER before the AUX Response timer expires.
10.4.4.2.2#5	TD 10.004	A DP IN Adapter shall not send an AUX Request to a DP OUT Adapter while the AUX Reply to the preceding AUX Request is outstanding.
10.4.4.2.2#6	TD 10.004	DP IN Adapter shall increment AUX_REQ_CNTR by 1 on every received AUX request from DPTX and shall reset to zero on transition to IDLE state.
10.4.4.2.2#7	TD 10.004	Table 10-10: DP IN Adapter Port AUX Handling State Machine
10.4.4.2.2#8		When a DPTX reads address 00205h during link training, a DP IN Adapter shall respond with value of 0h.
10.4.4.2.2#9		When a DP IN Adapter updates the DP OUT Adapter as the result of an External or Combined transaction, it shall perform the update only after receiving an AUX Response and before sending the AUX ACK response to the DPTX. This rule applies for all cases except when receiving the first AUX Request to the <i>LT-tunable PHY Repeater DPCD Capability and ID</i> field.
10.4.4.2.2#10		Upon reception of the first AUX Request to the <i>LT-tunable PHY Repeater DPCD Capability and ID</i> field, the DP IN Adapter sends a SET_CONFIG Packet of type SET_LTPR_MODE without waiting for an AUX Response. The update shall be done by sending SET_CONFIG Packets to the DP OUT Adapter.
<b>10.4.4.2.3 DP OUT Adapter Requirements</b>		
10.4.4.2.3#1	TD 10.004	A DP OUT Adapter that receives a DPTX initiated AUX Request while handling a DP OUT Adapter Initiated AUX Transaction, shall send the DPTX initiated AUX Request as soon as it is in Talk Mode.
<b>10.4.4.2.3.1 DPTX Initiated AUX Transactions</b>		
10.4.4.2.3.1#1	TD 10.004	A DP OUT Adapter that receives an AUX Request from a DP IN Adapter shall initiate the AUX Request as soon as it is in Talk Mode.
10.4.4.2.3.1#2	TD 10.004	A DP OUT Adapter that receives an AUX Response shall send the AUX Response over the AUX Path to the DP IN Adapter.
10.4.4.2.3.1#3	TD 10.004	If the AUX Reply Timer expires before an AUX Response is received, a DP OUT Adapter shall send a SET_CONFIG of type SET_AUX_INIT and shall not retry the AUX Request.
<b>10.4.4.2.3.2 DP OUT Adapter Initiated AUX Transactions</b>		
<b>10.4.4.3 LTPR Transparent Mode</b>		
10.4.4.3#1	NT	A DP IN Adapter shall implement AUX Replier.

10.4.4.3#2	NT	A DP OUT Adapter shall implement AUX Requester.
<b>10.4.4.3.1 AUX Timeout Timers</b>		
10.4.4.3.1#1	NT	The AUX Response Timeout timer in a DP IN Adapter shall not be activated.
10.4.4.3.1#2	NT	The AUX Reply Timeout timer in a DP OUT Adapter shall be set to 3.2ms.
<b>10.4.4.3.2 DP IN Adapter Requirements</b>		
10.4.4.3.2#1	NT	A DP IN Adapter that receives an AUX Request shall classify the AUX Transaction as one of the following types: Internal AUX Transaction – AUX Request which targets only DPCD addresses that are defined as internal in Table 10-9; External AUX Transaction – AUX Request which targets only DPCD addresses that are not defined as internal in Table 10-9; Combined AUX Transaction – AUX Request which targets both Internal and External DPCD addresses. The AUX Response is initially generated by the DPRX and altered by the DP IN Adapter.
10.4.4.3.2#2	NT	For External and Combined AUX Transactions, a DP IN Adapter shall send the AUX Request downstream to the DP OUT Adapter.
10.4.4.3.2#3	NT	A DP IN Adapter shall not: Generate AUX DEFER; Gate any External or Combined AUX Request sent by the DPTX; Gate any AUX Response sent by the DPRX.
10.4.4.3.2#4		When a DP IN Adapter updates the DP OUT Adapter as the result of an External or Combined transaction, it shall perform the update only after receiving an AUX Response and before sending the AUX ACK response to the DPTX.
10.4.4.3.2#5		The update shall be done by sending SET_CONFIG Packets to the DP OUT Adapter.
<b>10.4.4.3.3 DP OUT Adapter Requirements</b>		
10.4.4.3.3#1	NT	A DP OUT Adapter that receives a DPTX initiated AUX Request while handling a DP OUT Adapter Initiated AUX Transaction, shall send the DPTX initiated AUX Request as soon as it is in Talk Mode.
<b>10.4.4.3.3.1 DP TX Initiated AUX Transactions</b>		
10.4.4.3.3.1#1	NT	A DP OUT Adapter that receives an AUX Request from a DP IN Adapter shall initiate the AUX Request as soon as it is in Talk Mode.
10.4.4.3.3.1#2	NT	A DP OUT Adapter that receives an AUX Response shall send the AUX Response over the AUX Path to the DP IN Adapter.
10.4.4.3.3.1#3	NT	If the AUX Reply Timer expires before an AUX Response is received, a DP OUT Adapter shall send a SET_CONFIG of type SET_AUX_INIT and shall not retry the AUX Request.



<b>10.4.4.3.3.2 DP OUT Adapter Initiated AUX Transactions</b>		
<b>10.4.4.4 AUX Delay Requirements</b>		
10.4.4.4#1	TD 10.004	The DP-to-USB4 Fabric delay shall be measured from the time the last bit arrives at the DP Adapter from the DisplayPort interface to the time when the first bit is sent to the USB4 Fabric.
10.4.4.4#2	TD 10.004	USB4 Fabric-to-DP delay shall be measured from the time when the last bit of the AUX Packet arrives at the DP Adapter to the time when the first bit is sent to the DisplayPort Interface, assuming the DP Adapter is in Talk Mode.
<b>10.4.4.5 Aggregation DisplayPort Capabilities</b>		
10.4.4.5#1	TD 10.002 TD 10.004	A DP IN Adapter shall update its DP_LOCAL_CAP and DP_COMMON_CAP registers if it receives an AUX Read Response that has lower parameter values than the registers currently contain.
10.4.4.5#2	TD 10.002 TD 10.004	Before transmitting the AUX Read Response, the DP IN Adapter shall update the AUX Read Response to reflect the aggregated DisplayPort Capabilities as shown in Table 10-11.
<b>10.4.4.6 DPCD DP Tunneling over USB4</b>		
10.4.4.6#1	NT	When a DP IN Adapter receives an AUX Request targeting the DP Tunneling over USB4 Field DPCDs, it shall respond with its internal data.
10.4.4.6#2	NT	A DP IN Adapter shall set the <i>DP Tunneling Support</i> bit to 1b in the DP TUNNELING_CAPABILITIES DPCD (Address E000Dh bit offset 0).
<b>10.4.5 DP Adapters Init Flow</b>		
10.4.5#1	TD 10.007	A DP IN Adapter in the Paired state shall do the following after receiving a first HPD Packet with the <i>P flag</i> set to 1b: Update MFDP Mode inner variable according to Section 10.4.5.1.
10.4.5#2	TD 10.007	A DP IN Adapter in the Paired state shall do the following after receiving a first HPD Packet with the <i>P flag</i> set to 1b: Send a SET_CONFIG Packet of type SET_AUX_INIT.
10.4.5#3	TD 10.007	The DP IN Adapter shall not drive HPD high on the DisplayPort Interface until after it performs the steps above.
10.4.5#4		A DP IN Adapter in the Paired state shall do the following after receiving a first HPD Packet with the <i>P flag</i> set to 1b: If the DP_COMMON_CAP.Protocol Adapter Version field equals 5, complete the DP Cable Discovery handshake as defined in Section 10.4.5.2.1.

10.4.5.1 Multi-Function DP		
10.4.5.1#1	TD 10.007	If a DP IN Adapter is not connected as part of a Multi-Function (as defined in the DisplayPort Alt Mode Specification), it shall send a SET_CONFIG Packet of type SET_MFDP with the MFDP Enable bit set to 0b.
10.4.5.1#2	TD 10.007	A DP OUT Adapter which receives a SET_CONFIG Packet of type SET_MFDP shall respond with a SET_CONFIG Packet of type SET_MFDP within tDPInit.
10.4.5.1#3	TD 10.007	If the DP OUT Adapter is connected as part of Multi-Function as defined in the DisplayPort 1.4a Specification, then the MFDP Enable bit shall be set to 1b, otherwise it shall be set to 0b.
10.4.5.2 DP Cable Discovery		
10.4.5.2.1 DP Cable Discovery Handshake		
10.4.5.2.1#1		A DP IN Adapter shall send a SET_CONFIG Packet of type CABLE_DISCOVERY to the DP OUT Adapter.
10.4.5.2.1#2		A DP OUT Adapter that receives a SET_CONFIG Packet of type CABLE_DISCOVERY shall respond with a SET_CONFIG Packet of type CABLE_DISCOVERY.
10.4.5.2.1#3		The Cable Type field in the SET_CONFIG Packet shall indicate which type of DP cable the DP OUT Adapter discovered on its connector.
10.4.5.2.1#4		The UHBR10_20_Support and UHBR13.5_Support fields in the SET_CONFIG Packet shall indicate the UHBR support the DP OUT Adapter discovered on its connector.
10.4.5.2.1#5		The DP OUT Adapter shall send the SET_CONFIG Packet within tDPInit after receiving the SET_CONFIG Packet from the DP IN Adapter.
10.4.5.2.1#6		After receiving the SET_CONFIG Packet of type CABLE_DISCOVERY from the DP OUT Adapter, the DP IN Adapter shall save the <i>Cable Type</i> field as DP OUT Adapter Cable Type.
10.4.5.2.2 DP Cable Discovery AUX Handling		
10.4.5.2.2#1		When the DPTX reads from DPCD address 02217h, a DP IN Adapter shall do the following: Save the AUX Response Cable Type field as the DPRX Cable Type.
10.4.5.2.2#2		When the DPTX reads from DPCD address 02217h, a DP IN Adapter shall do the following: Set the Cable Type field in the AUX Response to the same cable type that the DP IN Adapter discovered on its connector.

10.4.5.2.2#3		When the DPTX reads from DPCD address 02217h, a DP IN Adapter shall do the following: Set the UHBR10_20 Capability field in the AUX Response to the highest common capability between the AUX Response UHBR10_20 Capability field it received from DPRX and the UHBR10_20 Capability that the DP IN Adapter discovered on its connector.
10.4.5.2.2#4		When the DPTX reads from DPCD address 02217h, a DP IN Adapter shall do the following: Set the UHBR13.5 Capability bit in the AUX Response to the logical AND between the AUX Response UHBR13.5 Capability bit it received from DPRX and the UHBR13.5 Capability that the DP IN Adapter discovered on its connector.
10.4.5.2.2#5		When the DPTX writes to DPCD address 00110h, a DP IN Adapter shall do the following: Save the Cable Type field in the AUX Request as the DPTX Cable Type.
10.4.5.2.2#6		When the DPTX writes to DPCD address 00110h, a DP IN Adapter shall do the following: Set the Cable Type field in the AUX Request according to the following rules: If the saved DPRX Cable Type is not 000b (unknown cable type), then set the Cable Type field to the saved DPRX Cable Type; Else, if the DP IN Adapter received a SET_CONFIG Packet of type CABLE_DISCOVERY, then set the Cable Type field to the saved DP OUT Adapter Cable Type; Else, set the Cable Type field to 000b.
10.4.5.2.2#7		When DPTX reads from DPCD address 00110h, a DP IN shall set the Cable Type field in the AUX Response to the saved DPTX Cable Type.
<b>10.4.6 DP Source Discovery</b>		
<b>10.4.6.1 LTTTPR Recognition and Modes Change</b>		
10.4.6.1#1	NT	A DP IN Adapter shall modify the resulting AUX read response as defined in Section 10.4.4.5.
10.4.6.1#2	NT	If DP_COMMON_CAP.LTTTPR <i>Not Supported</i> is set to 1b, a DP Adapter shall operate only in Non-LTTTPR mode.
10.4.6.1#3	NT	When a DP IN Adapter is operating in Non-LTTTPR mode and it receives the first AUX Request to the <i>LT-tunable PHY Repeater DPCD Capability and ID</i> field, it shall: 1) Transition to LTTTPR Transparent mode; 2) Send a SET CONFIG Packet of type SET_LTTTPR_MODE with LTTTPR_Mode set to 0b; 3) Complete the AUX Transaction operating in LTTTPR Transparent mode.
10.4.6.1#4	NT	A DP IN Adapter shall do the following before transitioning from LTTTPR Transparent mode to LTTTPR Non-Transparent mode: Complete the AUX Transaction according to the current operation mode; Send a SET CONFIG Packet of type SET_LTTTPR_MODE with LTTTPR_Mode set to 1b.
10.4.6.1#5		When DPCD address F0002h is read by a DPTX, a DP IN Adapter shall determine and save the number of LTTTPRs located downstream.

10.4.6.1#6		If the DP_COMMON_CAP.Protocol Adapter Version equals 5, a DP IN Adapter shall follow the rules below when setting the Downstream LTTPrs field and Downstream_LTTPrs_Valid bit in a SET_CONFIG Packet of type SET_LTTPrs_MODE: If DPTX has read F0002h since HPD was asserted, then set the Downstream LTTPrs field to the saved downstream LTTPrs value and set the Downstream_LTTPrs_Valid bit to 1b; Else, set the Downstream LTTPrs field to 0h and the Downstream_LTTPrs_Valid bit to 0b.
<b>DPRX Capabilities Read</b>		
10.4.6.2#1	NT	The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall: 1) Snoop the read response and record the values of the DPCD_REV, MAX_LINK_RATE, MAX_LANE_COUNT, TPS3_SUPPORTED and TPS4_SUPPORTED fields located at DPCD addresses 00000h/02200h, 00001h/02201h, 00002h/02202h and 00003h/02203h respectively.
10.4.6.2#2	NT	The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall: 2) Update the Maximal DPCD Rev, Maximal Link Rate, Maximal Lane Count, <i>8b10b</i> TPS3 Capability and <i>8b10b</i> TPS4 Capability fields in the DP_LOCAL_CAP and DP_COMMON_CAP registers to reflect the lowest common capabilities between the existing values of those registers and the recorded values from step 1.
10.4.6.2#3	NT	The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall: 3) Send a SET_CONFIG Packet of type SET_CMN_DPRX with MSG Data equal to the snooped DPCD_REV which reflects the DPRX DPCD_REV.
10.4.6.2#4	NT	The DPRX Capabilities read is performed by the DPTX. In response to a DPRX Capabilities read, a DP IN Adapter shall: 4) Set the <i>DPRX Capabilities Read Done</i> field in the DP_COMMON_CAP register to 1b. Note that this field is set to 1b regardless of whether or not the values in the <i>Maximal Link Rate</i> and <i>Maximal Lane Count</i> fields in Step 2 were changed.
<b>10.4.6.3 Sink Count Read</b>		
10.4.6.3#1	TD 10.002	When DPCD addresses 00200h or 02002h are read by the DPTX, a DP IN Adapter shall snoop the read response and record the value of the SINK_COUNT.
10.4.6.3#2	TD 10.002	When the recorded SINK_COUNT value is zero, the DP IN Adapter shall send a SET_CONFIG Packet of type SET_SINK_COUNT, reflecting the recorded value.
10.4.6.3#3	TD 10.002	When a DP OUT Adapter receives a SET_CONFIG Packet of type SET_SINK_COUNT with the SINK_COUNT value equal to zero, the DP OUT Adapter shall: Report an Unplug event as defined in Section 10.3.3.

10.4.6.3#4	TD 10.002 TD 10.004	When a DP OUT Adapter receives a SET_CONFIG Packet of type SET_SINK_COUNT with the SINK_COUNT value equal to zero, the DP OUT Adapter shall: Set the ADP_DP_CS_2.HPD Status to 0b in the DP OUT Adapter Configuration Capability Field.
10.4.6.3#5	TD 10.002 TD 10.004	While a DP OUT Adapter is Unplugged and has the ADP_DP_CS_2.HPD Status set to 0b in the DP OUT Adapter Configuration Capability Field, it shall do the following upon IRQ detection: Report a Plug event as defined in Section 10.3.3.
10.4.6.3#6	TD 10.002 TD 10.004	While a DP OUT Adapter is Unplugged and has the ADP_DP_CS_2.HPD Status set to 0b in the DP OUT Adapter Configuration Capability Field, it shall do the following upon IRQ detection: Set the ADP_DP_CS_2.HPD Status to 1b in the DP OUT Adapter Configuration Capability Field.
<b>10.4.7 Down-Spread Control</b>		
10.4.7#1	NT	When DPCD address 00107h is written by a DPTX, a DP IN Adapter, operating in Non-LTTPR or LTTPR Transparent Modes, shall respond with AUX ACK and shall send a SET_CONFIG Packet of type SET_DOWNSPREAD.
10.4.7#2	NT	The MSG Data field in the SET_CONFIG Packet shall be equal to the value written by the DPTX.
10.4.7#3	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of type SET_DOWNSPREAD shall initiate an AUX write request to DPCD address 00107h with the value received in the MSG Data of the SET_CONFIG Packet.
<b>10.4.8 Stream Mode Set</b>		
10.4.8#1	NT	If the DPTX writes to DPCD address 00111h, a DP IN Adapter shall snoop the write request and record the value of the MST_EN bit.
10.4.8#2	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_STREAM_MODE, reflecting the recorded value of the MST_EN bit when a new recorded MST_EN value is different than the previous value
10.4.8#3	NT	The MST_EN default value at the DP Adapters shall be as defined in the DisplayPort 1.4a Specification.
10.4.8#4	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of type SET_STREAM_MODE shall respond with a SET_CONFIG Packet of type SET_STREAM_MODE, to signify the acknowledgment of the mode change.
10.4.8#5	NT	The value of the MSG Data field in the return packet has no meaning and shall be ignored by the DP IN Adapter.

10.4.9 DSC and FEC Enable		
10.4.9#1	NT	If the DPTX writes to DPCD address 00120h, a DP IN Adapter shall snoop the write request and record the values of the <i>FEC_READY</i> , <i>FEC_ERROR_COUNT_SEL</i> and <i>LANE_SELECT</i> fields.
10.4.9#2	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_FEC_READY, reflecting the recorded value of the FEC_READY bit when a new recorded FEC_READY value is different than the previous value.
10.4.9#3	NT	The FEC_READY default value at the DP Adapters shall be as defined in the DisplayPort 1.4a Specification.
10.4.9#4	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of type SET_FEC_READY shall respond with a SET_CONFIG Packet of type SET_FEC_READY within tDPInit, to signify the acknowledgment of the mode change.
10.4.9#5	NT	The value of the <i>MSG Data</i> field in the return packet has no meaning and shall be ignored by the DP IN Adapter.
10.4.10 DP Link Training		
10.4.10.1 8b/10b LTTTPR Non-Transparent		
10.4.10.1#1	NT	The DP IN and DP OUT Adapters shall follow the LTTTPR Non-Transparent link training as defined in the DisplayPort 1.4a Specification while noting the following points: <u>DP IN as UFP and DFP</u> – As described in Section 10.4.4, the DP IN Adapter serves as UFP and DFP for AUX handling, therefore it updates the DP OUT Adapter with the different stages of the LTTTPR Non-Transparent link training through SET_CONFIG Packets; <u>Training Patterns</u> – Training Patterns are not carried over the USB4 Fabric.
10.4.10.1.1 DP IN Adapter Requirements		
10.4.10.1.1#1	NT	After DP Link training is finished on the UFP, a DP IN Adapter shall maintain symbol lock and lane alignment in its receiver while DPTX trains the rest of downstream DP Links
10.4.10.1.1#2	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_LINK after DPTX writes TPS1 to the DP IN Adapter TRAINING_PATTERN_SET_PHY_REPEATERx DPCD register.
10.4.10.1.1#3	NT	The SET_CONFIG packet shall have the following values: LC = LANE_COUNT_SET value written by DPTX; LR = LINK_BW_SET value written by the DPTX; MSG Data = 1b, representing DP Link Training Mode = LTTTPR Non-Transparent.

10.4.10.1.1#4	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_TRAINING with TS = 0xFF after DPTX writes 0x0 to the DP IN Adapter TRAINING_PATTERN_SET_PHY_REPEATERx DPCD register.
10.4.10.1.1#5	NT	When a DP IN Adapter receives the AUX ACK for the DPCD AUX Write of 0x0 to the DPRX TRAINING_PATTERN_SET DPCD register, it shall first send a SET_CONFIG Packet of type SET_TRAINING with TS = 0x0 and then send the AUX ACK to the DPTX.
10.4.10.1.1#6	NT	After DP Link training is finished on the UFP, a DP IN Adapter shall detect a Training pattern on its receiver.
10.4.10.1.1#7	NT	After detecting the Training pattern, the DP IN Adapter shall send a single corresponding SET_CONFIG Packet of type SET_TRAINING for every change in Training pattern.
10.4.10.1.1#8	NT	The TS field shall be equal to the detected Training pattern as defined in Table 10-5.
10.4.10.1.1#9	NT	A DP IN Adapter shall send SET_CONFIG Packet of Type SET_VSPE when DPTX writes the TRAINING_LANE0_SET or TRAINING_LANE0_SET_PHY_REPEATERx DPCD register of the next downstream receiver.
10.4.10.1.1#10	NT	The MSG Data field shall carry the value in the write request.
10.4.10.1.1#11	NT	The SET_VSPE SET_CONFIG Packet shall be sent by the DP IN Adapter before sending the AUX Request Packet.
10.4.10.1.1#12	NT	A DP Adapter shall have higher priority generating and parsing SET_CONFIG packets over AUX Transaction.
10.4.10.1.1#13	NT	A DP IN Adapter shall respond to a DPTX that link training has ended successfully only when all the following are true: The DP IN Adapter internal status indicates link training has ended successfully; The DP IN Adapter sent at least nine DP Clock Sync Packets after it sent the SET_CONFIG Packet of type SET_LINK.
<b>10.4.10.1.2 DP OUT Adapter Requirements</b>		
10.4.10.1.2#1	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of Type SET_LINK with the DP Link Training Mode bit set to 1b shall start its internal Symbol clock PLL according to the Link Rate field, and start the Lifetime Counter as defined in Section 10.6.1.2.
10.4.10.1.2#2	NT	A DP OUT Adapter that receives a SET_CONFIG Packet of Type SET_TRAINING with TS field equal to 1, 2, 3 or 7 shall transmit TPS1, TPS2, TPS3 or TPS4 accordingly.
10.4.10.1.2#3	NT	Deprecated.

10.4.10.1.2#4	NT	A DP OUT Adapter shall set its Voltage Swing (VS) and Pre-Emphasis (PE) levels for all enabled lanes upon receiving a SET_CONFIG Packet of type SET_VSPE. The VS and PE levels shall be according to the MSG Data. The DP OUT Adapter shall transition on the 10-bit symbol boundary when: Transitioning from one training pattern to another training pattern; Transitioning to IDLE sequence after DP Link training is done.
<b>10.4.10.1.3 DP Link Training Example</b>		
<b>10.4.10.1.3.1 LTTTPR - CR_DONE Phase</b>		
<b>10.4.10.1.3.2 LTTTPR - EQ Phase</b>		
<b>10.4.10.1.3.3 DPRX - CR_DONE Phase</b>		
<b>10.4.10.1.3.4 DPRX - EQ Phase</b>		
<b>10.4.10.2 8b/10b Non-LTTTPR and 8b/10b LTTTPR Transparent</b>		
10.4.10.2#1	NT	A DP Adapter shall perform DisplayPort link training according to the DisplayPort 1.4a Specification with the modifications and requirements defined in Section 10.4.10.2.1 and Section 10.4.10.2.2
<b>10.4.10.2.1 DP IN Adapter Requirements</b>		
10.4.10.2.1#1	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_LINK after DPTX writes TPS1 to the DP RX TRAINING_PATTERN_SET DPCD register.
10.4.10.2.1#2	NT	The SET_CONFIG packet shall have the following values: LC = LANE_COUNT_SET value written by DPTX; LR = LINK_BW_SET value written by the DPTX; TPS = Reflects TPS3 and TPS4 support as indicated in the DP_COMMON_CAP register; MSG Data = 0b, representing DP Link Training Mode = Non-LTTTPR and LTTTPR Transparent modes.
10.4.10.2.1#3	NT	A DP IN Adapter shall respond to a status read of LANEx_CR_DONE as follows: If a SET_CONFIG Packet of type STATUS_CR_DONE was not received since link training started, set the LANEx_CR_DONE bits to 0b.
10.4.10.2.1#4	NT	A DP IN Adapter shall respond to a status read of LANEx_CR_DONE as follows: If a SET_CONFIG Packet of type STATUS_CR_DONE was received since link training started, set the LANEx_CR_DONE bits to be the internal DP IN Adapter status for a lane ANDed with the relevant bit present in the last received SET_CONFIG MSG Data.



10.4.10.2.1#5	NT	A DP IN Adapter shall respond to a DPTX that link training has ended successfully only when all the following are true: The DP IN Adapter internal status indicates link training has ended successfully; The DP IN Adapter received a SET_CONFIG Packet of type SET_LINK, carrying the same <i>LC</i> and <i>LR</i> fields that it sent to the DP OUT Adapter when link training was initiated; The DP IN Adapter sent at least nine DP Clock Sync Packets after it received a SET_CONFIG Packet of type STATUS_CR_DONE.
10.4.10.2.1#6	NT	While the conditions (as defined in this section) for successful link training are not met, a DP IN Adapter shall respond to a status read of INTERLANE_ALIGN_DONE, LANEx_CHANNEL_EQ_DONE and LANEx_SYMBOL_LOCKED as follows: If a SET_CONFIG Packet of type STATUS_TRAINING_FAIL was received since link training started, set the following bits: INTERLANE_ALIGN_DONE shall be set to 0b. LANEx_CHANNEL_EQ_DONE is equal to the DP IN internal status ANDed with LANEx_CHANNEL_EQ_DONE that was received as MSG Data by the STATUS_TRAINING_FAIL. LANEx_SYMBOL_LOCKED is equal to the DP IN internal status ANDed with LANEx_SYMBOL_LOCKED that was received as MSG Data by the STATUS_TRAINING_FAIL.
10.4.10.2.1#7	NT	Else, a DP IN Adapter shall use one or more of the methods below to indicate to DPTX that link training has not completed successfully yet: Set INTERLANE_ALIGN_DONE to 0b; Set LANEx_CHANNEL_EQ_DONE to 0b for any of the active lanes; Set LANEx_SYMBOL_LOCKED to 0b for any of the active lanes.
<b>10.4.10.2.2 DP OUT Adapter Requirement</b>		
10.4.10.2.2#1	NT	A DP OUT Adapter receiving a SET_CONFIG Packet of type SET_LINK, with <i>LC</i> field other than 0h shall: Initiate link training with the target Link Rate and Lane Count received from the SET_LINK Packet.
10.4.10.2.2#2	NT	A DP OUT Adapter receiving a SET_CONFIG Packet of type SET_LINK, with <i>LC</i> field other than 0h shall: Link training proceeds according to the DisplayPort 1.4a spec except that a DP OUT Adapter that concludes that it needs to either reduce the Link Rate or Lane Count shall treat it as link training failure and shall not reduce the Link Rate or Lane Count.
10.4.10.2.2#3	NT	A DP OUT Adapter which finishes the Clock Recovery Sequence (as defined in the DisplayPort 1.4a Specification) shall send a SET_CONFIG Packet of type STATUS_CR_DONE, reflecting the LANEx_CR_DONE statuses of the active lanes.
10.4.10.2.2#4	NT	The <i>Phase</i> field shall be set to 0b.
10.4.10.2.2#5	NT	A DP OUT Adapter in EQ phase which detects that the DP receiver has lost Clock Recovery on one or more of the active lanes shall conclude that link training has failed and shall send a SET_CONFIG Packet of type STATUS_CR_DONE, reflecting the new LANEx_CR_DONE statuses of the active lanes.

10.4.10.2.2#6	NT	The <i>Phase</i> field shall be set to 1b.
10.4.10.2.2#7	NT	If link training fails for a reason other than lost Clock Recovery, a DP OUT Adapter shall send a SET_CONFIG Packet of type STATUS_TRAINING_FAIL.
10.4.10.2.2#8	NT	If link training finishes successfully, a DP OUT Adapter shall: Send a SET_CONFIG Packet of type SET_LINK, with the same <i>LC</i> and <i>LR</i> fields it received from the DP IN Adapter when link training was initiated.
10.4.10.2.2#9	NT	If link training finishes successfully, a DP OUT Adapter shall: Generate IDLE pattern (including SR) for both MST and SST DP Links.
10.4.10.2.2#10	NT	The MSG Data shall be set as follows: LANEx_CHANNEL_EQ_DONE is equal to the value of the last read from LANEx_CHANNEL_EQ_DONE field in DPRX. LANEx_SYMBOL_LOCKED is equal to the value of the last read from LANEx_SYMBOL_LOCKED field in DPRX.
<b>10.4.3.10 128b/132b LTTPr</b>		
10.4.3.10#1		A DP IN Adapter shall act as the upstream facing port of the LTTPr, according to the DisplayPort Specification.
10.4.3.10#2		A DP OUT Adapter shall act the downstream facing port of the LTTPr, according to the DisplayPort Specification.
<b>10.4.3.10.1 DP IN Adapter Requirements</b>		
10.4.3.10.1#1		128b/132b link training starts when a DPTX writes 01h to DPCD address 00102h and the MAIN_LINK_CHANNEL_CODING_SET is equal to 02h. When 128b/132b link training starts, a DP IN Adapter shall: Respond with an AUX ACK.
10.4.3.10.1#2		128b/132b link training starts when a DPTX writes 01h to DPCD address 00102h and the MAIN_LINK_CHANNEL_CODING_SET is equal to 02h. When 128b/132b link training starts, a DP IN Adapter shall: Switch to operate in an AUX Intra-Hop mode, as defined by the DisplayPort Specification.
10.4.3.10.1#3		128b/132b link training starts when a DPTX writes 01h to DPCD address 00102h and the MAIN_LINK_CHANNEL_CODING_SET is equal to 02h. When 128b/132b link training starts, a DP IN Adapter shall: Set 128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE to 0b.
10.4.3.10.1#4		128b/132b link training starts when a DPTX writes 01h to DPCD address 00102h and the MAIN_LINK_CHANNEL_CODING_SET is equal to 02h. When 128b/132b link training starts, a DP IN Adapter shall: Set 128b/132b_LT_FAILED to 0b.

10.4.3.10.1#5		128b/132b link training starts when a DPTX writes 01h to DPCD address 00102h and the MAIN_LINK_CHANNEL_CODING_SET is equal to 02h. When 128b/132b link training starts, a DP IN Adapter shall: Send a SET_CONFIG Packet of type 128b132b_SET_LINK. The MSG Data of the SET_CONFIG packet shall have the following values: LANE_COUNT_SET = LANE_COUNT_SET value written by DPTX; LINK_BW_SET = LINK_BW_SET value written by the DPTX.
10.4.3.10.1#6		A DP IN Adapter shall set the 128b/132b_LT_FAILED bit to 1b if one of the following conditions are true, otherwise it shall be set to 0b: The DP IN Adapter completed the EQ_DONE phase unsuccessfully; A SET_CONFIG Packet of type 128b132b_EQ_DONE was received with the 128b/132b_LT_FAILED bit set to 1b in the MSG Data
10.4.3.10.1#7		A DP IN Adapter shall set the 128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE bit to 1b if all the following conditions are true, otherwise it shall be set to 0b: the DP IN Adapter completed the EQ_DONE phase successfully; A SET_CONFIG Packet of type 128b132b_EQ_DONE was received with the 128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE bit set to 1b in the MSG Data
10.4.3.10.1#8		When a DP IN Adapter receives a SET_CONFIG Packet of type 128b132b_CDS_DONE, it shall disable the AUX Intra-Hop mode
10.4.3.10.1#9		When a DPTX writes 0h to DPCD address 00102h, the AUX Intra-Hop is disabled, and the link is still operating in 4-Bits CDI, it means that link training is ending successfully. A DP IN Adapter shall perform the following in order: 1. Send a SET_CONFIG Packet of type 128b132b_SWITCH_TO_1BIT_CDI; 2. Send the AUX Write request:
10.4.3.10.1#10		A DP IN Adapter shall start converting DisplayPort 128b/132b Link Layer symbols into Tunneled Packets when it receives the first LLCP Link Layer Symbol.
10.4.3.10.1#11		Link Training is aborted as follows: When a DPTX writes 0h to DPCD address 00102h and the AUX Intra-Hop is enabled, a DP IN Adapter shall send a SET_CONFIG Packet of type 128b132b_LT_ABORT.
10.4.3.10.1#12		Link Training is aborted as follows: When a DP IN Adapter receives a SET_CONFIG Packet of type 128b132b_LT_ABORT_DONE, it shall disable the AUX Intra-Hop mode
<b>10.4.3.10.2 DP OUT Adapter Requirements</b>		
10.4.3.10.2#1		When a DP OUT Adapter receives a SET_CONFIG Packet of type 128b132b_SET_LINK, it shall start the 128b132b_EQ_DONE link training phase as defined by the DisplayPort specification:
10.4.3.10.2#2		The DP OUT Adapter shall set the link rate to be equal to the <i>LINK_BW_SET</i> field it received in the <i>MSG Data</i> of the SET_CONFIG Packet.

10.4.3.10.2#3		The DP OUT Adapter shall set the lane count to be equal to the <i>LANE_COUNT_SET</i> field it received in the <i>MSG Data</i> of the SET CONFIG Packet.
10.4.3.10.2#4		A DP OUT Adapter completes the EQ_DONE phase when one of the two conditions are met: Failure: The read value from the 128b/132b_LT_FAILED bit is 1b; Success: EQ_DONE phase ends successfully and the read value from the 128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE bit is 1b.
10.4.3.10.2#5		When a DP OUT Adapter completes the EQ_DONE phase it shall send a SET CONFIG Packet of type 128b132b_EQ_DONE with the following MSG Data: Local EQ_DONE Succeeded – If all activate lanes reported LANEx_CHANNEL_EQ_DONE = 1b then set this bit to 1b, else set this bit to 0b; 128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE – Shall be set to 1b in case of EQ_DONE phase ended successfully, else shall be set to 0b; 128b/132b_LT_FAILED – Shall be set to 0b in case of EQ_DONE phase ended successfully, else shall be set to 1b.
10.4.3.10.2#6		When a DP OUT Adapter receives a SET CONFIG Packet of type 128b132b_CDS it shall do the following: 1.Start adjusting the PLL frequency as described in Section 10.6; 2.Ensure, in an implementation specific manner, that within eight PLL frequency adjustments the link symbol clock frequency difference between its own and the DPTX is such that buffer overflow and buffer underrun is avoided; 3.Write 03h to DPCD address 00102h and receive an AUX ACK; 4. Send a SET CONFIG Packet of type 128b132b_CDS_DONE.
10.4.3.10.2#7		A DP OUT Adapter shall not self-generate any more AUX Transactions after receiving the AUX ACK.
10.4.3.10.2#8		When a DP OUT Adapter receives a SET CONFIG Packet of type 128b132b_SWITCH_TO_1BIT_CDI, it shall parse the next AUX Response: If the response is an AUX ACK, a DP OUT Adapter shall do the following: 1.Transition from 128b/132b_TPS2 to normal operation at the next PHY Sync symbol; 2.Send the AUX ACK; 3.Send a SET CONFIG Packet of type 128b132b_SWITCH_TO_1BIT_CDI_DONE.
10.4.3.10.2#9		When a DP OUT Adapter receives a SET CONFIG Packet of type 128b132b_LT_ABORT it shall do the following steps: 1.Terminate the link training process as defined in the DisplayPort 1.4a Specification; 2.If an AUX transaction is ongoing, wait for its completion; 3.Send a SET CONFIG Packet of type 128b132b_LT_ABORT_DONE.
<b>10.4.10.4 Transition to High Speed Tunnel</b>		
10.4.10.4#1	NT	A DP IN Adapter shall start converting DisplayPort Main-Link Symbols into Tunneled Packets and sending those Packets over the Main-Link Path when all of the following are true: Link Training has completed successfully; For an 8b/10b DP Link: The DP IN Adapter received an SR; For a 128b/132b DP Link: The DP IN Adapter received an LLCP.

<b>10.4.11 Power States Set</b>		
10.4.11#1	NT	When DPTX writes to DPCD address 00600h, a DP IN Adapter shall snoop the write request and record the value of the <i>SET_POWER_STATE</i> field.
10.4.11#2	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_POWER, reflecting the recorded value in the following cases: A first DPCD write of address 00600h after an HPD Plug event.
10.4.11#3	NT	A DP IN Adapter shall send a SET_CONFIG Packet of type SET_POWER, reflecting the recorded value in the following cases: The new recorded SET_POWER_STATE is different than the previous value.
<b>10.4.12 DP Main-Link Disable</b>		
10.4.12#1	NT	DP OUT Adapter which receives a Main-Link disable message shall disable its transmitters.
<b>10.4.13 Link-Init</b>		
10.4.13#1	NT	Upon Link-Init activation, a DP IN Adapter shall turn off its DisplayPort receivers and stop any transmission of Tunneled Packets over the Main-Link Path until the end of the next successful Link training, as defined in Section 10.4.10.3.
10.4.13#2	NT	Upon Link-Init activation, a DP OUT Adapter shall turn off its DisplayPort transmitters.
<b>10.4.14 DP PHY Testability</b>		
<b>10.4.14.1 DP IN Adapter PHY Layer Testing</b>		
10.4.14.1#1	NT	The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Before entering DP IN PHY Test Mode: Connect a Router with a DP OUT Adapter and a DPRX. Both the DP OUT Adapter and the DPRX need to support the Link Rate and Lane Count required by the test; Verify that a DP Link is established.
10.4.14.1#2	NT	The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Entering DP IN PHY Test Mode: The DP IN Adapter shall enter DP IN PHY Test Mode when the DPTX writes a non-zero value to LINK_QUAL_LANE <sub>Ex</sub> _SET in the DPCD registers.
10.4.14.1#3	NT	The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: While in DP IN PHY Test Mode: The DP IN Adapter shall keep the Hot Plug Detect signal high; The DP IN Adapter shall respond to all AUX transactions related to the PHY layer testing.

10.4.14.1#4	NT	The PHY layer of a DP IN Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Exiting DP IN PHY Test Mode: The DP IN Adapter shall exit DP IN PHY Test Mode when the DPTX initiates DP Link Training.
<b>10.4.14.2 DP OUT Adapter PHY Layer Testing</b>		
10.4.14.2#1	NT	The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Before entering DP OUT PHY Test Mode: Connect a Router with a DP IN Adapter and a DPTX. Both the DP IN Adapter and the DPTX need to support the test required Link Rate and Lane Count; Verify that a DP Link is established.
10.4.14.2#2	NT	The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Entering DP OUT PHY Test Mode: When the DPTX reads the following sequence, the DP IN Adapter shall send a SET_CONFIG Packet of Type SET_PHY_TEST_MODE and enter DP OUT PHY Test Mode: AUTOMATED_TEST_REQUEST is set to 1b (DPCD 00201h or 02003h bit 1); PHY_TEST_PATTERN is set to 1b (DPCD 00218h bit 3). The DP OUT Adapter shall enter DP OUT PHY Test Mode when it receives a SET_CONFIG Packet of type SET_PHY_TEST_MODE.
10.4.14.2#3	NT	The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: While in DP OUT PHY Test Mode: The DP OUT Adapter shall act as the DPTX under test; The DP OUT Adapter shall send HPD Packet with Plug Flag set to 0b; The DP IN Adapter shall not forward any AUX Transactions to the DP OUT Adapter.
10.4.14.2#4	NT	The PHY layer of a DP OUT Adapter shall be tested as described in the DisplayPort 1.4a PHY CTS with the changes listed below: Exiting DP OUT PHY Test Mode: Upon a DPRX HPD signal de-assertion: The DP OUT Adapter shall exit DP OUT PHY Test Mode; The Connection Manager tears down the DP Paths, causing both of the DP Adapters to enter the Present State.
<b>10.4.15 CLx Support</b>		
<b>10.4.15.1 AUX Paths</b>		
<b>10.4.15.1.1 CLx Entry</b>		
10.4.15.1.1#1		The AUX Path sleep handshake shall only be performed if the DP_COMMON_CAP.Protocol Adapter Version is equal 5.
10.4.15.1.1#2		A DP IN Adapter shall not initiate an AUX Path sleep handshake while it is waiting for an AUX Response from the DP OUT Adapter.

10.4.15.1.1#3		A DP IN Adapter initiates the AUX Path sleep handshake by performing the following steps: If the DP_COMMON_CAP.ALPM Support bit is 1b and the USB4 CL1 Granted through ALPM bit in the DPCD Tunnel POWER MANAGEMENT CONFIGURATION (address E0032h bit 0) is set to 1b, a DP IN Adapter shall send a PM Packet with the CLx State field set to 01b over the AUX Path.
10.4.15.1.1#4		A DP OUT Adapter that receives a SET_CONFIG Packet of type AUX_PATH_CLX with S/W bit set to 1b shall: 1. Send the ACK Packet for the SET_CONFIG Packet.
10.4.15.1.1#5		A DP OUT Adapter that receives a SET_CONFIG Packet of type AUX_PATH_CLX with S/W bit set to 1b shall: 2. Send a PM Packet with the CLx State field set to 01b over the AUX Path within tDPAUXSleepHS.
<b>10.4.15.1.2 CLx Exit</b>		
10.4.15.1.2#1		If a DP IN Adapter initiates an AUX Path sleep handshake and does not send a SET_CONFIG Packet over the AUX Path after completing the handshake, then upon reception of an AUX Request, the DP IN Adapter shall send a SET_CONFIG Packet of type AUX_PATH_CLX with the S/W bit set to 0b.
10.4.15.1.2#2		The following rules determine when the SET_CONFIG Packet shall be sent: If the DP IN Adapter sent a PM Packet with the <i>CLx State</i> field set to 01b as part of the last AUX Path sleep handshake, then it shall send the SET_CONFIG Packet within tDPAUXtoWAKE after receiving the end of the AUX_SYNC pattern of the AUX Request.
10.4.15.1.2#3		The following rules determine when the SET_CONFIG Packet shall be sent: Else it shall send the SET_CONFIG Packet within tDPAUXDelayIn after receiving the complete AUX Request.
<b>10.4.15.2 Main-Link Path</b>		
<b>10.4.15.2.1 ALPM Flow</b>		
10.4.15.2.1#1		A DP IN Adapter shall send a PM Packet with the CLx State field set to 01b over the Main-Link Path during the ALPM sleep sequence flow as described in Section 10.5.7.2.

<b>10.4.15.2.2 Inactive Main-Link</b>		
<b>10.5 High Speed Tunneling</b>		
<b>10.5.1 SST Tunneling</b>		
<b>10.5.1.1 Video Data Packet</b>		
<b>10.5.1.1.1 Transfer Unit Set</b>		
10.5.1.1.1#1	NT	A DP IN Adapter shall pack the active pixel data of a TU into either one or two TU Sets.
10.5.1.1.1#2	NT	When EOC control link symbols are present in a TU, a DP IN Adapter shall pack the EOC symbols using the same scheme as for active pixel symbols.
10.5.1.1.1#3	NT	The EOC symbols shall be packed in their 8-bit value representation (DCh).
10.5.1.1.1#4	NT	Each TU Set shall be prepended with a TU Set Header.
10.5.1.1.1#5	NT	The header in Figure 10-26(A) shall be used for a TU Set that contains a TU with no EOC Symbol.
10.5.1.1.1#6	NT	The header in Figure 10-26(B) shall be used for a TU Set that contains a TU with an EOC symbol.
10.5.1.1.1#7	NT	The fields forming the TU Set Header shall be as defined below: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the TU Set Header.
10.5.1.1.1#8	NT	The fields forming the TU Set Header shall be as defined below: <b>Video Count [13:8]</b> : When TU Type = 00b (active pixel line), if the TU Set does not contain an EOC symbol, this field shall contain the number of active video symbols per lane. If the TU Set contains an EOC symbol, this field shall contain the number of active video symbols per lane plus 1. A value of zero represents 64. The total number of active video symbols in the TU Set is equal to (Video Count * Number of Lanes).
10.5.1.1.1#9		The fields forming the TU Set Header shall be as defined below: When TU Type = 01b (dummy pixel line), if the TU Set does not contain an EOC symbol, this field shall contain the number of dummy data symbols per lane. If the TU Set contains an EOC symbol, this field shall contain the number of dummy data symbols per lane plus 1. A value of zero represents 64.
10.5.1.1.1#10	NT	The fields forming the TU Set Header shall be as defined below: <b>(No EOC) Fill Count [27:14]</b> : This field shall have the value as defined in 10.5.1.5.
10.5.1.1.1#11	NT	The fields forming the TU Set Header shall be as defined below: <b>(EOC) Fill Count [21:14]</b> : This field shall have the value as defined in 10.5.1.5.



10.5.1.1.1#12	NT	The fields forming the TU Set Header shall be as defined below: <b>(EOC) EOC Index [27:22]</b> : This field shall contain the index of the EOC symbol inside the TU Set. Symbols within a TU Set are indexed starting with zero (for the first symbol) and ending with (Video Count – 1) for the last symbol.
10.5.1.1.1#13	NT	The fields forming the TU Set Header shall be as defined below: <b>L [Bit 28]</b> : Last TU Flag. This flag shall be set to 1b if the TU is the last TU Set of a line. Otherwise shall be set to 0b.
10.5.1.1.1#14	NT	The fields forming the TU Set Header shall be as defined below: <b>TU Type [30:29]</b> : 00b – A TU Set that is part of an active pixel line; 01b – A TU Set that is part of a dummy pixel line; 10b-11b – Reserved.
10.5.1.1.1#15	NT	The fields forming the TU Set Header shall be as defined below: <b>EOC [Bit 31]</b> : This field shall be set to 1b if the TU Set contains an EOC symbol. Otherwise shall be set to 0b
10.5.1.1.1#16		When a DP IN Adapter supports Panel Replay Tunneling Optimization and it receives K28.7, it shall pack all the TUs within the dummy pixel line into TU Sets according to the same rules that are defined for a normal TU (i.e. a TU with an active pixel line) with the following exceptions: The TU Type shall be set to 01b.
10.5.1.1.1#17		When a DP IN Adapter supports Panel Replay Tunneling Optimization and it receives K28.7, it shall pack all the TUs within the dummy pixel line into TU Sets according to the same rules that are defined for a normal TU (i.e. a TU with an active pixel line) with the following exceptions: The dummy data symbols shall not be packed into the TU Set.
10.5.1.1.1#18		When a DP IN Adapter supports Panel Replay Tunneling Optimization and it receives K28.7, it shall pack all the TUs within the dummy pixel line into TU Sets according to the same rules that are defined for a normal TU (i.e. a TU with an active pixel line) with the following exceptions: If EOC is present, its 8-bit representation (DCh), shall not be sent.
10.5.1.1.1#19		A DP OUT Adapter shall generate a BE control symbol before the first TU of an active or dummy pixel line, for both TU Type values 00b and 01b.
<b>10.5.1.1.2 Packet Format</b>		
10.5.1.1.2#1	NT	A Video Data Packet shall have the format shown in Figure 10-28.
10.5.1.1.2#2	NT	All TU Set headers within the Video Data Packet payload shall be aligned to 32-bits by adding padding bytes at the end of the TU set payload if necessary.
10.5.1.1.2#3	NT	A DP IN Adapter shall follow the rules below when constructing a Video Data Packet: A Video Data Packet shall contain at least 1 TU Set and no more than 16 TU Sets. If a TU cannot fit within a single Video Data Packet, it shall be split into two TU sets.

10.5.1.1.2#4	NT	A DP IN Adapter shall follow the rules below when constructing a Video Data Packet: When a TU is split into two TU Sets, the remainder of the active pixel symbols shall be sent in the first TU Set in the next Video Data Packet. The <i>Fill Count</i> field in the TU Set Header of the second Video Data Packet for a TU that is split into multiple Video Data Packets shall be set to 0.
10.5.1.1.2#5	NT	A DP IN Adapter shall follow the rules below when constructing a Video Data Packet: The length of all TU Set Padding is included when calculating the <i>Length</i> field in the Tunneled Packet header.
<b>10.5.1.2 Main Stream Attribute Packet</b>		
10.5.1.2#1	NT	A Main Stream Attribute Packet shall consist of an MSA header followed by packet payload.
10.5.1.2#2	NT	The packet payload shall contain the encoding of the 36-byte attribute information following the <SS, SS> control symbol pair.
10.5.1.2#3	NT	The fields forming an MSA Header shall be as defined below: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the MSA Header.
10.5.1.2#4	NT	The fields forming an MSA Header shall be as defined below: <b>Fill Count [24:8]</b> : This field shall contain the fill count as defined in Section 10.5.1.5.
10.5.1.2#5	NT	The fields forming an MSA Header shall be as defined below: <b>Reserved [31:25]</b> : Reserved.
10.5.1.2#6	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Verify the <i>ECC</i> field in the MSA header. If an uncorrectable error has occurred, the Main Stream Attribute Packet shall be dropped and ignored.
10.5.1.2#7	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Send Fill Count number of Stuffing Symbols on all lanes of the DP Main-Link according to Section 10.5.1.5.
10.5.1.2#8	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Send the control symbol pair <SS, SS> on all lanes of the DP Main-Link.
10.5.1.2#9	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Send the stream attribute information contained in the first 36 bytes of the payload of the Main Stream Attribute Packet by steering bytes from the payload onto the lanes of the DP Main-Link in a round robin fashion starting with lane 0.
10.5.1.2#10	NT	Upon receiving a Main Stream Attribute Packet, a DP OUT Adapter shall do the following: Send the control symbol <SE> on all lanes of the DP Main-Link.

10.5.1.3 Blank Start Packet		
10.5.1.3#1	NT	A Blank Start Packet shall consist of a Blank Start header followed by packet payload.
10.5.1.3#2	NT	The packet payload shall contain the encoding of all 4 sets of <VB-ID, Mvid 7:0, Maud 7:0>.
10.5.1.3#3	NT	The fields forming the Blank Start header shall be as defined below: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the Blank Start Header.
10.5.1.3#4	NT	The fields forming the Blank Start header shall be as defined below: <b>Fill Count [24:8]</b> : This field shall have the value as defined in Section 10.5.1.5.
10.5.1.3#5	NT	The fields forming the Blank Start header shall be as defined below: <b>Reserved [29:25]</b> : Reserved.
10.5.1.3#6	NT	The fields forming the Blank Start header shall be as defined below: <b>CP [30]</b> : Content Protection Flag shall be set to 1b if Blank Start DP Control Link Symbols sequence were <BS,CP,CP,BS> or <SR,CP,CP,SR>.
10.5.1.3#7	NT	The fields forming the Blank Start header shall be as defined below: <b>SR [31]</b> : Scrambler Reset Flag shall be set to 1b if Blank Start DP Control Link Symbols sequence were <SR,BF,BF,SR> or <SR,CP,CP,SR>.
10.5.1.3#8	NT	Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations: 1) Verify the <i>ECC</i> field at the Blank Start Header. If an uncorrectable error has occurred, the Blank Start Packet shall be dropped.
10.5.1.3#9	NT	Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations: 2) Generate Stuffing Symbols on each lane of the DP Main-Link according to the <i>Fill Count</i> field in the Blank Start Header and Section 10.5.1.5.
10.5.1.3#10	NT	Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations: 3) Generate control symbols on each lane of the DP Main-Link marking the start of the blanking period based on the <i>SR Flag</i> and <i>CP Flag</i> as shown in Table 10-12.
10.5.1.3#11	NT	Upon receiving a Blank Start Packet, a DP OUT Adapter shall perform the following operations: 4) Steer the three double-words of Blank Start Packet payload starting with the second double-word onto the Main-Link by interleaving a byte at a time onto the lanes of the DP Main-Link starting with lane 0.

10.5.1.4 Secondary Data Packet		
10.5.1.4.1 Secondary Transfer Unit		
10.5.1.4.1#1	NT	A DP IN Adapter shall pack secondary data into one or more Secondary Tus.
10.5.1.4.1#2	NT	Each Secondary TU shall be prepended with a Secondary TU Header.
10.5.1.4.1#3	NT	The fields forming the Secondary TU Header shall be as defined below: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [31:8] of the Secondary TU Header.
10.5.1.4.1#4	NT	The fields forming the Secondary TU Header shall be as defined below: <b>Secondary Count [13:8]</b> : This field shall contain the number of secondary data symbols per lane. A value of zero represent 64 if ND bit equals 0. The total number of secondary data symbols in the Secondary TU is equal to (Secondary Count * Number of Lanes).
10.5.1.4.1#5	NT	The fields forming the Secondary TU Header shall be as defined below: <b>Fill Count [27:14]</b> : This field shall have the value as defined in Section 10.5.1.5. When both the <i>NSS</i> and <i>NSE</i> fields are 0b, the <i>Fill Count</i> field is extended by one bit and is constructed as {EFC, Fill Count} where EFC is the most significant bit.
10.5.1.4.1#6	NT	The fields forming the Secondary TU Header shall be as defined below: <b>L [Bit 28]</b> : Last TU Flag. This flag shall be set to 1b if the Secondary TU is either the last TU before a split or the TU represents the Secondary End Symbol. Otherwise it shall be set to 0b.
10.5.1.4.1#7	NT	The fields forming the Secondary TU Header shall be as defined below: <b>NSE [Bit 29]</b> : No Secondary End. This bit shall be set to 1b if Last TU Flag is set to 1b and a Secondary End Control symbol is not present at the DP Main-link. Otherwise it shall be set to 0b.
10.5.1.4.1#8	NT	The fields forming the Secondary TU Header shall be as defined below: <b>NSS [Bit 30]</b> : No Secondary Start. This bit shall be set to 1b if this is the first Secondary TU after a non-Secondary Tunneled Packet and a Secondary Start Control symbol is not present at the DP Main-Link. Otherwise it shall be set to 0b.
10.5.1.4.1#9	NT	The fields forming the Secondary TU Header shall be as defined below: <b>EFC/ND [31]</b> : Extended Fill Count/No Data. This bit shall be set to 1b if the Secondary TU does not have any Secondary data.
10.5.1.4.1#10	NT	The fields forming the Secondary TU Header shall be as defined below: <b>EFC</b> : When both the <i>NSS</i> and <i>NSE</i> fields are 0b, this bit is used as an extension to the Fill Count field.

10.5.1.4.1#11	NT	The fields forming the Secondary TU Header shall be as defined below: <b>ND:</b> When either the <i>NSS</i> or <i>NSE</i> fields are 1b, this bit is used to indicate whether or not the Secondary TU has any Secondary data. This bit shall be set to 1b if the Secondary TU does not contain Secondary data. If the Secondary TU contains Secondary data, this bit shall be set to 0b.
10.5.1.4.1#12	NT	A DP IN Adapter shall start packing secondary data into a Secondary TU in the following cases: A single Secondary Start Control symbol <SS> is present on the DP Main-link.
10.5.1.4.1#13	NT	A DP IN Adapter shall start packing secondary data into a Secondary TU in the following cases: The previous Secondary TU has reached the maximum capacity and the secondary data continues.
10.5.1.4.1#14	NT	A DP IN Adapter shall start packing secondary data into a Secondary TU in the following cases: The secondary data is split (as defined by the DisplayPort 1.4a Specification) by a non-Secondary Data Packet and this packet has now ended.
10.5.1.4.1#15	NT	A DP IN Adapter shall stop packing secondary data into a Secondary TU upon one of the following cases: Secondary End Control symbol <SE> is present on the DP Main-link.
10.5.1.4.1#16	NT	A DP IN Adapter shall stop packing secondary data into a Secondary TU upon one of the following cases: Maximum capacity is reached: For 1-Lane and 2-Lanes links: maximum capacity is reached when the <i>Secondary Count</i> field is 64; For 4-Lane links: maximum capacity is reached when the <i>Secondary Count</i> field is 62.
10.5.1.4.1#17	NT	A DP IN Adapter shall stop packing secondary data into a Secondary TU upon one of the following cases: Secondary data stream was split by MSA, BS or Active video as defined in the DisplayPort 1.4a Specification.
10.5.1.4.1#18	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 1) Verify the <i>ECC</i> field in the Secondary TU Header. If an uncorrectable error has occurred, the whole Secondary TU and the subsequent TUs within that packet shall be dropped and ignored.
10.5.1.4.1#19	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 2) Send Fill Count number of Stuffing Symbols on all lanes of the DP Main-Link according to Section 10.5.1.5.
10.5.1.4.1#20	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 3) If this Secondary TU is the first Secondary TU to follow a non-Secondary Data Packet and the <i>NSS</i> bit is not set in the Secondary TU Header, send the control symbol <SS> on all lanes of the DP Main-Link.

10.5.1.4.1#21	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 4) Send the secondary data contained in the Secondary TU. The number of cycles of data shall be as according to the <i>Secondary Count</i> field in the Secondary TU Header. The secondary data shall be sent on the DP Main-Link by steering bytes from the payload onto the lanes in a round robin fashion starting with lane 0.
10.5.1.4.1#22	NT	Upon receiving a Secondary Data Packet, a DP OUT Adapter shall do the following for each Secondary TU: 5) If the <i>L Flag</i> is set and the <i>NSE</i> bit is not set in the Secondary TU header, send the control symbol <SE> on all lanes of the DP Main-Link.
<b>10.5.1.4.2 Packet Format</b>		
10.5.1.4.2#1	NT	A Tunneled Secondary Data Packet shall have the format shown in Figure 10-34.
10.5.1.4.2#2	NT	A Tunneled Secondary Data Packet shall not include Secondary TUs from more than one DisplayPort SDP.
10.5.1.4.2#3	NT	All Secondary TU Headers within the Tunneled Secondary Data Packet payload shall be aligned to 32-bits by adding Secondary TU Padding bytes at the end of the Secondary TU payload if necessary.
<b>10.5.1.4.3 Secondary Data to Secondary TU Mapping Examples</b>		
<b>10.5.1.5 Fill Count</b>		
10.5.1.5#1	NT	DP IN Adapter shall calculate the <i>Fill Count</i> field according to the following formula: <i>Fill Count</i> field = Act_Fill_Count + DP_K_Prev_Pkt – Prev_Factor
10.5.1.5#2	NT	The following cycles shall be counted as the Act_Fill_Count: Stuffing Symbols; BE - Blanking End; FS - Filling Start; FE - Filling End.
10.5.1.5#3	NT	A DP OUT Adapter shall use the following formula to calculate the actual number of Stuffing Symbols to be driven over the DP link: Act_Fill_Count = <i>Fill Count</i> field + Prev_Factor – DP_K_Prev_Pkt
10.5.1.5#4	NT	A DP OUT Adapter shall ignore the <i>Fill Count</i> field in the first Tunneled Packet sent on the Main-Link Path after DP link training.
<b>10.5.2 8b/10b MST Tunneling</b>		
<b>10.5.2.1 Sub-MTP TU</b>		
10.5.2.1#1	NT	A Sub-MTP TU Header shall have the format shown in Figure 10-38.
10.5.2.1#2	NT	The fields forming the Sub-MTP TU Header shall be as defined below: <b>ECC [7:0]</b> : Error correction field that is calculated over bits [23:8] of the Sub-MTP TU Header.

10.5.2.1#3	NT	The fields forming the Sub-MTP TU Header shall be as defined below: <b>Data Count[13:8]</b> : This field shall contain the number of Data symbols per lane. The total number of Data symbols in the Sub-MTP TU is equal to ( <i>Data Count</i> * Number of Lanes).
10.5.2.1#4	NT	The fields forming the Sub-MTP TU Header shall be as defined below: <b>Type[17:14]</b> : This field shall contain the Type encoding of the Sub-MTP TU.
10.5.2.1#5	NT	The fields forming the Sub-MTP TU Header shall be as defined below: <b>Slot Number[23:18]</b> : This field shall contain the first slot number in the MTP which this Sub-MTP TU Header is describing.
10.5.2.1#6	NT	A DP IN Adapter that receives an MST stream shall perform the DisplayPort PHY layer and De-scrambler functions defined in the DisplayPort 1.4a Specification.
10.5.2.1#7	NT	Upon reception of the first SR after link training completion, a DP IN Adapter shall: Track the total number of allocated MST slots by snooping any DPCD AUX transactions that configure the VC Payload ID Table.
10.5.2.1#8	NT	Upon reception of the first SR after link training completion, a DP IN Adapter shall: Start mapping MTP from the DP Main-Link into Sub-MTP TUs.
10.5.2.1#9	NT	When a Parameter includes a Data byte, the DP IN Adapter shall append the de-scrambled Data byte as the Parameter.
10.5.2.1#10	NT	A DP IN Adapter shall pack the Data bytes by selecting a byte from each Lane of the Main-Link in a cyclic way, starting with lane 0.
10.5.2.1#11	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: A Sub-MTP TU is byte-aligned.
10.5.2.1#12	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: The total length of a Sub-MTP TU (Header + Parameter Bytes + Data Bytes) does not exceed 252 Bytes.
10.5.2.1#13	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: Slot 0 always starts a new Sub-MTP TU.
10.5.2.1#14	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: A Sub-MTP TU includes data from one MTP only.
10.5.2.1#15	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: A DP IN Adapter shall map an MTP into the minimum possible number of Sub-MTP TU.
10.5.2.1#16	NT	A DP IN Adapter shall follow the rules below when constructing a Sub-MTP TU: A Sub-MTP TU shall be split into 2 Sub-MTP TUs if it does not fit into an MTP packet according to Section 10.5.2.3.

10.5.2.2 MTP to Sub-MTP TU Examples		
10.5.2.2.2 Shifting SR		
10.5.2.2.2#1	NT	Upon detecting a sequence of four consecutive SR with 216 time-slot intervals, a DP IN Adapter shall switch to the new SR location.
10.5.2.2.2#2	NT	The first three SR that are not at Slot Zero's original location shall be mapped to a non-zero Slot Type 8 (1 K-Symbol), for the case of 1-lane, carrying Parameter byte = 8 (as defined in Table 10-17).
10.5.2.2.2#3	NT	The fourth SR shall be mapped to a non-zero Slot Type 1 (Shifting SR) forcing the next slot to be slot number 1.
10.5.2.2.2#4	NT	For the case of 2-Lane DP links, the first three SR shall be mapped to Type 9 (2 K-Symbols).
10.5.2.2.2#5	NT	For the case of and 4-Lane DP links, the first three SR shall be mapped to Type 11 (4 K-Symbols).
10.5.2.2.3 ACT		
10.5.2.2.4 SF, AVF, and VCPF		
10.5.2.2.4#1	NT	A DP IN Adapter shall not map an SF sequence into a Sub-MTP TU unless the SF sequence comes immediately after a VCPF or an AVF sequence.
10.5.2.3 MST Packet Format		
10.5.2.3#1	NT	An MST Packet shall have the format shown in Figure 10-46.
10.5.2.3#2	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: The first 3 bytes of the MST Packet payload contains the first Sub-MTP TU Header.
10.5.2.3#3	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: When concatenating two Sub-MTP TUs, the first TU is not be padded.
10.5.2.3#4	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: The maximum number of MTPs packed into one MST Packet does not exceed 17.
10.5.2.3#5	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: The <i>Length</i> field in the Tunneled Packet Header does not include padding bytes.
10.5.2.3#6	NT	A DP IN Adapter shall follow the rules below when constructing an MST Packet: The Payload of the Tunneled Packet shall be between 230 and 252 Bytes (inclusive), unless the Payload contains at least 16 MTPs.



<b>10.5.2.4 MST Packets to DP MTP</b>		
10.5.2.4#1	NT	A DP OUT Adapter shall analyze each Sub-MTP TU Header and recreate the MTP K-Code and data bytes according to Table 10-16 (for slot zero) or Table 10-17 (for non-zero slots).
10.5.2.4#2	NT	If a DP OUT Adapter has a slot for which it lacks sufficient information to recreate the MTP K-Code and/or data bytes, it shall follow the rules below: If the last Sub-MTP TU Header was VCPF, insert VCPF.
10.5.2.4#3	NT	If a DP OUT Adapter has a slot for which it lacks sufficient information to recreate the MTP K-Code and/or data bytes, it shall follow the rules below: If the last Sub-MTP TU Header was Unallocated, insert unallocated (data bytes equal zero).
10.5.2.4#4	NT	If a DP OUT Adapter has a slot for which it lacks sufficient information to recreate the MTP K-Code and/or data bytes, it shall follow the rules below: For all other cases, insert SF.
10.5.2.4#5	NT	After creating the MTPs, the DP OUT Adapter shall follow all the PHY Layer functions required by the DisplayPort 1.4a Specification.
10.5.2.4#6		If a DP OUT Adapter supports Panel Replay optimization, then the following exceptions apply when recreating the MTP K-Code and data bytes according to the incoming Sub-MTP TUs: If the Sub-MTP TU Header is AVF, a DP OUT Adapter shall insert dummy pixel data.
10.5.2.4#7		If a DP OUT Adapter supports Panel Replay optimization, then the following exceptions apply when recreating the MTP K-Code and data bytes according to the incoming Sub-MTP TUs: If the Sub-MTP TU Header is either 1 K-Symbol, 2 K-Symbol, 3 K-Symbol or 4 K-Symbol, then for every K-Symbol index that equals 7, a DP OUT Adapter shall insert dummy pixel data.
10.5.2.4#8		If a DP OUT Adapter has a slot for which it lacks sufficient information to recreate the MTP K-Code and/or data bytes, it shall follow the rules below: If the last Sub-MTP TU Header was AVF, insert dummy pixel data.
<b>10.5.3 128b/132b Tunneling</b>		
<b>10.5.3.1 128b/132b LLC P Encapsulation</b>		
10.5.3.1#1		Upon reception of Link Layer Control Packet (LLCP) over the DisplayPort Main-Link, a DP IN Adapter shall send a 128b/132b LLC P Packet. A 128b/132b LLC P Packet has the PDF field in the Tunneled Packet Header set to 8h.
10.5.3.1#2		A 128b/132b LLC P Packet shall consist of a 128b/132b LLC P Header followed by six DWs that contain the three LLC P Data Link Symbols that were received over the DisplayPort Main-Link.

10.5.3.1#3		The fields forming a 128b/132b LLC Header shall be as defined below: <b>Allocated Slots [7:0]</b> : The number of allocated time slots within each MTP in the Link Layer Frame associated with the LLC.
10.5.3.1#4		The fields forming a 128b/132b LLC Header shall be as defined below: <b>Gap Counter [24:8]</b> : This field shall contain the number of 128b/132b Link Symbol Clocks between the first LLC_MARKER symbol of the current LLC and the first LLC_MARKER symbol of the previous LLC.
10.5.3.1#5		The fields forming a 128b/132b LLC Header shall be as defined below: The Gap Counter of the first LLC Packet sent after link training shall be set to 0h.
10.5.3.1#6		The fields forming a 128b/132b LLC Header shall be as defined below: The Gap Counter of the first LLC Packet sent after an ALPM wake sequence shall be set to 0h.
10.5.3.1#7		The fields forming a 128b/132b LLC Header shall be as defined below: The Gap Counter shall be set to 0x1FFFF if the count is greater than 0x1FFFF.
10.5.3.1#8		The fields forming a 128b/132b LLC Header shall be as defined below: <b>Reserved [31:25]</b> : Reserved.
10.5.3.1#9		A DP IN Adapter shall map the LVP field received on the DisplayPort Link Layer lane X to the LVP – Lane X field, since the LVP field may be different for each DisplayPort Link Layer lane.
<b>10.5.3.2 Time Slot Allocation</b>		
10.5.3.2#1		Upon reception of an LLC Packet with the <i>ACT</i> bit set to 1b over the DisplayPort Main-Link, a DP IN Adapter shall update the <i>Allocated Slots</i> field in the 128b/132b LLC Header according to the snooped AUX transactions.
10.5.3.2#2		If the <i>ACT</i> bit is set to 0b, a DP IN Adapter shall set the <i>Allocated Slots</i> field to the same value it sent in the previous LLC Packet.
10.5.3.2#3		If an LLC Packet is the first received LLC Packet and the <i>ACT</i> bit is set to 0b, a DP IN Adapter shall set the <i>Allocated Slots</i> field to 0h.
<b>10.5.3.3 128b/132b MTP Encapsulation</b>		
10.5.3.3#1		When the number of allocated time slots is not zero and the last received <i>Link Layer End Indicator</i> bit was set to 0b: A DP IN Adapter shall pack the Data and Control symbols into a Tunneled Packet in the same order as received over the 128b/132b DisplayPort Link.

10.5.3.3#2		When the number of allocated time slots is not zero and the last received <i>Link Layer End Indicator</i> bit was set to 0b: A DP IN Adapter shall pack the Data Link Symbols into a Tunneled Packet by selecting a Data Link Symbol from each Lane of the DP Main-Link in a cyclic way, starting with Lane 0.
10.5.3.3#3		When the number of allocated time slots is zero or the last received <i>Link Layer End Indicator</i> bit was set to 1b, a DP IN Adapter shall not send 128b/132b Data Packet and 128b/132b Control and Data Packet.
<b>10.5.3.3.1 128b/132b Control and Data Packet</b>		
10.5.3.3.1#1		A 128b/132b Control and Data Packet shall have the format shown in Figure 10-52.
10.5.3.3.1#2		A DP IN Adapter shall follow the rules below when constructing an 128b/132b Control and Data Packet: The Tunneled Packet shall include at least one 128b/132b Control TU.
10.5.3.3.1#3		A DP IN Adapter shall follow the rules below when constructing an 128b/132b Control and Data Packet: The first doubleword in the payload contains a 128b/132b TU Header.
10.5.3.3.1#4		A DP IN Adapter shall follow the rules below when constructing an 128b/132b Control and Data Packet: The Tunneled Packet shall not include two consecutive Control TUs with the same Control Type field.
10.5.3.3.1#5		A DP IN Adapter shall follow the rules below when constructing an 128b/132b Control and Data Packet: The Tunneled Packet shall not include two consecutive Data TUs.
10.5.3.3.1#6		A DP IN Adapter shall follow the rules below when constructing an 128b/132b Control and Data Packet: The number of consecutive time slots (both allocated and unallocated) described by the Tunneled Packet shall not exceed 128 time slots. If the data of a time slot is split between two Tunneled Packets, the time slot is counted by each of the Tunneled Packets.
10.5.3.3.1#7		A DP IN Adapter shall follow the rules below when constructing an 128b/132b Control and Data Packet: A DP IN Adapter shall concatenate 128b/132b TUs into a single Tunneled Packet until one of the following conditions are true, resulting sending the Tunneled Packet: The Tunneled Packet payload size is either 248 or 252 bytes; The maximum number (128) of allowed time slots described by the Tunneled Packet is reached; An LLCp was received.
<b>10.5.3.3.1.1 128b/132b Transfer Unit</b>		
10.5.3.3.1.1#1		A 128/132b TU Header shall have the format shown in Figure 10 53.

10.5.3.3.1.1#2		The fields forming the 128b/132b TU Header shall be as defined below: <b>Control Type [3:0]</b> : For a Control TU, this field shall contain the value that represents the Control Link Symbol as defined in Table 10-22. For a Data TU this field shall be set to 0.
10.5.3.3.1.1#3		The fields forming the 128b/132b TU Header shall be as defined below: <b>Reserved [6:4]</b> : Reserved.
10.5.3.3.1.1#4		The fields forming the 128b/132b TU Header shall be as defined below: <b>Data TU [7]</b> : This bit identifies the 128b/132b TU type: 0b – Indicates a 128b/132b Control TU; 1b – Indicates a 128b/132b Data TU.
10.5.3.3.1.1#5		The fields forming the 128b/132b TU Header shall be as defined below: <b>Count [15:8]</b> : For a 128b/132b Data TU, this field shall contain the number of Data DWs following the 128b/132b TU Header. For a 128b/132b Control TU, this field shall contain the number of allocated time slots carrying the same Control symbol. This field shall have a value greater than zero.
10.5.3.3.1.1#6		The fields forming the 128b/132b TU Header shall be as defined below: <b>Reserved [31:16]</b> : Reserved.
10.5.3.3.1.1#7		A DP IN Adapter shall follow the rules below when constructing a 128b/132b TU: A 128b/132b TU shall be doubleword-aligned.
10.5.3.3.1.1#8		A DP IN Adapter shall follow the rules below when constructing a 128b/132b TU: The total length of a 128b/132b TU shall not exceed 252 Bytes.
10.5.3.3.1.1#9		A DP IN Adapter shall follow the rules below when constructing a 128b/132b TU: A 128b/132b TU may include data from up to 128 consecutive time slots.
10.5.3.3.1.1#10		A DP IN Adapter shall follow the rules below when constructing a 128b/132b TU: A 128b/132b TU shall not include data from more than 128 consecutive time slots.
<b>10.5.3.3.2 128b/132b Data Packet</b>		
10.5.3.3.2#1		A 128b/132b Data Packet shall have the format shown in Figure 10 54.
10.5.3.3.2#2		A DP IN Adapter shall pack Data Symbols into a single Packet until one of the below conditions are true, resulting sending the Tunneled Packet: The Tunneled Packet payload size is either 248 or 252 bytes; The maximum number of time slots (both allocated and unallocated) described by the Tunneled Packet reached the maximum allowed (128 time slots). If the data of a time slot is split between two Tunneled Packets, the time slot is counted by each of the Tunneled Packets; An LLC/P was received.

<b>10.5.3.4 128b/132b Encapsulation Examples</b>		
<b>10.5.3.4.1 No Time Slots are Allocated</b>		
10.5.3.4.2 MSA Packet Encapsulation		
10.5.3.4.3 128b/132b Data Only, 128 Time Slots		
10.5.3.4.4 128b/132b Data Only, 252 Bytes		
10.5.3.4.5 128b/132b Data and Control, 128 Time Slots		
<b>10.5.4 FEC Functionality</b>		
10.5.4.1 8b/10b FEC		
<b>10.5.4.1.1 SR Count</b>		
10.5.4.1.1#1	NT	A DP Adapter shall implement the SR Count counter, which counts the number of cycles that have elapsed since the last SR.
10.5.4.1.1#2	NT	A DP IN Adapter shall initiate the SR Count at the first cycle after receiving an SR.
10.5.4.1.1#3	NT	A DP OUT Adapter shall initiate the SR Count at the first cycle after transmitting an SR.
<b>10.5.4.1.2 DP IN Adapter Requirements</b>		
10.5.4.1.2#1	NT	A DP IN Adapter shall: Implement FEC Decoding as defined in the DisplayPort 1.4a Specification.
10.5.4.1.2#2	NT	A DP IN Adapter shall: Construct an FEC_DECODE Packet as defined in Section 10.5.4.4 upon FEC_DECODE_EN or FEC_DECODE_DIS sequence detection.
10.5.4.1.2#3	NT	A DP IN Adapter shall: The Adapter Layer shall prioritize the FEC_DECODE Packet over all other Main-Link Path packets when pass it to the Transport Layer.
10.5.4.1.2#4	NT	A DP IN Adapter shall not: Tunnel any FEC-related symbols including FEC_PARITY_MARKER, FEC_DECODE & FEC_PARITY_PH.
10.5.4.1.2#5	NT	A DP IN Adapter shall not: Count the Link cycles of FEC Symbols for fill count purposes.
<b>10.5.4.1.3 DP OUT Adapter Requirements</b>		
10.5.4.1.3#1	NT	A DP OUT Adapter shall: Implement FEC Encoding as defined in the DisplayPort 1.4a Specification.

10.5.4.1.3#2	NT	A DP OUT Adapter shall: Apply majority voting for the repeated fields with in the FEC_DECODE Packet: SR Count; FEN; FDS.
10.5.4.1.3#3	NT	A DP OUT Adapter shall: Generate FEC_DECODE_EN and FEC_DECODE_DIS upon reception of a FEC_DECODE Packet.
10.5.4.1.3#4	NT	FEC_DECODE_EN sequence shall be generated if <i>FEN</i> field in the FEC_DECODE Packet is 1b.
10.5.4.1.3#5	NT	FEC_DECODE_DIS sequence shall be generated if <i>FDS</i> fields in the FEC_DECODE Packet is 1b.
10.5.4.1.3#6	NT	The first symbol of the FEC_DECODE_EN and FEC_DECODE_DIS sequences shall be transmitted according to the <i>SR Count</i> field of the FEC_DECODE Packet, i.e. the FEC_DECODE_EN and FEC_DECODE_DIS sequence shall be transmitted <i>SR Count</i> link clock cycles after the most recently transmitted SR.
10.5.4.1.3#7	NT	When a FEC_DECODE Packet is received, a DP OUT Adapter compares the Packet SR Count and the Counter SR Count as follows: If Packet SR Count > Counter SR Count the DP OUT Adapter waits for the Counter SR Count to be equal to Packet SR Count then generate the FEC sequence.
10.5.4.1.3#8	NT	When a FEC_DECODE Packet is received, a DP OUT Adapter compares the Packet SR Count and the Counter SR Count as follows: Else, a DP OUT Adapter waits for next SR to be transmitted, then waits for the Counter SR Count to be equal to Packet SR Count then generate the FEC sequence.
10.5.4.1.3#9	NT	A DP OUT Adapter shall not: Count the Link cycles of FEC Symbols for fill count purposes.
<b>10.5.4.1.4 FEC_DECODE Packet</b>		
10.5.4.1.4#1	NT	A FEC_DECODE Packet shall have the format shown in Figure 10-60.
10.5.4.1.4#2	NT	The <i>PDF</i> field in the header shall be set to 7 and the <i>Length</i> field shall be 14h.
10.5.4.1.4#3	NT	An FEC Command shall have the format defined in Figure 10-61.
10.5.4.1.4#4	NT	The three FEC Commands in an FEC_DECODE Packet shall be identical to each other.
10.5.4.1.4#5	NT	The fields in an FEC Command shall contain the following: <b>SR Count [29:0]</b> : This field contains the number of DP Link clock cycles between the last received SR and the first FEC_DECODE_EN or FEC_DECODE_DIS sequences. The minimum value for this field is 1h. (occurs when SR is immediately followed by FEC_DECODE sequence).

10.5.4.1.4#6	NT	The fields in an FEC Command shall contain the following: <b>FEC DISABLE (FDS) [30]</b> : This field shall be set to 1b if a FEC_DECODE_DIS sequence was detected. In all other cases it shall be set to 0b.
10.5.4.1.4#7	NT	The fields in an FEC Command shall contain the following: <b>FEC ENABLE (FEN) [31]</b> : This field shall be set to 1b if a FEC_DECODE_EN sequence was detected. In all other cases it shall be set to 0b.
<b>10.5.4.2 128b/132b FEC</b>		
10.5.4.2#1		A DP IN Adapter shall implement FEC Decoding as defined in the DisplayPort 1.4a Specification.
10.5.4.2#2		A DP IN Adapter shall not tunnel any FEC-related symbols including RS Parity symbols and the associated padding bits.
10.5.4.2#3		A DP OUT Adapter shall implement FEC Encoding as defined in the DisplayPort 1.4a Specification.
<b>10.5.5 DP OUT Adapter Buffer</b>		
10.5.5#1	NT	A DP OUT Adapter shall implement a buffer that can be used to compensate for the jitter in the latency of the received Tunneled Packets.
10.5.5#2	NT	Deprecated.
10.5.5#3	NT	The DP OUT Adapter transitions from sending self-generated idle pattern to reconstructing the DP Main-Link from the Tunneled Packets after completing the following steps: 1) The DP OUT Adapter shall adjust the PLL frequency at least once as a result of an Adjust PLL event as described in Section 10.6.
10.5.5#4	NT	The DP OUT Adapter transitions from sending self-generated idle pattern to reconstructing the DP Main-Link from the Tunneled Packets after completing the following steps: 2) The DP OUT Adapter ensures, in an implementation specific manner, that within eight PLL frequency adjustments the link symbol clock frequency difference between its own and the DPTX is such that buffer overflow and buffer underrun is avoided.
10.5.5#5	NT	The DP OUT Adapter transitions from sending self-generated idle pattern to reconstructing the DP Main-Link from the Tunneled Packets after completing the following steps: 3) The DP OUT Adapter shall wait to receive an SR (for 8b/10b DP Link) or an LLCP (for 128b/132b DP Link) from the DP IN Adapter.
10.5.5#6	NT	All Main-Link Path Tunneled Packets, besides DP Clock Sync Packets, are dropped by the DP OUT Adapter until reception of the SR (for 8b/10b DP Link) or an LLCP (for 128b/132b DP Link).

10.5.5#7	NT	After the next step is completed, the received SR (for 8b/10b DP Link) or an LLCp (for 128b/132b DP Link), shall be the first symbol driven by the DP OUT Adapter as the reconstructed Main-link.
10.5.5#8	NT	The DP OUT Adapter transitions from sending self-generated idle pattern to reconstructing the DP Main-Link from the tunneled packets after completing the following steps: 4) The DP OUT Adapter delays sending the SR (for 8b/10b DP Link) or an LLCp (for 128b/132b DP Link) in Step 3 for a number of Accumulation Cycles.
10.5.5#9	NT	During the delay, the DP OUT Adapter shall accumulate the DP Main-Link traffic from the DP IN Adapter.
<b>10.5.5.1 Buffer Operation</b>		
10.5.5.1#1	NT	If the buffer becomes empty, a DP OUT Adapter shall continue to drive Dummy Symbols on the DP Main Link, assuming that the next Main-Link Path Tunneled Packet holds a Fill Count value larger than the driven Dummy Cycles.
<b>10.5.5.2 Accumulation Cycles</b>		
10.5.5.2#1	NT	A DP OUT Adapter shall report the Maximum Accumulation Cycles it performs.
<b>10.5.6 HDCP</b>		
10.5.6#1	NT	A DP IN Adapter shall not perform HDCP decryption.
10.5.6#2	NT	It shall not drop or modify an AUX Request or AUX Response associated with HDCP functionality.
10.5.6#3	NT	A DP OUT Adapter shall not perform HDCP encryption.
<b>10.5.7 AUX-less Advanced Link Power Management (ALPM)</b>		
10.5.7#1		A DP Adapter that supports ALPM shall set the DP_LOCAL_CAP.ALPM Support bit to 1b.
10.5.7#2		A DP Adapter that does not supports ALPM shall set the DP_LOCAL_CAP.ALPM Support bit to 0b.
10.5.7#3		If ALPM is supported over a DP Tunnel, the DP Adapters shall support the sleep sequence defined in Section 10.5.7.2 and the wake sequence defined in Section 10.5.7.3.
<b>10.5.7.1 ALPM DP Link Control Packet</b>		
10.5.7.1#1		An ALPM DP Link Control Packet shall have the format shown in Figure 10-63.



10.5.7.1#2		The PDF field in the header shall be set to 11 and the Length field shall be 04h.
10.5.7.1#3		The fields forming the ALPM DP Link Control Packet payload shall be as defined below: S/W [0]: This bit indicates if this is a sleep or a wake packet. In a sleep sequence, this bit shall be set to 1b. In a wake sequence, it shall be set to 0b
10.5.7.1#4		The fields forming the ALPM DP Link Control Packet payload shall be as defined below: SR Count [23:1]: When operating with a 8b/10b DP Link and the S/W bit is set to 1b, this field contains the number of DP Link clock cycles between the last received SR and the first ML_PHY_SLEEP sequence. The minimum value for this field is 1h (occurs when SR is immediately followed by ML_PHY_SLEEP sequence). When operating with a 128b/132b DP Link or the S/W bit is set to 0, this field shall be set to 0h.
10.5.7.1#5		The fields forming the ALPM DP Link Control Packet payload shall be as defined below: Type [31:24]: This field shall be set to 01h, indicating that the packet is a DP Link Control Packet of type ALPM.
<b>10.5.7.2 Sleep Sequence</b>		
10.5.7.2#1		Upon reception of an ML_PHY_SLEEP sequence, as defined in the DisplayPort Specification, a DP IN Adapter shall perform the following sleep sequence: 1. Stop sending DP Clock Sync Packets.
10.5.7.2#2		Upon reception of an ML_PHY_SLEEP sequence, as defined in the DisplayPort Specification, a DP IN Adapter shall perform the following sleep sequence: 2. Send as Tunneled Packets, all the DP Main-Link constructs that were received prior to the ML_PHY_SLEEP.
10.5.7.2#3		Upon reception of an ML_PHY_SLEEP sequence, as defined in the DisplayPort Specification, a DP IN Adapter shall perform the following sleep sequence: 3. Send a DP Link Control Packet of type ALPM with the following fields: a. S/W – Set to 1b. b. SR Count – If the DP Link is 8b/10b then set to the number of cycles as described in Section 10.5.7.1. If the DP Link is 128b/132b then set to 0h.
10.5.7.2#4		Upon reception of an ML_PHY_SLEEP sequence, as defined in the DisplayPort Specification, a DP IN Adapter shall perform the following sleep sequence: 4.If USB4 CL1 Granted through ALPM bit in the DPCD Tunnel POWER MANAGEMENT CONFIGURATION (address E0032h bit 0) is set to 1b, the DP IN Adapter shall send a PM Packet with the CLx State field set to 01b over the Main-Link Path.
10.5.7.2#5		Upon reception of an ALPM DP Link Control Packet with the S/W bit set to 1b, a DP OUT Adapter shall perform the following sleep sequence:1.Store the current transmitter frequency.

10.5.7.2#6		Upon reception of an ALPM DP Link Control Packet with the S/W bit set to 1b, a DP OUT Adapter shall perform the following sleep sequence: 2. For a 128b/132b DP Link: Reconstruct the Tunneled Packets that were received prior to the ALPM DP Link Control Packet into DP native packets and transmit them over the DP Main Link; insert scrambled zeros to complete the FEC frame that includes the DP native packets from Step 2.
10.5.7.2#7		Upon reception of an ALPM DP Link Control Packet with the S/W bit set to 1b, a DP OUT Adapter shall perform the following sleep sequence: 3. For an 8b/10b DP Link, compare the Packet SR Count and the Counter SR Count as follows: If Packet SR Count > Counter SR Count, the DP OUT Adapter waits for the Counter SR Count to be equal to Packet SR Count; Else, a DP OUT Adapter waits for the next SR to be transmitted, then waits for the Counter SR Count to be equal to Packet SR Count. While performing this step, reconstruct the Tunneled Packets into DP native packets and transmit them over the DP Main Link
10.5.7.2#8		Upon reception of an ALPM DP Link Control Packet with the S/W bit set to 1b, a DP OUT Adapter shall perform the following sleep sequence: 4. Generate ML_PHY_SLEEP pattern as DPTX generates it, according to the DisplayPort Specification. A DP OUT Adapter generates the ML_PHY_SLEEP pattern according to the number of LTTPRs reported in the Downstream_LTTPRs field in the SET_LTTPR_MODE SET_CONFIG Packet it received from the DP IN Adapter.
<b>10.5.7.3 Wake Sequence</b>		
10.5.7.3#1		Upon detecting an LFPS, which is qualified as a wake signal according to the DisplayPort Specification, a DP IN Adapter shall send a DP Link Control Packet of type ALPM with the S/W bit set to 0b and the SR Count field set to 0h.
10.5.7.3#2		The DP IN Adapter shall send the DP Link Control Packet within tDPALPMWake after detecting the LFPS.
10.5.7.3#3		When a DP IN Adapter ends its PHY establishment and detects an ML_PHY_LOCK, as defined by DisplayPort Specification, it shall start converting DisplayPort Main-Link Symbols into Tunneled Packets after receiving an SR (for a 8b/10b DP Link) or an LLCp (for a 128b/132b DP Link).
10.5.7.3#4		After a DP IN Adapter sends the DP Link Control Packet of type ALPM with the S/W bit set to 0b, it shall: 1. Wait for ADP_DP_CS_13. <i>CLI Exit Time</i> .
10.5.7.3#5		After a DP IN Adapter sends the DP Link Control Packet of type ALPM with the S/W bit set to 0b, it shall: 2. Before advancing to Step 3, ensure it has ended its PHY establishment and detected an ML_PHY_LOCK.

10.5.7.3#6		After a DP IN Adapter sends the DP Link Control Packet of type ALPM with the S/W bit set to 0b, it shall: 3. Enable its Clock Synchronization – Start advancing the Lifetime Counter and send DP Clock Sync Packets as defined in Section 10.6.
10.5.7.3#7		Upon reception of an ALPM DP Link Control Packet with the S/W bit set to 0b, a DP OUT Adapter shall perform the following wake sequence: 1. Start generating the LFPS followed by ML_PHY_LOCK_LTTTPR pattern as the LTTTPR that is adjacent to the DPTX generates it, according to DisplayPort Specification. The DP OUT Adapter shall start generating LFPS within tDPALPMWake after receiving the ALPM DP Link Control Packet: DP OUT Adapter shall generate the ML_PHY_LOCK_LTTTPR pattern for tDCS, as defined in the DisplayPort Spec. The tDCS is calculated according to the number of LTTTPRs reported in the Downstream_LTTTPRs field in the SET_LTTTPR_MODE SET_CONFIG Packet it received from the DP IN Adapter; DP OUT Adapter shall activate its transmitters at the nominal frequency.
10.5.7.3#8		Upon reception of an ALPM DP Link Control Packet with the S/W bit set to 0b, a DP OUT Adapter shall perform the following wake sequence: 2. Complete the following within tACDS (tACDS is defined in DisplayPort specification): Transition the transmitters frequency from the nominal frequency to the same frequency it saved during the previous sleep sequence; Switch the transmitted pattern from ML_PHY_LOCK_LTTTPR to ML_PHY_LOCK.
10.5.7.3#9		Upon reception of an ALPM DP Link Control Packet with the S/W bit set to 0b, a DP OUT Adapter shall perform the following wake sequence: 3. For a 128b/132b DP Link, send 7*(Downstream_LTTTPRs + 1) ML_PHY_LOCK and then transition to 1-Bit CDI operation at the next PHY Sync symbol.
10.5.7.3#10		Upon reception of an ALPM DP Link Control Packet with the S/W bit set to 0b, a DP OUT Adapter shall perform the following wake sequence: 4. For a 8b/10b DP Link, continue transmitting ML_PHY_LOCK,
10.5.7.3#11		Upon reception of an ALPM DP Link Control Packet with the S/W bit set to 0b, a DP OUT Adapter shall perform the following wake sequence: 5. Start accumulating DP Main Link traffic coming from the DP IN Adapter after receiving an SR (for 8b/10b DP Link) or an LLCP (for 128b/132b DP Link). After accumulating for a number of Accumulation Cycles, A DP OUT Adapter shall start reconstructing the DP Main-Link from the Tunneled Packets.
10.5.7.3#12		Upon reception of an ALPM DP Link Control Packet with the S/W bit set to 0b, a DP OUT Adapter shall perform the following wake sequence: 6. After waiting for tCLxConvergeTime from the reception the ALPM DP Link Control Packet with the S/W bit set to 0b, enable its Clock Synchronization – Start advancing the Lifetime Counter.

<b>10.6 DP Link Clock Sync</b>		
<b>10.6.1 Synchronization Method</b>		
<b>10.6.1.1 Events</b>		
<b>10.6.1.1.1 Measuring Events</b>		
<b>10.6.1.1.2 Adjust PLL Event</b>		
<b>10.6.1.2 Lifetime Counter</b>		
10.6.1.2#1	NT	A DP OUT Adapter shall start counting as soon as Link Symbol clock is stable for starting link training with DPRX.
10.6.1.2#1	NT	A DP IN Adapter shall start counting as soon as it completed its equalization process.
10.6.1.2#3	NT	In order to filter out the variation introduced by spread-spectrum modulation, the LC shall be filtered using a first order IIR filter.
10.6.1.2#4	NT	The filtering operation shall be done with 8-bit truncation at the fraction part to assure reproducible result.
10.6.1.2#5	NT	All operands of IIR filter shall have the same format of 64 bits of integer followed by 8 bits of fraction.
<b>10.6.1.3 DP Clock Sync Packet</b>		
10.6.1.3#1	NT	A DP Clock Sync Packet shall have the format shown in Figure 10-67.
10.6.1.3#2	NT	The fields forming a DP Clock Sync Packet shall be as defined below: <b>Reserved:</b> This field is reserved and shall be set to 0.
10.6.1.3#3	NT	The fields forming a DP Clock Sync Packet shall be as defined below: <b>Window Count:</b> This field is defined in Section 10.6.2.1. The <i>Window Count</i> field structure is shown in Figure 10-65(A).
10.6.1.3#4	NT	The fields forming a DP Clock Sync Packet shall be as defined below: <b>FLC:</b> This field contains the snapshot of the Filtered Lifetime Counter at the time the Window Measured Event occurred.
10.6.1.3#5	NT	The fields forming a DP Clock Sync Packet shall be as defined below: <b>CRC32:</b> This field contains a CRC32 computed over the entire payload using the following DW order: DW1, DW3, DW2, DW7, DW6, DW5, DW4. The following CRC shall be used: Width: 32; Poly: 1EDC 6F41h; Init: FFFF FFFFh; RefIn: True; RefOut: True; XorOut: FFFF FFFFh.

<b>10.6.2 DP Adapter Requirements</b>		
<b>10.6.2.1 DP IN Adapter Requirements</b>		
10.6.2.1#1	NT	A DP IN Adapter shall: Implement a Lifetime Counter as described in Section 10.6.1.1.2.
10.6.2.1#2	NT	A DP IN Adapter shall: Implement the logic to perform the LC filtering.
10.6.2.1#3	NT	A DP IN Adapter shall: Update FLC upon an Update Counter Event.
10.6.2.1#4	NT	A DP IN Adapter shall: Upon the first Measure Window Event: Capture the current FLC; Store the current captured FLC to be used as previous captured FLC at the next Measure Window Event.
10.6.2.1#5	NT	A DP IN Adapter shall: Upon each subsequent Measure Window Event: Capture the current FLC; Compute the Window Count by calculating the current captured FLC minus the FLC that was captured at the previous Measure Event; Construct a DP Clock Sync Packet and send it over the Main-Link Path within tDPClockSync after the Measure Window Event; Store the current captured FLC to be used as previous captured FLC at the next Measure Window Event.
<b>10.6.2.2 DP OUT Adapter Requirements</b>		
10.6.2.2#1	NT	A DP OUT Adapter shall: Implement a Lifetime Counter as described in Section 10.6.1.2.
10.6.2.2#2	NT	A DP OUT Adapter shall: Implement the logic to perform the LC filtering.
10.6.2.2#3	NT	A DP OUT Adapter shall: Update FLC upon an Update Counter Event.
10.6.2.2#4	NT	A DP OUT Adapter shall: Upon a Measure Window Event: Capture the current FLC; Compute the Window Count as described in Section 10.6.2.1.
10.6.2.2#5	NT	A DP OUT Adapter shall: Upon receiving a DP Clock Sync Packet after the Measure Window Event and before the PLL Adjust Event, compute the PLL frequency adjustment. The method for computing the PLL frequency adjustment is outside the scope of this specification.
10.6.2.2#6	NT	A DP OUT Adapter shall: Upon an Adjust PLL Event, adjust the PLL frequency based on the computation performed at the Measure Window Event.
10.6.2.2#7	NT	If a DP OUT Adapter receives a DP Clock Sync Packet after an Adjust PLL Event but before the next Measure Window Event, it shall not adjust the PLL and shall silently discard the packet.
10.6.2.2#8	NT	If a DP OUT Adapter receives a DP Clock Sync Packet before it computed the first Window Count, it shall not adjust the PLL and shall silently discard the packet.

10.6.2.2#9	NT	When a DP OUT Adapter changes the DisplayPort Main-Link transmitter frequency as a result of adjusting the PLL frequency, it shall adhere to the DisplayPort 1.4a Specification.
10.6.2.2#10	NT	The PLL frequency adjustment shall be completed within tDPPLLAdjust after the Adjust PLL Event.
<b>10.7 DP BW Allocation Mode</b>		
10.7#1		A DP IN Adapter shall support DP BW Allocation Mode.
<b>10.7.1 DP BW Allocation Mode Enablement</b>		
10.7.1#1		Deprecated.
10.7.1#2		A DP IN Adapter shall: Update the AUX Response for DPCD DP TUNNELING and PANEL REPLAY OPTIMIZATION SUPPORT. DP_IN_BW_Allocation_Mode_Support (E000Dh, bit 7) to 1b.
10.7.1#3		A DP IN Adapter shall: Update the AUX Response for DPCD USB4_DRIVER_BW_CAPABILITY.USB4_Driver_BW Allocation Mode Support (E0020h, bit 7) to have the same value as ADP_DP_CS_2.CM BW Allocation Mode Support.
10.7.1#4		When a Connection Manager changes ADP_DP_CS_2.CM BW Allocation Mode Support bit, a DP IN Adapter shall: Set the BW_Allocation_Capability_Changed field to 1b in DP_TUNNELING_STATUS DPCD register.
10.7.1#5		When a Connection Manager changes ADP_DP_CS_2.CM BW Allocation Mode Support bit, a DP IN Adapter shall: Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h)
10.7.1#6		When a Connection Manager changes ADP_DP_CS_2.CM BW Allocation Mode Support bit, a DP IN Adapter shall: If Unmask_BW_Allocation_IRQ is 1b, generate an IRQ_HPD.
10.7.1#7		When DPTX sets DPTX_BW_ALLOCATION_MODE_CONTROL.DP_Display_Driver_BW_Allocation_Mode_Enable (E0030h, bit 7) to 1b, a DP IN Adapter shall: Enable DP BW Allocation Mode.
10.7.1#8		When DPTX sets DPTX_BW_ALLOCATION_MODE_CONTROL.DP_Display_Driver_BW_Allocation_Mode_Enable (E0030h, bit 7) to 1b, a DP IN Adapter shall: Send the Connection Manager a Notification Packet with Event Code = DP_BW as defined in Table 6-12.

10.7.2 Interaction with DPTX		
10.7.2#1		When a DP IN Adapter receives a DPCD AUX Write transaction that targets a DPCD register within Table 10-23, and the targeted DPCD field Type is Read/Write, it shall update the corresponding field in Adapter configuration space with the value of the write transaction.
10.7.2#2		When a DP IN Adapter receives a DPCD AUX Read transaction that targets a DPCD register within Table 10-23, and the targeted DPCD field Type is Read Only, it shall update the read transaction with the value in the corresponding field in Adapter Configuration Space.
10.7.2#3		When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW register, a DP IN Adapter shall: Store the current Allocated BW in an internal variable.
10.7.2#4		When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW register, a DP IN Adapter shall: If the recovery timer is advancing, stop and reset it.
10.7.2#5		When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW register, a DP IN Adapter shall: Initiate a bandwidth request handshake with the Connection Manager as defined in Section 10.7.3.
10.7.2#6		When a Connection Manager writes a value to the Allocated BW field that is equal to or greater than the Requested BW, a DP IN Adapter shall: Set the BW Request Succeeded field to 1b in DP_TUNNELING_STATUS DPCD register.
10.7.2#7		When a Connection Manager writes a value to the Allocated BW field that is equal to or greater than the Requested BW, a DP IN Adapter shall: Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h).
10.7.2#8		When a Connection Manager writes a value to the Allocated BW field that is equal to or greater than the Requested BW, a DP IN Adapter shall: If Unmask_BW_Allocation_IRQ is 1b, generate an IRQ_HPDP.
10.7.2#9		When a Connection Manager writes a value to the Allocated BW field that is equal to or greater than the Requested BW, a DP IN Adapter shall: If the ESTIMATED_BW field was locked for updates due to bandwidth request failure, unlock it.
10.7.2#10		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: Set the ESTIMATED_BW field to the Allocated BW, and lock its value (i.e. ignore any changes in the Estimated_BW field).
10.7.2#11		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: Set the BW Request Failed to 1b in DP_TUNNELING_STATUS DPCD register.

10.7.2#12		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h).
10.7.2#13		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: If Unmask_BW_Allocation_IRQ is 1b, generate an IRQ_HPDP.
10.7.2#14		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: Start the recovery timer.
10.7.2#15		When a Connection Manager writes a value to the Allocated BW field that is smaller than the Requested BW, a DP IN Adapter shall: If the recovery timer has reached tDPBWRecoveryTimeout, the DP IN Adapter initiates a bandwidth allocation request. The DP BW that a DP IN Adapter requests shall be the same bandwidth as before the failed bandwidth allocation (i.e. the same value as in the Allocated BW field before the DPTX last updated the DPCD Requested BW register).
<b>10.7.2.1 Estimated Bandwidth</b>		
10.7.2.1#1		Upon a change in the Estimated BW field, a DP IN adapter shall: Set Estimated BW Changed bit in the DPCD DP_TUNNELING_STATUS register to 1b.
10.7.2.1#2		Upon a change in the Estimated BW field, a DP IN adapter shall: Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_
10.7.2.1#3		Upon a change in the Estimated BW field, a DP IN adapter shall: If Unmask_BW_Allocation_IRQ is 1b, generate an IRQ_HPDP.
<b>10.7.3 Interaction with the Connection Manager</b>		
10.7.3#1		When DPTX sends a DPCD AUX write transaction that targets the REQUESTED_BW field, a DP IN Adapter shall: 1)Set the ADP_DP_CS_8.DPTX Req field to 1b; 2) Send the Connection Manager a Notification Packet with Event Code = DP_BW as defined in Table 6-12; 3)Wait for the Connection Manager to set the ADP_DP_CS_2.CM Ack bit to 1b; 4) Set the ADP_DP_CS_8.DPTX Req field to 0b; 50 Wait for the Connection Manager to set the ADP_DP_CS_2.CM Ack bit to 0b.
<b>10.8 DP Discovery</b>		
<b>10.8.1 DPRX Discovery</b>		
10.8.1#1		A Device Router shall support DPRX Discovery through one of two options: Full Implementation – The Device Router implements a dedicated DP OUT Adapter for each Connector it supports; Partial Implementation – The Device Router implements less DP OUT Adapters than the number of Connectors that it supports.



<b>10.8.1.1 Virtual AUX Tunnel</b>		
<b>10.8.1.2 Full Implementation</b>		
10.8.1.2#1		A Device Router that supports DPRX Discovery through the Full Implementation option shall set the Partial DP Connectivity Implementation bit to 0b.
10.8.1.2#2		The Device Router sends notifications for monitor plug and unplug events as defined in Section 10.3.3.1.
10.8.1.2#3		The Device Router shall contain a DP OUT Adapter for each Downstream facing USB Type-C port on the Device Router and shall contain a DP OUT Adapter for each native DP connector it supports (i.e. the total number of DP OUT Adapters shall be equal to the number of Connectors supported)
<b>10.8.1.3 Partial Implementation</b>		
10.8.1.3#1		The Device Router shall set the Partial DP Connectivity Implementation bit to 1b.
10.8.1.3#2		The Device Router shall implement a DP OUT AUX Adapter, as defined in Section 10.8.1.3.1.
10.8.1.3#3		The Device Router shall support the following Router Operations: Get Connectors Information; Connect DP OUT Adapter.
10.8.1.3#4		The Device Router shall support the following modes, which depend on the value of the SW Mapping bit: HW Mapping Mode (SW Mapping = 0b; Default) – The Device Router autonomously controls the mapping of monitors to DP OUT Adapters.
10.8.1.3#5		The Device Router shall support the following modes, which depend on the value of the SW Mapping bit: SW Mapping Mode (SW Mapping = 1b) – The Device Router maps monitors and DP OUT Adapters according to Connection Manager commands.
<b>10.8.1.3.1 DP OUT AUX Adapter</b>		
10.8.1.3.1#1		A Device Router shall implement full connectivity between the DP OUT AUX Adapter and all Downstream facing USB Type-C connectors and between the DP OUT AUX Adapter and all native DP Connectors.
10.8.1.3.1#2		The DP OUT AUX Adapter shall adhere to all the DP OUT Adapter requirements except the following: It shall not implement the Main-Link Path and the Main-Link DP Physical Layer. It therefore does not reconstruct Main-Link data and does not perform Link Training.
10.8.1.3.1#3		The DP OUT AUX Adapter shall adhere to all the DP OUT Adapter requirements except the following: It shall not implement the <i>Video Enable</i> bit. Therefore, Path Enable and Path Disable events are defined as when the <i>AUX Enable</i> bit is set to 1b and 0b, respectively.

10.8.1.3.1#4		The DP OUT AUX Adapter shall adhere to all the DP OUT Adapter requirements except the following: For AUX Transaction initiation, it shall operate in DPTX Only mode, as described in Section 10.3.1.
<b>10.8.1.3.2 HW Mapping</b>		
<b>10.8.1.3.3 SW Mapping</b>		
10.8.1.3.3#1		When a Device Router is in SW Mapping mode, any change within the Device Router connectivity between a DP OUT Adapter and a Connector shall be done using a Connect DP OUT Adapter Router Operation.
10.8.1.3.3#2		When a Device Router detects a Plug Event, an Unplug Event or an IRQ_HPD (as defined in the DisplayPort 1.4a Specification) on a Connector number N, which is not connected to a DP OUT Adapter or a DP OUT AUX Adapter, it shall send the Connection Manager a Notification Packet with Event Code = DP_CON_CHANGE as defined in Table 6-12 with the following Event Info: Connector Number field equal to N; IRQ_HPD field set to 1b if IRQ_HPD was detected, otherwise set to 0b; Plug/Unplug field set to 1b if Plug was detected, otherwise set to 0b.
<b>10.8.2 DPTX Discovery</b>		
10.8.2#1		A Router that supports DPTX Discovery shall set the DPTX Discovery Support bit to 1b, otherwise it shall set this bit to 0b.
<b>10.8.2.1 DP IN Adapter Requirements</b>		
10.8.2.1#1		A DP IN Adapter shall enter the DPTX Discovery state when the ADP_DP_CS_13.DPTX Discovery Mode bit is set to 1b.
10.8.2.1#2		Upon entering the DPTX Discovery state, a DP IN Adapter shall:1.Set the DPCD DPTX_DISCOVERY_STATUS.Discovery_Mode bit (E002Dh, bit 0) to 1b.
10.8.2.1#3		Upon entering the DPTX Discovery state, a DP IN Adapter shall:2.Drive the HPD signal high.
10.8.2.1#4		Upon entering the DPTX Discovery state, a DP IN Adapter shall:3.Start the DPTX Discovery timer.
10.8.2.1#5		While in DPTX Discovery state: If a DP IN Adapter receives an AUX Request that is listed in Table 10-26, the DP IN Adapter shall reply with an AUX Response. The DP IN Adapter shall not forward the AUX Request to the DP Tunnel.
10.8.2.1#6		While in DPTX Discovery state: If the DPTX performs an AUX Write to a field listed in Table 10 27, the DP IN Adapter shall update the corresponding DP IN field as defined in Table 10 27.

10.8.2.1#7		While in DPTX Discovery state: If the DPTX sets DPCD DPTX_DISCOVERY_CONTROL.Discovery_Done bit (E00033h, bit 7) to 1b, the DP IN Adapter shall set the ADP_DP_CS_9.Discovery Success bit to 1b and shall send the Connection Manager a Notification Packet with Event Code = DPTX_DISCOVERY as defined in Table 6 11.
10.8.2.1#8		While in DPTX Discovery state: If a DP IN Adapter receives an AUX Request that is not listed in Table 10 26 or the DPTX Discovery timer is equal or greater than tDPTXDiscoveryTimeout, a DP IN Adapter shall: 1.Drop the AUX Request; 2.Drive the HPD signal low; 3.Set the ADP_DP_CS_9.Discovery failure bit to 1b; 4.Send the Connection Manager a Notification Packet with Event Code = DPTX_DISCOVERY as defined in Table 6 11; 5.Drop any incoming AUX Requests until it exits the DPTX Discovery state.
10.8.2.1#9		A DP IN Adapter shall exit the DPTX Discovery state when the ADP_DP_CS_13.DPTX Discovery Mode bit is set to 0b.
10.8.2.1#10		If the DP Paths are enabled when the <i>DPTX Discovery Mode</i> bit is set to 0b and the DPTX Discovery ended successfully, a DP IN Adapter shall keep the HPD signal high. Upon the first received HPD with the <i>P Flag</i> bit set to 1b, a DP IN Adapter shall: 1.Set DPCD DPTX_DISCOVERY_STATUS.Discovery_Mode bit (E002Dh, bit 0) to 0b.
10.8.2.1#11		If the DP Paths are enabled when the <i>DPTX Discovery Mode</i> bit is set to 0b and the DPTX Discovery ended successfully, a DP IN Adapter shall keep the HPD signal high. Upon the first received HPD with the <i>P Flag</i> bit set to 1b, a DP IN Adapter shall: 2.Set DPCD DP_TUNNELING_STATUS.Exit_Discovery_Mode bit (E0025h, bit 4) to 1b.
10.8.2.1#12		If the DP Paths are enabled when the <i>DPTX Discovery Mode</i> bit is set to 0b and the DPTX Discovery ended successfully, a DP IN Adapter shall keep the HPD signal high. Upon the first received HPD with the <i>P Flag</i> bit set to 1b, a DP IN Adapter shall: 3.Set DPCD LINK_SERVICE_IRQ_VECTOR_ESI0.DP_TUNNELING_IRQ bit (02005h, bit 5) to 1b.
10.8.2.1#13		If the DP Paths are enabled when the <i>DPTX Discovery Mode</i> bit is set to 0b and the DPTX Discovery ended successfully, a DP IN Adapter shall keep the HPD signal high. Upon the first received HPD with the <i>P Flag</i> bit set to 1b, a DP IN Adapter shall: 4.Generate an IRQ_HPDP.
10.8.2.1#14		If the DP Paths are disabled when the DPTX Discovery Mode bit is set to 0b, a DP IN Adapter shall: 1.Set DPCD DPTX_DISCOVERY_STATUS.Discovery_Mode bit (E002Dh, bit 0) to 0b.
10.8.2.1#15		If the DP Paths are disabled when the DPTX Discovery Mode bit is set to 0b, a DP IN Adapter shall: 2.Drive the HPD signal low.

## 10.9 Timing Parameters

### Chapter 13 Assertions

Assertion #	How to Test	Assertion Description
<b>13 TBT3 Compatibility</b>		
<b>13.8.1.1 DP IN Adapter Requirements</b>		
13.8.1.1#1	TBD	A DP IN Adapter operating in TBT3-Compatible mode follows the requirements listed in Section 10.4.4.2.1 except the following: The Link Status DPCD registers, as defined in Table 10-9, shall be mapped statically as Internal registers.
13.8.1.1#2	TBD	A DP IN Adapter operating in TBT3-Compatible mode follows the requirements listed in Section 10.4.4.2.1 except the following: DPCD address 00600h is mapped as Internal register.
13.8.1.1#3	TBD	A DP IN Adapter operating in TBT3-Compatible mode follows the requirements listed in Section 10.4.4.2.1 except the following: An AUX Read Transaction to the LTTPR DPCD Field, addresses F0000h-F02FFh, are mapped as Internal registers. A DP IN Adapter shall set the data of the AUX Response to 0h.
13.8.1.1#4	TBD	A DP IN Adapter operating in TBT3-compatible mode follows the requirements listed in Section 10.4.4.5 except the following: DSC Support field in the DSC SUPPORT DPCD register shall always be set to 0b.
13.8.1.1#5	TBD	A DP IN Adapter operating in TBT3-compatible mode follows the requirements listed in Section 10.4.4.5 except the following: FEC_CAPABLE field in FEC_CAPABILITY DPCD register shall always be set to 0b.

# Test Setups

## Host with DP IN Adapter

This section describes the test setups for a Host Router that contains a DP IN Adapter.

### AN\_HOST\_DFP1—DPIN\_01

This section describes the test setup for a Host Router that is running DP IN Adapter general testing.

- Vendor provides host system for UUT with a Host Router and a GPU in one of the following configurations:

The Host Router and the GPU are integrated into the same SoC

The Host Router and the GPU are both down on the motherboard

The Host Router is an Add-in Card connected to a KG GPU (or DP Source) through a cable

KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout)

In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 21

USB4 CV should be installed on the Vendor host system

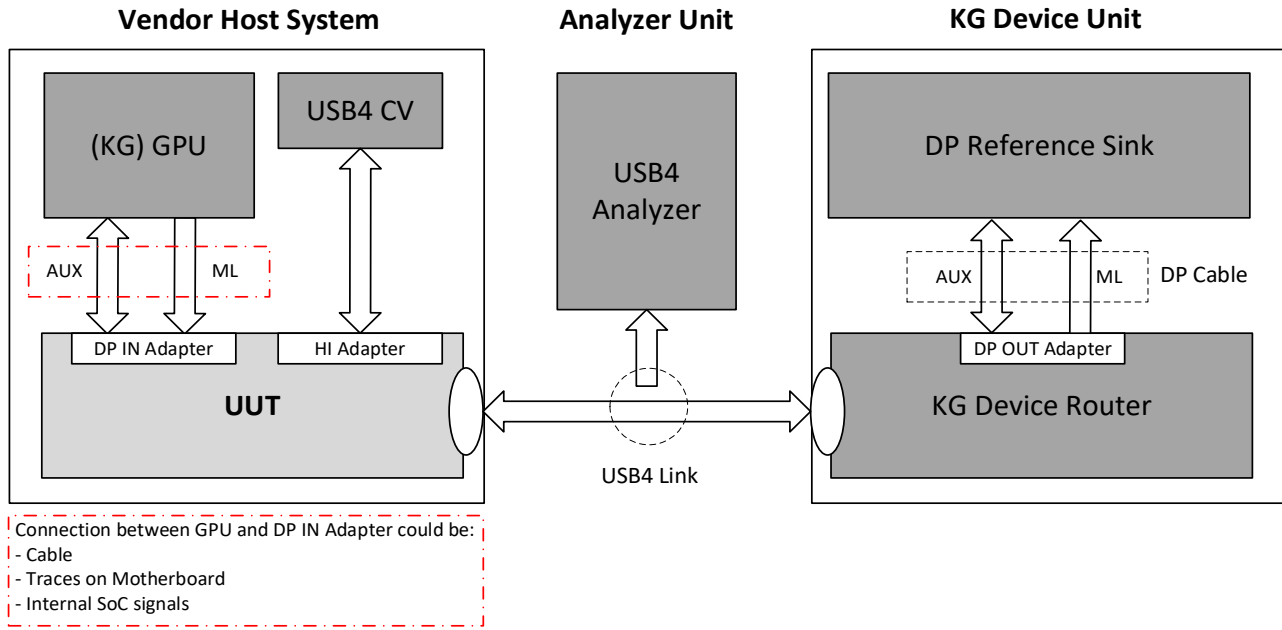
KG Device Unit connects to the UUT and presents as UFP

KG Device Unit contains:

KG Device Router

DP Reference Sink CTS tools

A USB4 Host must support DP Alt mode on its DFPs. The full VESA CTS shall be run on a Host system with a DP Reference Sink in DP Alt Mode.



## AN\_HOST\_DFP1—DPIN\_02

This section describes the test setup for a Host Router running DP IN Adapter specific testing.

Vendor provides host system for UUT with a Host Router and a GPU in one of the following configurations:

The Host Router and the GPU are integrated into the same SoC

The Host Router and the GPU are both down on the motherboard

The Host Router is an Add-in Card connected to a KG GPU (or DP Source) through a cable

KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout)

In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 21

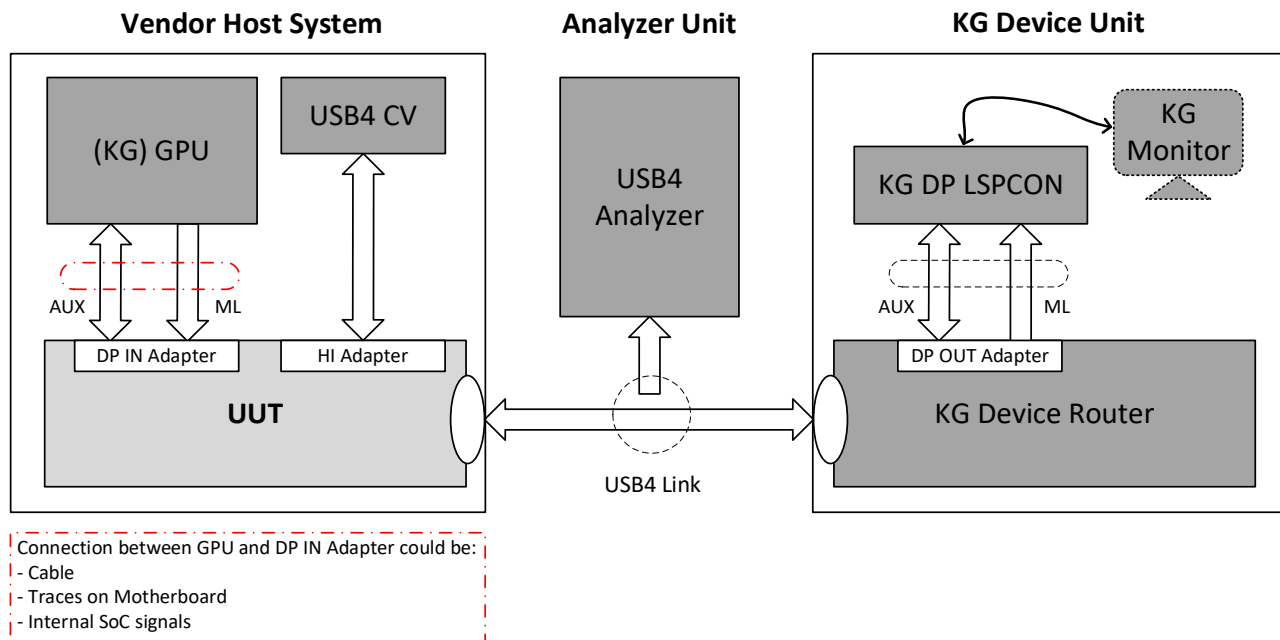
USB4 CV should be installed on the Vendor host system

KG Device Unit connects to the UUT and presents as UFP

KG Device Unit contains:

KG Device Router

KG DP LSPCON dongle and KG monitor



## AN\_HOST\_DFP1—DPIN\_07

This section describes the test setup for a Host Router running DP IN Adapter specific testing.

Vendor provides host system for UUT with a Host Router and a GPU in one of the following configurations:

The Host Router and the GPU are integrated into the same SoC

The Host Router and the GPU are both down on the motherboard

The Host Router is an Add-in Card connected to a KG GPU (or DP Source) through a cable

KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout) and supports DP BW Managment

In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 21

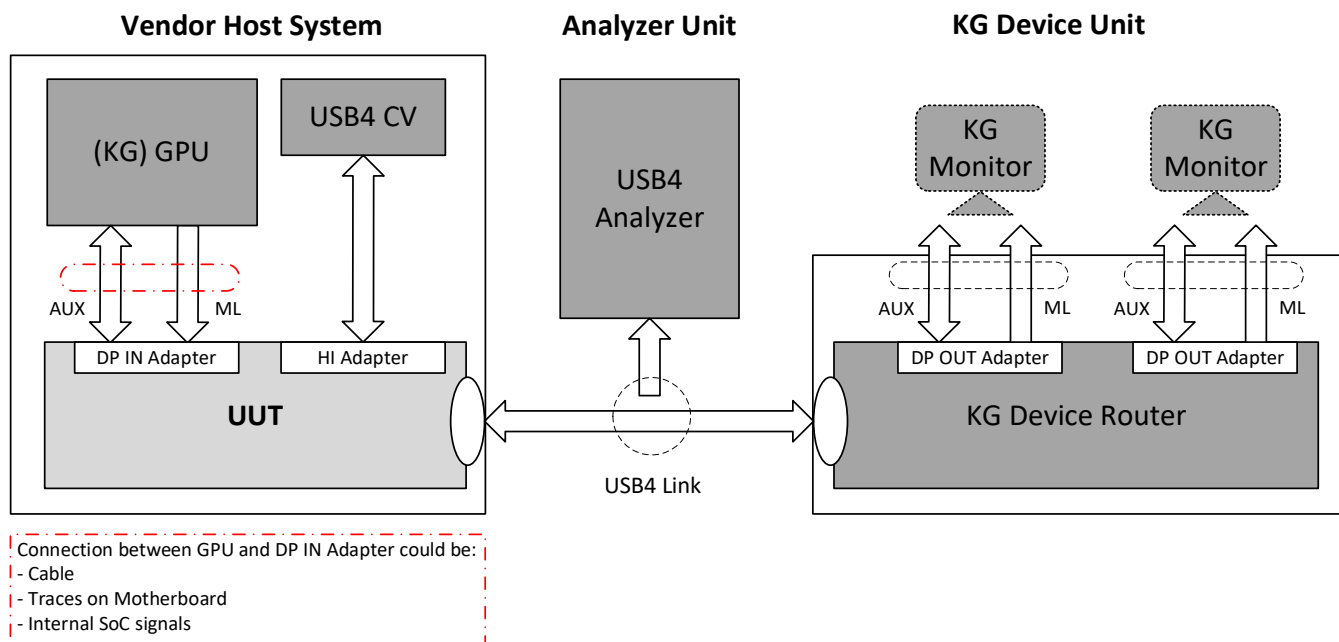
USB4 CV should be installed on the Vendor host system

KG Device Unit connects to the UUT and presents as UFP

KG Device Unit contains:

KG Device Router

2 x KG monitors





## Device with DP IN Adapter

This section describes the test setups for a Device Router that contains a DP IN Adapter and no USB4 DFP.

### AN\_DEV\_UFP1—DPIN\_03

This section describes the test setup for a Device Router running DP IN Adapter general testing.

Vendor provides Device System for UUT with a Device Router and a GPU in one of the following configurations:

The Device Router and the GPU are integrated into the same SoC

The Device Router and the GPU are both down on a motherboard

The Device Router is connected to a KG GPU (or DP Source) through a cable

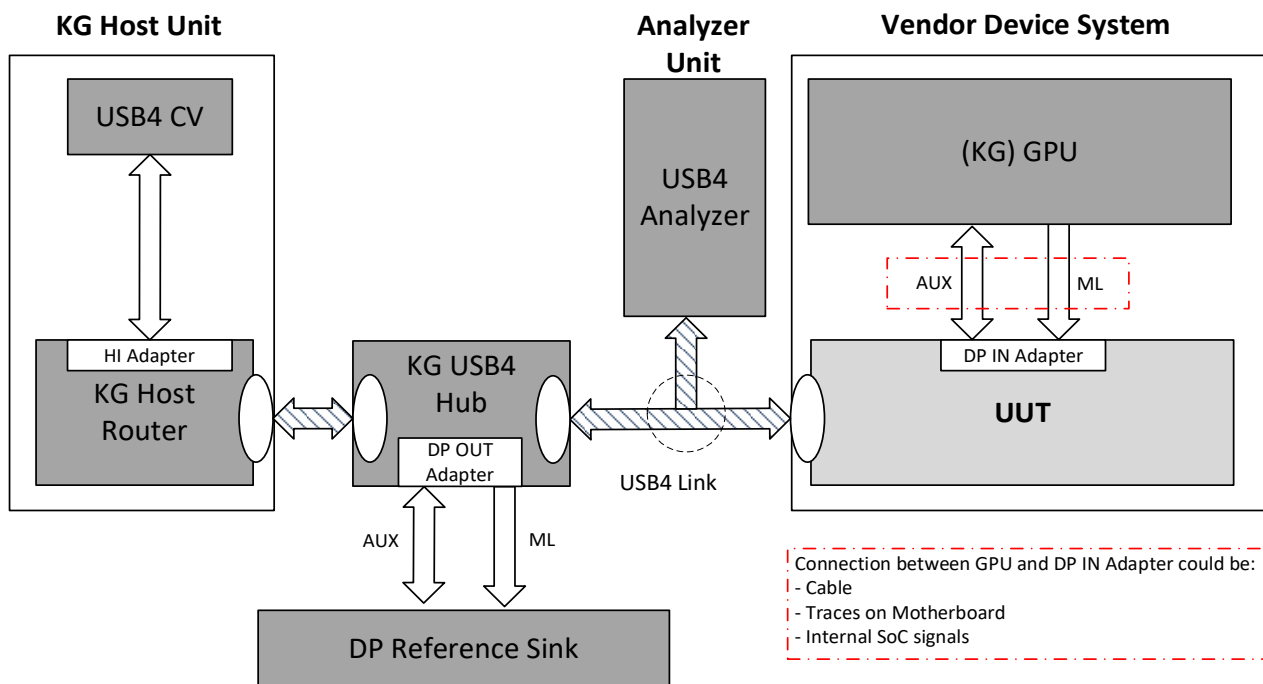
KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout)

In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 21

KG Host Unit with USB4 CV installed

KG USB4 Hub with at least two USB4 DFPs

DP Reference Sink CTS tools



## AN\_DEV\_UFP1—DPIN\_04

This section describes the test setup for a Device Router running DP IN Adapter specific testing.

Vendor provides Device System for UUT with a Device Router and a GPU in one of the following configurations:

The Device Router and the GPU are integrated into the same SoC

The Device Router and the GPU are both down on a motherboard

The Device Router is connected to a KG GPU (or DP Source) through a cable

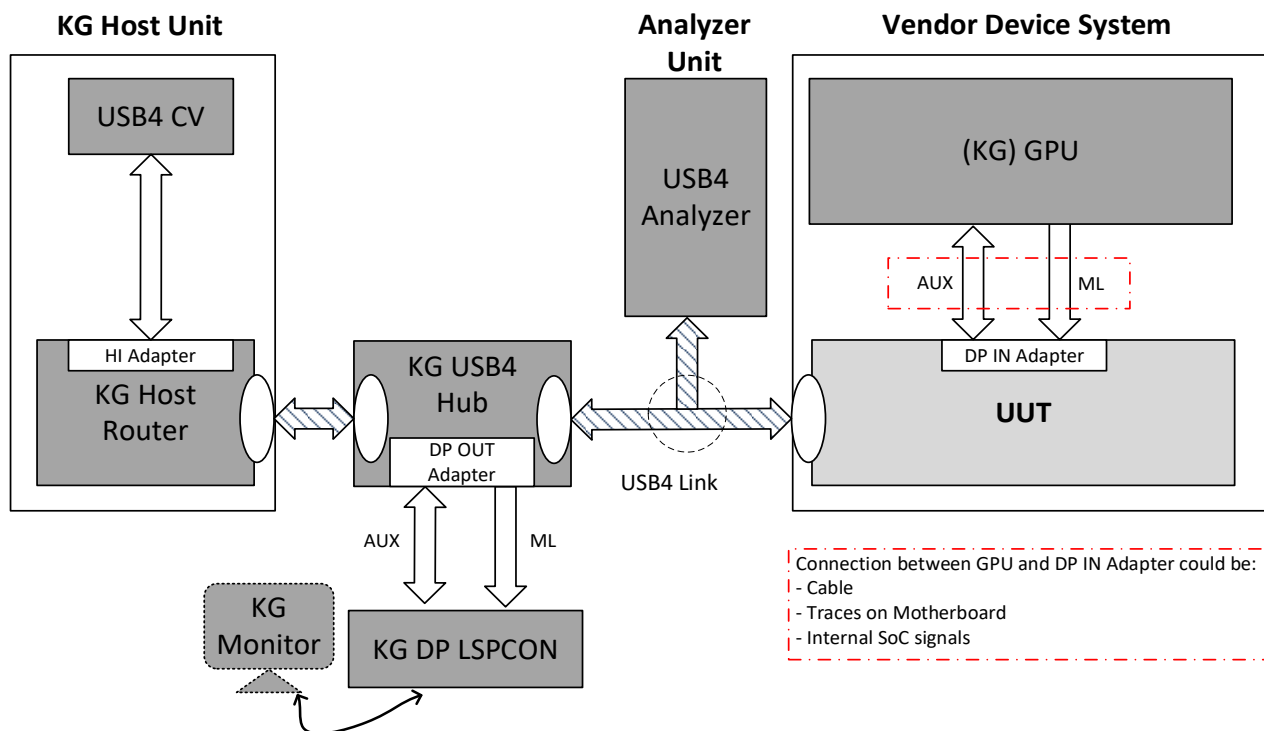
KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout)

In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 21

KG Host Unit with USB4 CV installed

KG USB4 Hub with at least two USB4 DFPs

KG DP LSPCON Dongle and KG monitor



## Hub with DP IN Adapter

This section describes the test setups for a Device Router that contains a DP IN Adapter and one or more USB4 DFP.

### AN\_HUB\_UFP1—DPIN\_05

This section describes the test setup for a Device Router running DP IN Adapter general testing.

Vendor provides Device System for UUT with a Device Router and a GPU in one of the following configurations:

The Device Router and the GPU are integrated into the same SoC

The Device Router and the GPU are both down on a motherboard

The Device Router is connected to a KG GPU (or DP Source) through a cable

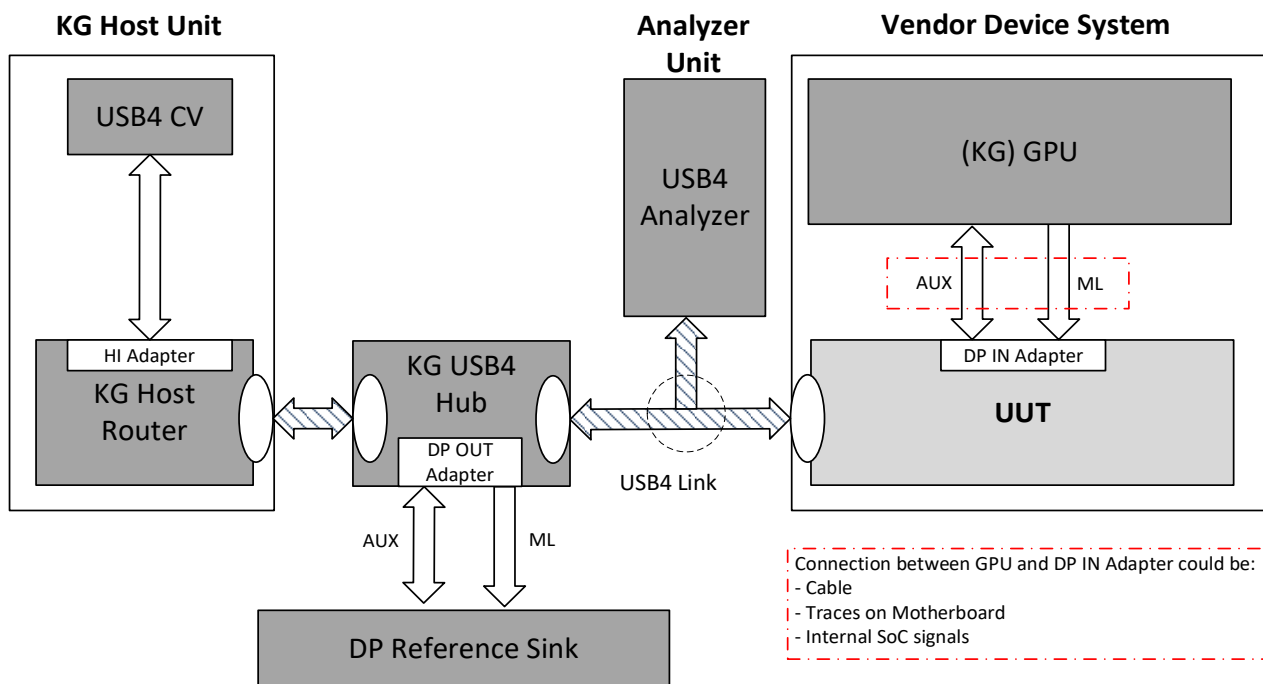
KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout)

In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 21

KG Host Unit with USB4 CV installed

KG USB4 Hub with at least two USB4 DFPs

DP Reference Sink CTS tools



## AN\_HUB\_UFP1—DPIN\_06

This section describes the test setup for a Device Router running DP IN Adapter specific testing.

Vendor provides Device System for UUT with a Device Router and a GPU in one of the following configurations:

The Device Router and the GPU are integrated into the same SoC

The Device Router and the GPU are both down on a motherboard

The Device Router is connected to a KG GPU (or DP Source) through a cable

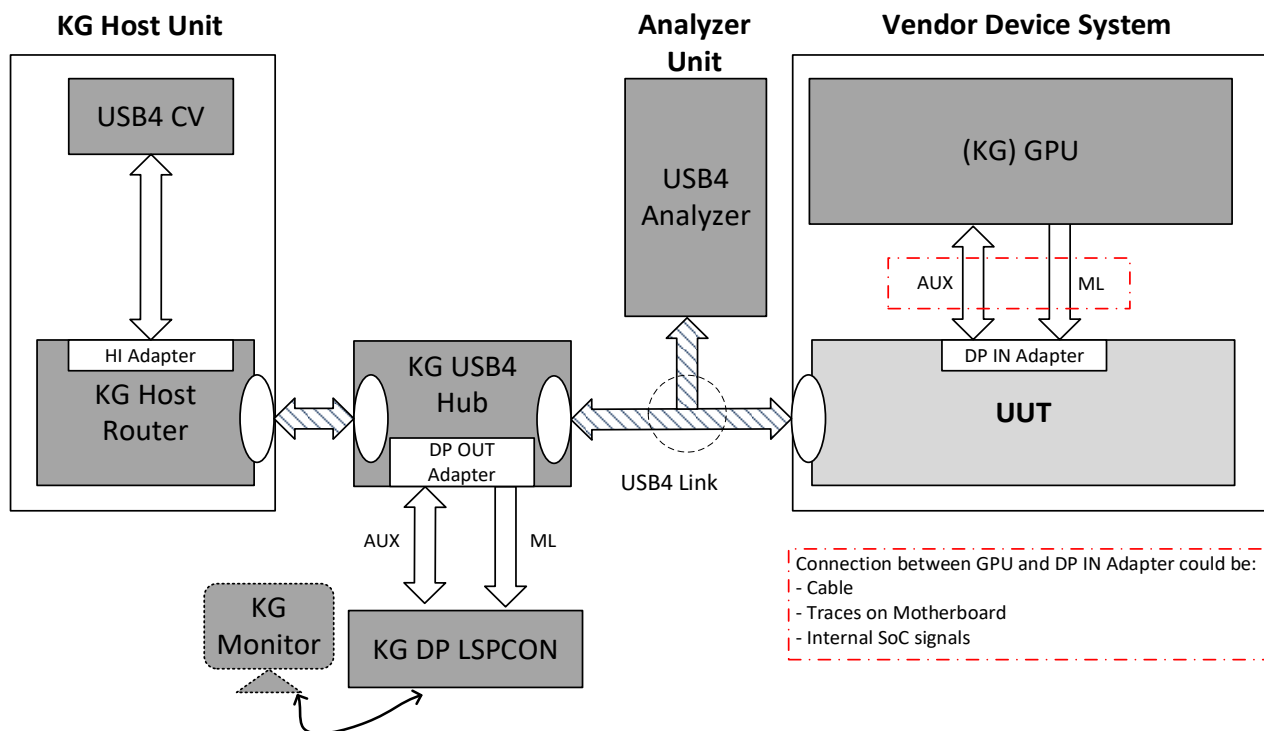
KG GPU (or DP Source) is VESA compliant and is LTTPR Aware (provides the 3.2 ms AUX Timeout)

In such cases where the KG GPU (or DP Source) is connected to the DP IN Adapter by way of a removable cable, the KG GPU(s) (or DP Source) shall meet the capability requirements outlined in Table 21

KG Host Unit with USB4 CV installed

KG USB4 Hub with at least two USB4 DFPs

KG DP LSPCON Dongle and KG monitor



## Host with DP OUT Adapter

This section describes the test setups for a Host Router that contains a DP OUT Adapter. This setup is for a DP OUT Adapter that is integrated with a DPRX.

### AN\_HOST\_DFP1—DPOUT\_01

This section describes the test setup for a Host Router running DP OUT Adapter general testing.

Vendor provides host system for UUT with an integrated DPRX connected to the DP OUT Adapter.

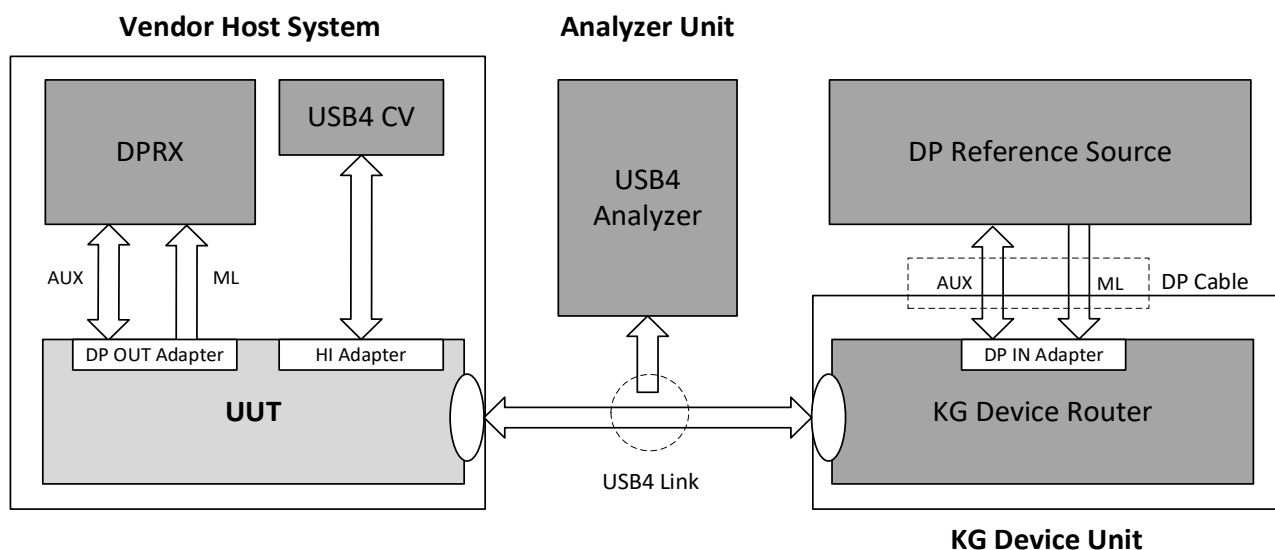
USB4 CV should be installed on the Vendor host system

KG Device Unit connects to UUT and presents as UFP

KG Device Unit contains a KG Device Router with a DP IN Adapter that connects to an exposed connector

DP Reference Source CTS tools

*Note: A KG Device Router with a DP IN Adapter is not available yet. This test setup is not currently used.*



## Device with DP OUT Adapter

This section describes the test setups for a Device Router that contains a DP OUT Adapter and no USB4 DFP.

### AN\_DEV\_UFP1—DPOUT\_02

This section describes the test setup for a Device Router running DP OUT Adapter general testing. This setup is for a DP OUT that connects to an exposed connector.

Vendor provides Device System for UUT with an exposed connector

DP Reference Sink CDT tools

KG Host Unit connects to UUT and presents as DFP

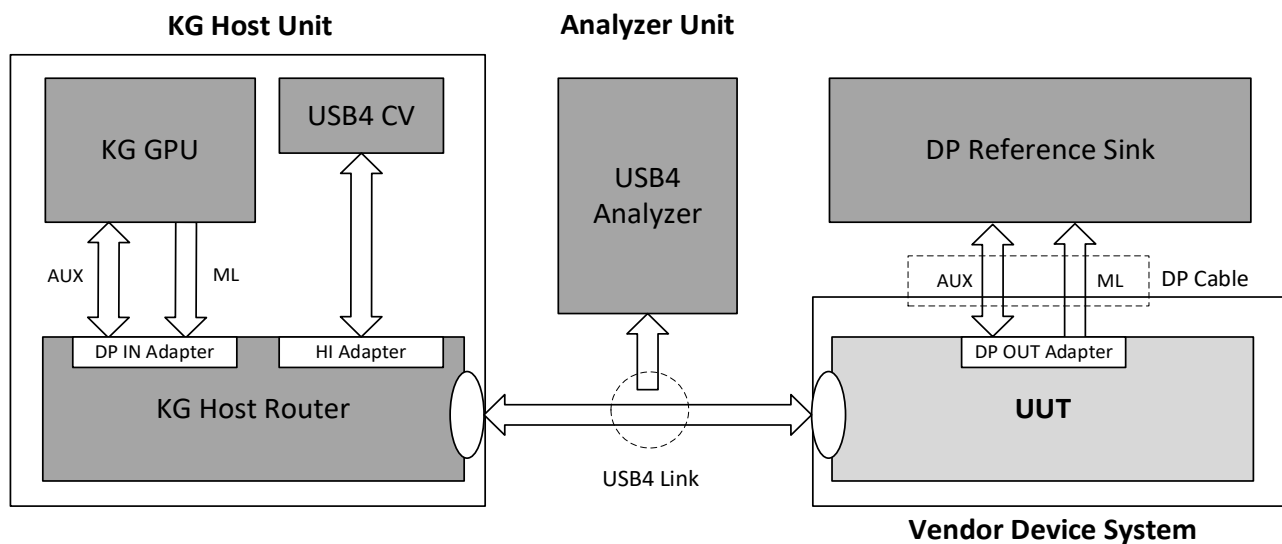
KG Host Unit contains:

KG Host Router

KG GPU

USB4 CV

KG GPU(s) (or DP Source) are VESA compliant and LTTPR Aware (provides the 3.2 ms AUX Timeout) and shall meet the capability requirements outlined in Table 21



## AN\_DEV\_UFP1—DPOUT\_03

This section describes the test setup for a Device Router running DP OUT Adapter specific testing. This setup is for a DP OUT that connects to an exposed connector.

Vendor provides Device System for UUT with an exposed connector

KG DP LSPCON Dongle and KG monitor

KG Host Unit connects to UUT and presents as DFP

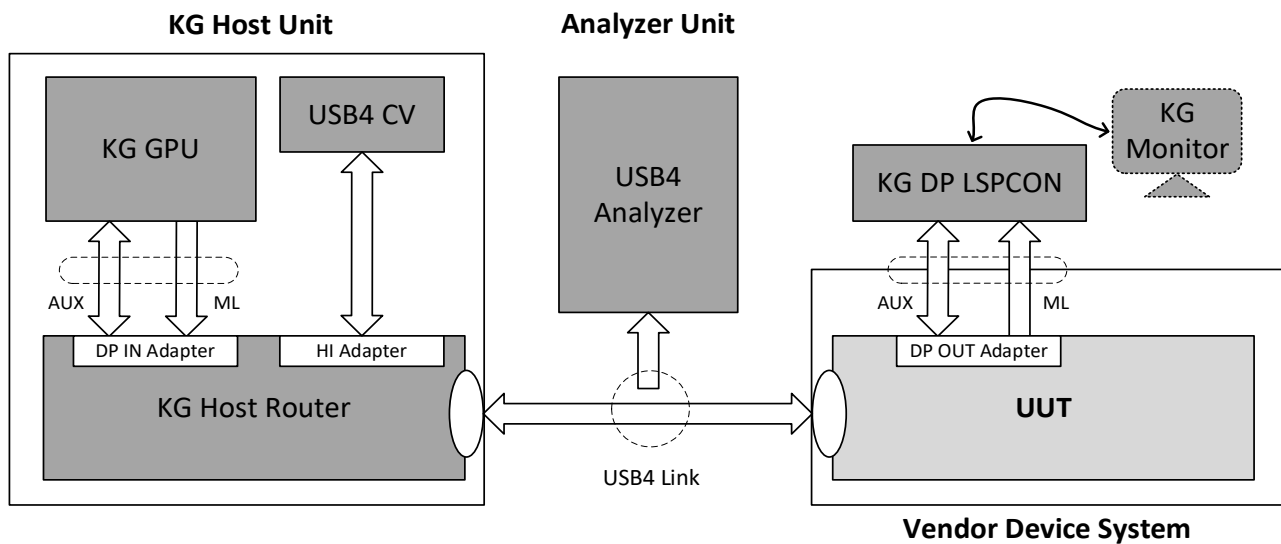
KG Host Unit contains:

KG Host Router

KG GPU

USB4 CV

KG GPU(s) (or DP Source) are VESA compliant and LTTPR Aware (provides the 3.2 ms AUX Timeout) and shall meet the capability requirements outlined in Table 21



## AN\_DEV\_UFP1—DPOUT\_04

This section describes the test setup for a Device Router running DP OUT Adapter general testing. This setup is for a DP OUT Adapter that is integrated with a DPRX.

Vendor provides Device System for UUT with an integrated DPRX

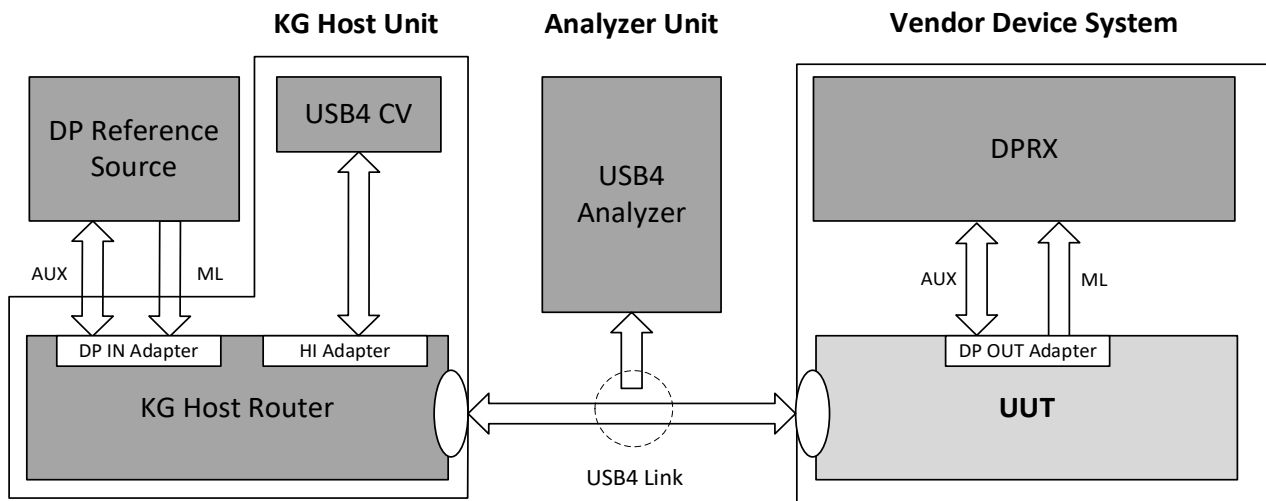
DP Reference Source CTS tools

KG Host Unit connects to UUT and presents as DFP

KG Host Unit contains:

KG Host Router

USB4 CV





## AN\_DEV\_UFP1—DPOUT\_05

This section describes the test setup for a Device Router running DP OUT Adapter general testing. This setup is for a DP OUT that connects to an exposed connector.

Vendor provides Device System for UUT with an exposed connector

KG Monitor

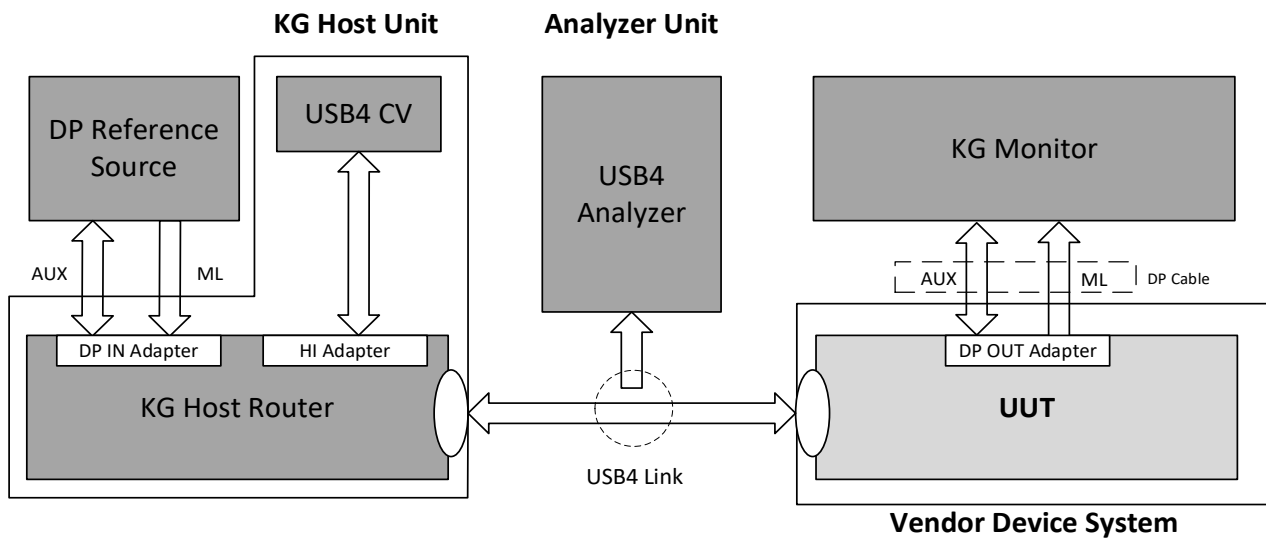
DP Reference Source CTS tools

KG Host Unit connects to UUT and presents as DFP

KG Host Unit contains:

KG Host Router

USB4 CV



## Hub with DP OUT Adapter

This section describes the test setups for a Device Router that contains a DP OUT Adapter and one or more USB4 DFP.

### AN\_HUB\_UFP1—DPOUT\_06

This section describes the test setup for a Device Router running DP OUT Adapter general testing. This setup is for a DP OUT that connects to an exposed connector.

Vendor provides Device System for UUT with an exposed connector

DP Reference Sink CDT tools

KG Host Unit connects to UUT and presents as DFP

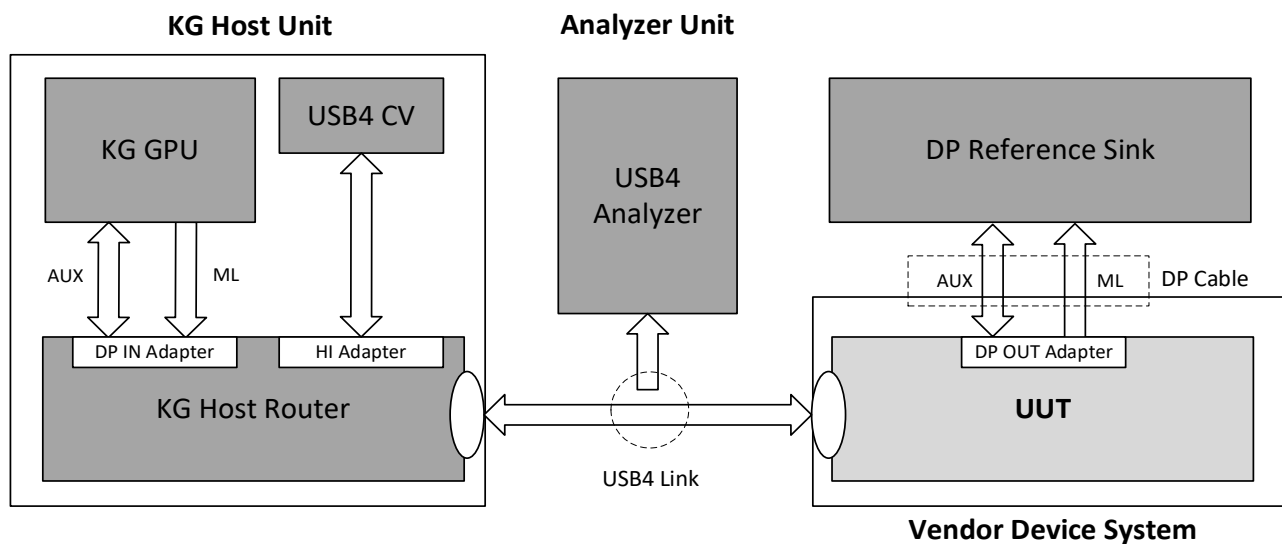
KG Host Unit contains:

KG Host Router

KG GPU

USB4 CV

KG GPU(s) (or DP Source) are VESA compliant and LTTPR Aware (provides the 3.2 ms AUX Timeout) and shall meet the capability requirements outlined in Table 21



## AN\_HUB\_UFP1—DPOUT\_07

This section describes the test setup for a Device Router running DP OUT Adapter specific testing. This setup is for a DP OUT that connects to an exposed connector.

Vendor provides Device System for UUT with an exposed connector

KG DP LSPCON Dongle and KG monitor

KG Host Unit connects to UUT and presents as DFP

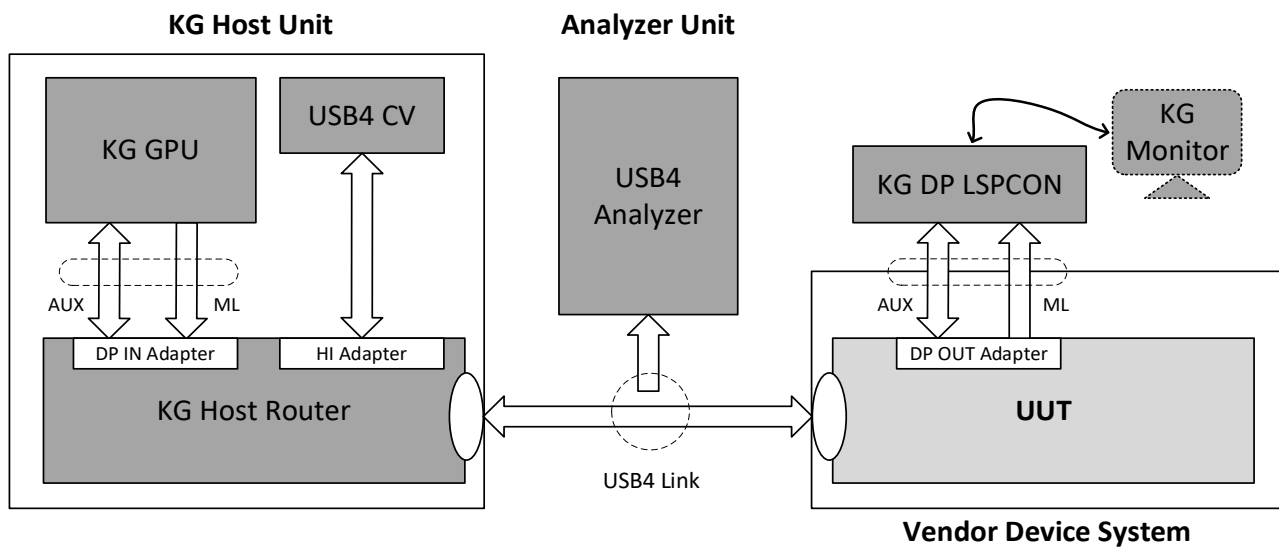
KG Host Unit contains:

KG Host Router

KG GPU

USB4 CV

KG GPU(s) (or DP Source) are VESA compliant and LTTPR Aware (provides the 3.2 ms AUX Timeout) and shall meet the capability requirements outlined in Table 21



## AN\_HUB\_UFP1—DPOUT\_08

This section describes the test setup for a Device Router running DP OUT Adapter general testing. This setup is for a DP OUT Adapter that is integrated with a DPRX.

Vendor provides Device System for UUT with an integrated DPRX

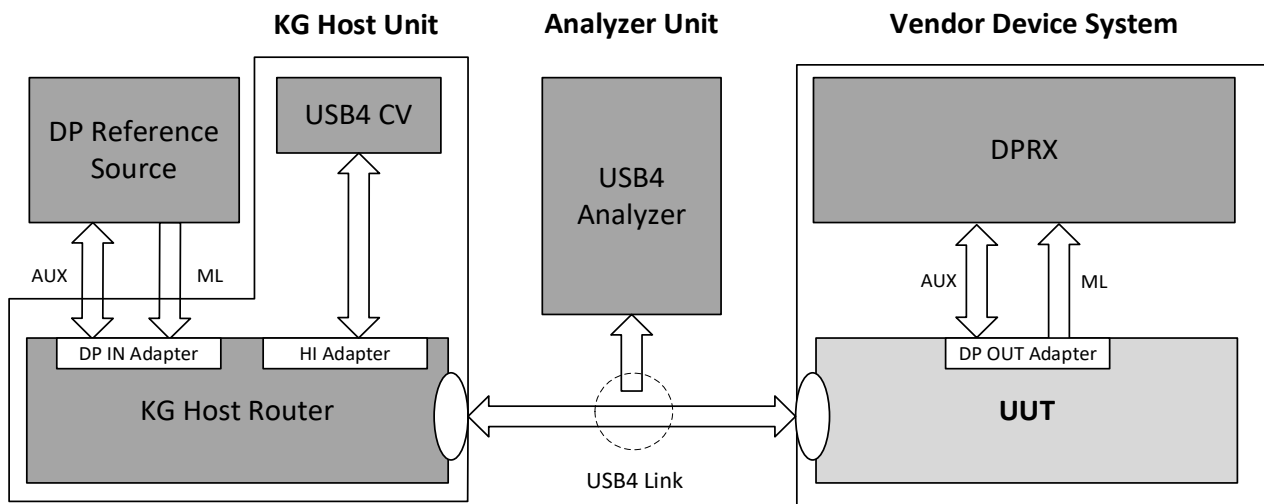
DP Reference Source CTS tools

KG Host Unit connects to UUT and presents as DFP

KG Host Unit contains:

KG Host Router

USB4 CV



## AN\_HUB\_UFP1—DPOUT\_09

This section describes the test setup for a Device Router running DP OUT Adapter general testing. This setup is for a DP OUT that connects to an exposed connector.

Vendor provides Device System for UUT with an exposed connector

KG Monitor

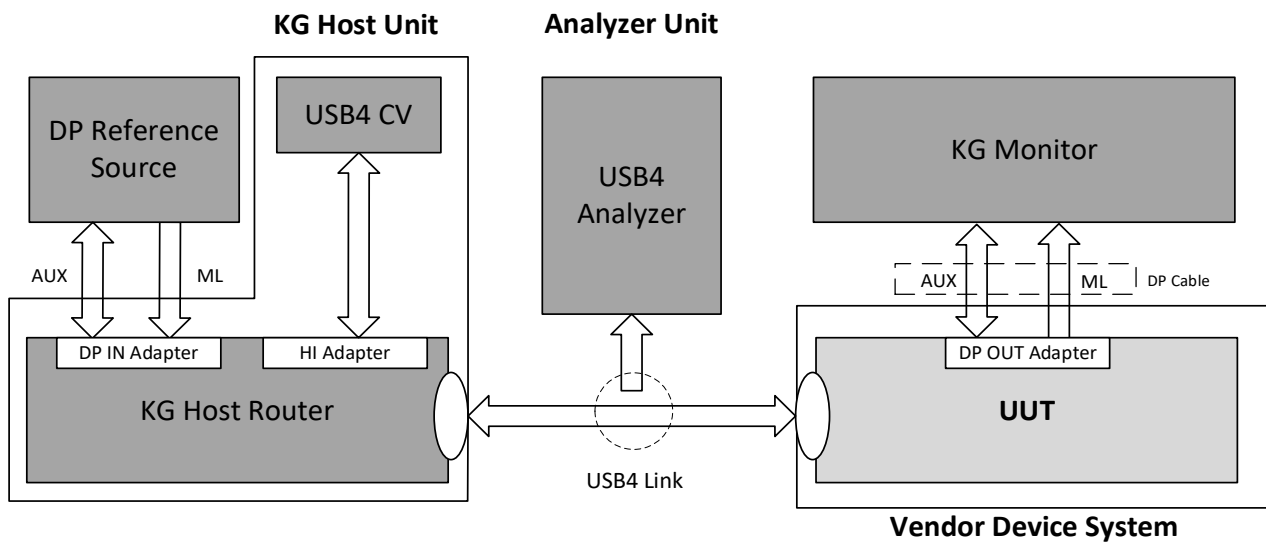
DP Reference Source CTS tools

KG Host Unit connects to UUT and presents as DFP

KG Host Unit contains:

KG Host Router

USB4 CV



## USB4 Naming Convention Changes

- DisplayPort DP Reference Sink – USB4 DP Sink.
- Source DUT functionality is split between DP IN Adapter in UUT and DP OUT Adapter in KG Device Router.
- In DP CTS tests including a Source DUT writes to Exerciser DP Sink DPCD, The writes are performed by the DP OUT Adapter in KG Device Router.

## DP Question List

### DP IN Adapter Capability Question List

Question	Answer
What is the maximum supported lane count?	1 lane 2 lanes 4 lanes
What is the maximum supported link rate (and associated bit rate)?	1.62Gbps/lane (RBR) 2.7Gbps/lane (HBR) 5.4Gbps/lane (HBR2) 8.1Gbps/lane (HBR3)
What is the Maximal DPCD Rev?	DPCD r1.1 DPCD r1.2 DPCD r1.3 DPCD r1.4a
Does Router support MST?	Not supported Supported
Does Router Support FEC?	Not supported Supported
Does Router support SST SDP Split	Not supported Supported
Does Router support LTTPR?	Not supported Supported
Does Router support DSC?	Not supported Supported
Does Router support HDCP	Not supported Supported

## DP OUT Adapter Capability Question List

Question	Answer
What is the maximum supported lane count?	1 lane 2 lanes 4 lanes
What is the maximum supported link rate (and associated bit rate)?	1.62Gbps/lane (RBR) 2.7Gbps/lane (HBR) 5.4Gbps/lane (HBR2) 8.1Gbps/lane (HBR3)
What is the Maximal DPCD Rev?	DPCD r1.1 DPCD r1.2 DPCD r1.3 DPCD r1.4a
Does Router support MST?	Not supported Supported
Does Router Support FEC?	Not supported Supported
Does Router support SST SDP Split	Not supported Supported
Does Router support LTTPR?	Not supported Supported
Does Router support DSC?	Not supported Supported
Does Router support HDCP	Not supported Supported
Does the DP OUT Adapter connect to a USB Type-C connector	Not supported Supported



# Test Descriptions

## DP IN Adapter Tests

### TD 10.001 DP IN Adapter Configuration Capability TD\_DP IN\_1

#### A. Purpose:

- Verify that a DP IN Adapter contains the correct values in the Adapter Configuration Space Basic Attributes and DP Configuration Capability

#### B. Asserts:

- 10.2.1#1
- 10.2.2#1
- 10.3.2.2#1
- 10.4.2.1#5
- 10.4.2.2#1
- 10.4.3.5#1
- 10.4.3.5#2
- 10.4.3.5#3
- 10.4.6.2#4
- 8.2.2.6.1#11

#### C. Setup:

- AN\_HOST\_DFP1—DPIN\_01
- AN\_DEV\_UFP1—DPIN\_03
- AN\_HUB\_UFP1—DPIN\_05

#### D. Procedure:

USB4 CV performs the following steps:

##### Part 1 – Verify Default Values

1. Connect the setup without the DP Reference Sink
2. Read the Adapter Configuration Space of DP IN Adapter on the UUT
3. Verify that the Basic Attributes has the values in the Default Value column in Table 1 (10.2.1#1, 10.2.2#1)
4. Verify that the DP Configuration Capability has the values in the Default Value column in Table 2 (10.2.1#1, 10.2.2#1)
5. For a Ver. 2 Router, Verify that the DP Configuration Capability has the values in the Default Value column in Table 3 (10.2.1#1, 10.2.2#1)
6. Connect the DP Reference Sink to the KG Device Router
7. Configure DP path after getting a Hot Plug Event Packet from the DP OUT Adapter, according to the USB4 Connection Manager Guide.
8. Verify that the DPRX Capabilities Read Done bit is set to 1b within 5 sec (10.4.6.2#4)
9. Read the Adapter Configuration Space of the DP IN on the UUT
10. Verify that the Basic Attributes have the values as the Paired column in Table 1 (10.2.2#1)

11. Verify that the DP Configuration Capability has the values as the Paired column in Table 2 (10.2.2#1, 10.4.2.1#5)
12. For a Ver. 2 Router, verify that the DP Configuration Capability has the values as the Paired column in Table 3 (10.2.2#1)

#### Part 2 – Verify Configuration Bits

13. Wait for the DP link to be stable
14. Start the Analyzer
15. Set the SWLI bit to 1b in the DP IN Adapter in the UUT
16. Read-1: Read Address 0 in Router CS of Compliance Device
17. Wait 2 seconds and set SWLI bit to 0b in the DP IN Adapter in the UUT
18. Stop the Analyzer
19. If there is a DP Link re-training, meaning there are either 8b10\_SET\_LINK or a 128b132b\_SET\_LINK SET\_CONFIG Tunnel Packet with Lane Count field set to a non-zero value in the trace, then verify that there are no Main-Link DP Path Packets coming from the DP IN Adapter between the Read-1 transaction and the DP Link re-training.
20. Else, verify that there are no Main-Link DP Path Packets coming from the DP IN Adapter after the Read-1 until the end of the trace. (8.2.2.6.1#11)
21. Wait for the DP link to be stable
22. Start the Analyzer
23. Write to HPDC in the DP IN Adapter in the UUT
24. Wait 2 seconds
25. Write to HPDS in the DP IN Adapter in the UUT
26. Wait 2 seconds
27. Stop the Analyzer
28. Verify that the DP IN Adapter initiates Link training by sending an 8b10\_SET\_LINK or a 128b132b\_SET\_LINK SET\_CONFIG Tunnel Packet with Lane Count field set to a non zero value (10.4.3.5#1, 10.4.3.5#2, 10.4.3.5#3)

#### Part 3 – Verify Default Values After Path Teardown

29. Disconnect the DP Reference Sink from the KG Device Router
30. After receiving a Hot Unplug Event Packet from the DP OUT Adapter, tear down the DP Path as described in the USB4 Connection Manager Guide
31. Read the Adapter Configuration Space of the DP IN Adapter in the UUT
32. Verify that the Basic Attributes have the default values described in the Default Value column of Table 1 (10.4.2.2#1)
33. Verify that the DP Configuration Capability has the values described in the Default Value column of Table 2 (10.4.2.2#1)
34. For a Ver. 2 Router, verify that the DP Configuration Capability has the values described in the Default Value column of Table 3 (10.4.2.2#1)



**Table 1 – Adapter Configuration Space Basic Attributes**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value		Paired
0	ADP_CS_0	31:0	Vendor Defined	VD	Vendor Defined		Same as Default Value
1	ADP_CS_1	7:0	Next Capability Pointer	RO	Vendor Defined		
		18:8	Max Counter Sets	RO	Vendor Defined		
		19	Counters Configuration Space (CCS) Flag	RO	Vendor Defined		
		20	Bytes Counter Supported	V1: Rsvd V2: RO	V1: 0 V2: Vendor Defined		
		21	Received Bytes Counter Enable	V1: Rsvd V2: RW	0		
		22	Lock Bytes Counter with TimeOffsetFromHR Low Supported	V1: Rsvd V2: RO	V1: 0 V2: Vendor Defined		
		23	Lock Bytes Counter with TimeOffsetFromHR Low Enable	V1: Rsvd V2: RW	0		
		31:24	Reserved	Rsvd	0		
2	ADP_CS_2	7:0	Adapter Type Sub-type	RO	IN 01h	OUT 02h	
		15:8	Adapter Type Version	RO	01h		
		23:16	Adapter Type Protocol	RO	0Eh		
		31:24	Reserved	Rsvd	01h		
3	ADP_CS_3	19:0	Reserved	Rsvd	0		
		25:20	Adapter Number	RO	Vendor Defined		
		28:26	Reserved	Rsvd	0		
		29	HEC Error (HE)	R/Clr	0		

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	Paired
4	ADP_CS_4	30	Flow Control Error (FCE)	R/Clr	0	
		31	Shared Buffering Capable (SBC)	RO	Vendor Defined	
		9:0	Non-Flow Controlled Buffers	R/W	Vendor Defined	
		19:10	Reserved	Rsvd	0	
		29:20	Total Buffers	RO	Vendor Defined	
		30	Plugged	RO	0	
		31	Lock (LCK)	R/W	0	
		10:0	Max Input HopID	RO	Vendor Defined	
		21:11	Max Output HopID	R/W	Vendor Defined	
		28:22	Link Credits Allocated	R/W	0	
5	ADP_CS_5	29	HEC Error Enable (HEE)	R/W	0	
		30	Flow Control Error Enable (FCEE)	R/W	0	
		31	Disable Hot Plug Events (DHP)	R/W	0	
		31:0	HEC Errors	W/Clr	0	
		31:0	Invalid HopID Errors	W/Clr	0	
		31:0	ECC Errors	W/Clr	0	
6	ADP_CS_6	31:0	HEC Errors	W/Clr	0	
7	ADP_CS_7	31:0	Invalid HopID Errors	W/Clr	0	
8	ADP_CS_8	31:0	ECC Errors	W/Clr	0	

**Table 2 – DP IN Adapter Configuration Capability Fields**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	Paired
0	ADP_DP_CS_0	7:0	Next Capability pointer	RO	Vendor Defined	Same as Default Value
		15:8	Capability ID	RO	04h	
		26:16	Video HopID	RO	9	
		29:27	Reserved	Rsvd	0	
		30	AUX Enable (AE)	R/W	0	1
		31	Video Enable (VE)	R/W	0	1

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	Paired
1	ADP_DP_CS_1	10:0	AUX Tx HopID	RO	8	Same as Default Value
		21:11	AUX Rx HopID	RO	8	
		31:22	Reserved	Rsvd	0	
2	ADP_DP_CS_2	2:0	NRD Max Lane Count Similar to remote without BW reeducation by CM	RW	0	The value written by USB4CV during Path Setup
		3	SW Link Init (SWLI)	R/W	0	Same as Default Value
		5:4	Reserved	RsvdZ	0	
		6	HPD Status	RO	0	1
		9:7	NRD Max Link Rate Similar to remote without BW reeducation by CM	RW	0	The value written by USB4CV during Path Setup
		10	CM Ack	R/W	0	
		12:11	Granularity	R/W	0	
		15:13	Group_ID	R/W	0	
		19:16	CM_ID	R/W	0	
		20	CM BW Allocation Mode Support	R/W	0	
		23:21	Reserved	Rsvd	0	0
		31:24	Estimated BW	R/W	0	The value written by USB4CV during Path Setup
3	ADP_DP_CS_3	8:0	Vendor Defined	VD	Vendor Defined	Same as Default Value
		9	HPD Output Clear (HPDC)	R/W	0	
		10	HPD Output Set (HPDS)	R/W	0	
		31:11	Vendor Defined	VD	Vendor Defined	

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	Paired
4	DP_LOCAL_CAP	3:0	Protocol Adapter Version	RO	Version 1: 4 Version 2: 5	
		7:4	Maximal DPCD Rev	RO	3	
		11:8	8b10b Maximal Link Rate	RO	Vendor Defined	
		14:12	Maximal Lane Count	RO	Vendor Defined	
		15	8b10b MST Capability	RO	Vendor Defined	
		16	Panel Replay Tunneling Optimization Support	RO	Version 1: 0 Version 2: Vendor Defined	
		17	128b/132b Link Layer & 10Gbps/Lane Support	RO	Version 1: 0 Version 2: Vendor Defined	
		18	20Gbps/Lane Support	RO	Version 1: 0 Version 2: Vendor Defined	
		19	13.5Gbps/Lane Support	RO	Version 1: 0 Version 2: Vendor Defined	
		20	ALPM Support	RO	Version 1: 0 Version 2: Vendor Defined	
		21	Reserved	Rsvd	0	
		22	8b10b TPS3 Capability	RO	Vendor Defined	
		23	Reserved	Rsvd	1	
		24	8b10b TPS4 Capability	RO	Vendor Defined	

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	Paired
		25	8b10b FEC Not Supported	RO	0b if <i>DSC Not Supported</i> is 0b or <i>Panel Replay Tunneling Optimization Support</i> is 1b, else Vendor Defined	
		26	Secondary Split Capability	RO	Vendor Defined	
		27	LTTPR Not Supported	RO	Version 1: Vendor Defined Version 2: 0	
		28	DP IN BW Allocation Mode Support	RO	Version 1: VD Version 2: 1	
		29	DSC Not Supported	RO	0 if <i>128b/132b Link Layer &amp; 10Gbps/Lane Support</i> is 1b else Vendor Defined	
		31:30	Reserved	Rsvd	0	
5	DP_REMOTE_CAP	3:0	Protocol Adapter Version	R/W	0	The value written by USB4CV during Path Setup
		7:4	Maximal DPCD Rev	R/W	0	
		11:8	8b10b Maximal Link Rate	R/W	0	
		14:12	Maximal Lane Count	R/W	0	
		15	8b10b MST Capability	R/W	0	
		16	Panel Replay Tunneling Optimization Support	R/W	0	
		17	128b/132b Link Layer & 10Gbps/Lane Support	R/W	0	
		18	20Gbps/Lane Support	R/W	0	
		19	13.5Gbps/Lane Support	R/W	0	
		20	ALPM Support	R/W	0	



DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	Paired
		21	Reserved	RsvdZ	0	0
		22	8b10b TPS3 Capability	R/W	0	The value written by USB4CV during Path Setup
		23	Reserved	VD	VD	VD
		24	8b10b TPS4 Capability	R/W	0	The value written by USB4CV during Path Setup
		25	8b10b FEC Not Supported	R/W	0	
		26	Secondary Split Capability	R/W	0	
		27	LTTPR Not Supported	R/W	0	
		28	Reserved	RsvdZ	0	0
		29	DSC Not Supported	RO	0	The value written by USB4CV during Path Setup
		31:30	Reserved	RsvdZ	0	0
6	DP_STATUS	2:0	Lane Count	RO	0	NA
		7:3	Reserved	Rsvd	0	0
		11:8	Link Rate	RO	0	NA
		23:12	Reserved	Rsvd	0	0
		31:24	Allocated BW	R/W	0	The value written by USB4CV during Path Setup

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	Paired
7	DP_COMMON_CAP	3:0	Protocol Adapter Version	RO	0	The lower value of this field between DP IN and DP OUT DP_LOCAL_CAP
		7:4	Maximal DPCD Rev	RO	0	3
		11:8	8b10b Maximal Link Rate	RO	0	The lower value of this field between DP IN and DP OUT DP_LOCAL_CAP
		14:12	Maximal Lane Count	RO	0	
		15	8b10b MST Capability	RO	0	
		16	Panel Replay Tunneling Optimization Support	RO	0	
		17	128b/132b Link Layer & 10Gbps/Lane Support	RO	0	
		18	20Gbps/Lane Support	RO	0	
		19	13.5Gbps/Lane Support	RO	0	
		20	ALPM Support	RO	0	
		21	Reserved	Rsvd	0	0
		22	8b10b TPS3 Capability	RO	0	The AND of this bit between DP IN and DP OUT DP_LOCAL_CAP
		23	Reserved	VD	VD	VD
		24	8b10b TPS4 Capability	RO	0	The AND of this bit between DP IN and DP OUT DP_LOCAL_CAP

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	Paired
		25	8b10b FEC Not Supported	RO	0	The OR of this bit between DP IN and DP OUT DP_LOCAL_C AP
		26	Secondary Split Capability	RO	0	The AND of this bit between DP IN and DP OUT DP_LOCAL_C AP
		27	LTTPR Not Supported	RO	0	The OR of this bit between DP IN and DP OUT DP_LOCAL_C AP
		28	Reserved	Rsvd	0	0
		29	DSC Not Supported	RO	0	The OR of this bit between DP IN and DP OUT DP_LOCAL_C AP
		30	Reserved	Rsvd	0	0
		31	DPRX Capabilities Read Done	RO	0	1 within 5 Sec after Tunnel pair
8	ADP_DP_CS_8	7:0	Requested BW	RO	0	NA – Depends on DPTX
		29:8	Reserved	Rsvd	0	0
		30	DPTX BW Allocation Mode Enable	RO	0	NA – Depends on DPTX
		31	DPTX Req	RO	0	

**Table 3 – DP IN Adapter Added Configuration Capability Fields in Version 2**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	Paired
9	ADP_DP_CS_9	0	Discovery Success (DS)	RO	0	Same as Default Value
		1	Discovery Failure (DF)	RO	0	
		2	Grant Extended Delay (GED)	RO	0	
		31:3	Reserved	Rsvd	0	
10	ADP_DP_CS_10	23:0	DPTX IEEE_OUI	RO	0	NA – Depends on DPTX
		27:24	DPTX Port Number	RO	0	
		30:28	DPTX_Unique_ID	RO	0	
		31	Reserved	Rsvd	0	0
11	ADP_DP_CS_11	31:0	DPTX Device Identification String LSB	RO	0	NA – Depends on DPTX
12	ADP_DP_CS_12	15:0	DPTX Device Identification String MSB	RO	0	NA – Depends on DPTX
		31:16	Reserved	Rsvd	0	0
13	ADP_DP_CS_13	0	DPTX Discovery Mode (DDM)	R/W	0	Same as Default Value
		6:1	CL1 Exit Time	R/W	0	
		31:7	Reserved	Rsvd	0	

## TD 10.002 DP IN Adapter DP CTS LL Test TD\_DP IN\_2

*Note: This test does not require the use of the USB4 CV. It can be run with the USB4 CV or any other software-based Connection Manager.*

### A. Purpose:

- Verify that the DP IN Adapter passes the compliance tests defined in the DP Link CTS

### B. Asserts:

- 10#1
- 10#2
- 10.1.3#1

### C. Setup:

- AN\_HOST\_DFP1—DPIN\_01
- AN\_DEV\_UFP1—DPIN\_03
- AN\_HUB\_UFP1—DPIN\_05

### D. Procedure:

- For AN\_HOST\_DFP1—DPIN\_01 setup
  - The DP Link Layers tests to be executed are the ones marked as ‘Yes’ in the “DP Tunneling Subset” column for Source Testing in Table 8 to Table 13.
- For AN\_DEV\_UFP1—DPIN\_03 or AN\_HUB\_UFP1—DPIN\_05 setup
  - The DP Link Layers tests for Source Testing that are defined in Table 8 to Table 13 are executed. If the only method to utilize the DPTX is through DP Tunneling, then the executed tests are the ones marked as ‘Yes’ in the “DP Tunneling Only” column, otherwise the executed tests are the ones marked as ‘Yes’ in the “DP Tunneling Subset” column.

### Part 1 – Source Device Services Test Procedures

1. Connect test setup
2. Run the tests in Table 8
3. Follow plug/unplug for pair/teardown the tunnel
4. Verify that the UUT passes all of the tests in Table 8 (10#1, 10#2, 10.1.3#1)

### Part 2 – Source Device Link Services Test Procedures

5. Connect test setup
6. Run the tests in Table 9
7. Follow plug/unplug for pair/teardown the tunnel
8. Verify that the UUT passes all of the tests in Table 9 (10#1, 10#2, 10.1.3#1)

### Part 3 –Source Isochronous Transport Services Test Procedures

9. Connect test setup
10. Run the tests in Table 10
11. Follow plug/unplug for pair/teardown the tunnel
12. Verify that the UUT passes all of the tests in Table 10 (10#1, 10#2, 10.1.3#1)

### Part 4 –Source Devices FEC Test Procedures

13. Connect test setup
14. Run the tests in Table 11
15. Follow plug/unplug for pair/teardown the tunnel
16. Verify that the UUT passes all of the tests in Table 11 (10#1, 10#2, 10.1.3#1)

### Part 5 – Source Devices DSC Test Procedures

17. Connect test setup
18. Run the tests in Table 12
19. Follow plug/unplug for pair/teardown the tunnel
20. Verify that the UUT passes all of the tests in Table 12 (10#1, 10#2, 10.1.3#1)
  - a. Run 4.6.1.3 with format 2k@120Hz, Reduced Blanking 2 (rb2)
  - b. Run 4.6.1.3 with format 5k@30Hz, Reduced Blanking 1 (rb1)
  - c. Run 4.6.1.7 with format 2k@30Hz, CTA

### Part 6 – Source Device LTTTPR Test Procedures

1. Connect test setup
2. Run the tests in Table 13
3. Follow plug/unplug for pair/teardown the tunnel
4. Verify that the UUT passes all of the tests in Table 13 (10#1, 10#2, 10.1.3#1)

## TD 10.003 DP IN Adapter LTTPR Test TD\_DP IN\_3

*Note: This test does not require the use of the USB4 CV. It can be run with the USB4 CV or any other software-based Connection Manager.*

*Note: This test is only relevant for a DP IN Adapter that is connected to an exposed connector*

### A. Purpose:

- Verify that the DP IN Adapter passes the compliance tests defined in the DP Link CTS for LTTPR

### B. Asserts:

- 10#1
- 10#2
- 10.1.3#1
- 10.3.1.1#1

### C. Setup:

- AN\_HOST\_DFP1—DPIN\_01
- AN\_DEV\_UFP1—DPIN\_03
- AN\_HUB\_UFP1—DPIN\_05

In the above setups, the Known Good GPU is replaced by a Reference Source. The Reference Source and Reference Sink may reside in the same testing equipment, creating a loopback.

### D. Procedure:

- The DP Link Layers tests to be executed are the ones marked as ‘Yes’ in the “DP IN Adapter” column for LTTPR Device Testing in Table 20

#### Part 1

1. Connect test setup
2. Run the tests in Table 20
3. Follow plug/unplug for pair/teardown the tunnel
4. Verify that the UUT passes all of the tests in Table 20 marked as ‘Yes’ in the “DP IN Adapter” column (10#1, 10#2, 10.1.3#1, 10.3.1.1#1)

## TD 10.004 DP IN Adapter MST Test TD\_DP IN\_4

### A. Purpose:

- Verify DP IN Adapter DP MST functionality (if supported)

B. Asserts:

- 10.4.8#2
- 10.5.2.1#6

C. Setup:

- AN\_HOST\_DFP1—DPIN\_01
- AN\_DEV\_UFP1—DPIN\_03
- AN\_HUB\_UFP1—DPIN\_05

D. Repetitions:

- At each iteration repeat 'Part 1' - Configure the DP Reference Sink as MST with the following parameters:
  - Link: HBR2 x 4 Lanes ; Monitors: Two FHD (1080p)
  - Link: HBR3 x 4 Lanes ; Monitors: Two 4K 8 bpc
  - Link: HBR2 x 2 Lanes ; Monitors: One FHD (1080p)
  - Link: RBR x 4 Lanes ; Monitors: One FHD (1080p)
  - Link: HBR3 x 1 Lane ; Monitors: One FHD (1080p)

E. Procedure:

USB4 CV performs the following steps:

Part 1 – MST Check

1. Configure the DP Reference Sink as MST with the maximal Lane Count and Link Rate according to the iteration parameters.
2. Configure the DP Reference Sink to support the Monitors according to the iteration.
3. Verify that the streams were activated and are stable over the DP Reference Sink (10.5.2.1#6)
4. For the cases of two monitors, Configure the Reference Sink to disconnect one of the monitors and verify that the other stream is stable over the DP Reference Sink. (10.5.2.1#6)

Part 2 – Disable MST

5. Keep Reference Sink configured to the last iteration parameters and monitors
6. Tear down the DP Paths
7. While setting up the DP Path, disable MST function as follows:
  - a. Read DP\_LOCAL\_CAP from DP OUT Adapter and record the values
  - b. Set bit 15 to 0b (disable MST) in the DP\_LOCAL\_CAP values read from the DP OUT Adapter
  - c. Copy the DP\_LOCAL\_CAP values (with bit 15 set to 0b) to the DP\_REMOTE\_CAP register in the DP IN Adapter
8. Start Analyzer
9. Wait 5 seconds
10. Stop Analyzer
11. Verify the Reference Sink responded to AUX Read from DPCD Address 00021h with MST\_CAP set to 1b (Bit[0] of the byte response is set to 1b).



12. Verify that the DP IN Adapter did not send a SET\_STREAM\_MODE SET\_CONFIG Packet with the *MODE* field set to 1b (10.4.8#2)

## TD 10.005 DP IN Sink Count TD\_DP IN\_5

### A. Purpose:

- Verify that the DP IN Adapter correctly follows sink\_count

### B. Asserts:

- 10.4.6.3#1
- 10.4.6.3#2

### C. Setup:

- AN\_HOST\_DFP1—DPIN\_02
- AN\_DEV\_UFP1—DPIN\_04
- AN\_HUB\_UFP1—DPIN\_06

### D. Procedure:

USB4 CV performs the following steps:

#### Part 1 – Teardown Tunnel upon Sink Count Equal 0

1. Connect the test setup with the DP dongle, but without the monitor
2. Enumerate the Routers
3. Verify the reception, within 5 seconds, of a Hot Plug Event Packet with:
  - a. UPG field = 0b
  - b. Topology ID = Routing ID if the Router where the DP OUT Adapter resides
  - c. Adapter Number = DP OUT Adapter where the dongle connects to
4. Start the Analyzer
5. Set up the Paths between the DP IN Adapter and the DP OUT Adapter
6. Verify the reception, within 5 seconds, of a Hot Plug Event Packet with the same parameters as step 3, but with UPG field = 1b
7. Stop the Analyzer
8. Teardown the Path
9. Verify in the trace that after seeing AUX Request to read DPCD address 00200h and AUX Response with data = 0, the DP IN Adapter sends a SET\_SINK\_COUNT SET\_CONFIG Packet with the *SINK\_COUNT* field set to 0b (10.4.6.3#1, 10.4.6.3#2)

#### Part 2 – Pair upon Monitor Connect to DP Dongle

10. Connect the monitor to the DP dongle
11. Verify the reception, within 5 seconds, of a Hot Plug Event Packet with the same parameters as step 3
12. Set up the Paths between the DP IN Adapter and the DP OUT Adapter
13. Verify that the picture on the monitor is stable

### Part 3 – Teardown Tunnel when Sink Count Goes to 0

14. Start the Analyzer
15. Disconnect the monitor from the DP dongle
16. Verify the reception, within 5 seconds, of a Hot Plug Event Packet with the same parameters as step 3, but with UPG field = 1b
17. Stop the Analyzer
18. Teardown the Path
19. Verify in the trace that after seeing AUX Request to read DPCD address 00200h and AUX Response with data = 0, the DP IN Adapter sends a SET\_SINK\_COUNT SET\_CONFIG Packet with the *SINK\_COUNT* field set to 0b (10.4.6.3#1, 10.4.6.3#2)

## TD 10.006 DP IN MFDP TD\_DP IN\_6

### A. Purpose:

- Verify that the DP IN Adapter reduces the number of lanes to 2 with MFDP

### B. Asserts:

- 10.4.5#1
- 10.4.5.1#1

### C. Setup:

- AN\_HOST\_DFP1—DPIN\_02
- AN\_DEV\_UFP1—DPIN\_04
- AN\_HUB\_UFP1—DPIN\_06

*Note: DP LSPCON is a Multi-Function DP Dongle*

### D. Procedure:

USB4 CV performs the following steps:

Part 1 – Reduce Lanes to 2 with MFDP

1. Connect test setup
2. Verify that the DP IN Adapter and DP OUT Adapter are paired and Path is set up between them
3. Verify that the DP IN Adapter sends SET\_CONFIG Packet of type SET\_MFDP with *MFDP Enable* bit set to 0b. (10.4.5.1#1)
4. Verify that the number of lanes is 2 by reading DP\_STATUS.Lane Count (bits 2:0) in both DP Adapters. Value is set to 2h. (10.4.5#1)
5. Verify that the picture on the monitor is stable

## TD 10.007 Tunnel Specific DPCD Register TD\_DP IN\_7

*Note: This test is only relevant for a DP IN Adapter that is connected to an exposed connector*

### A. Purpose:

- Verify that the DP IN Adapter reply to tunnel specific DPCD registers

### B. Asserts:

- 10.4.4.6#1
- 10.4.4.6#2
- 10.7.1#2
- 10.7.1#3

### C. Setup:

- AN\_HOST\_DFP1—DPIN\_01
- AN\_DEV\_UFP1—DPIN\_03
- AN\_HUB\_UFP1—DPIN\_05

In the above setups, the Known Good GPU is replaced by a Reference Source. The Reference Source and Reference Sink may reside in the same testing equipment, creating a loopback.

### D. Procedure:

USB4 CV performs the following steps:

1. Connect test setup
2. Before setting the Paths, write the following fields at the DP IN Adapter
  - a. Set ADP\_DP\_CS\_2. *Granularity* (Bits 12:11) to 2
  - b. Set ADP\_DP\_CS\_2. *Group\_ID* (Bits 15:13) to 7
  - c. Set ADP\_DP\_CS\_2. *CM\_ID* (Bits 19:16) to 0xF
  - d. Set ADP\_DP\_CS\_2. *Estimted\_BW* (Bits 31:24) to 30d
  - e. Set DP\_STATUS. *Allocated\_BW* (Bits 31:24) to 30d
  - f. If DP\_LOCAL\_CAP. *ALPM Support* is set to 1b: Set ADP\_DP\_CS\_13. *CL1 Exit Time* (Bits 6:1) to 0x3E
3. Verify that the picture on the monitor is stable
4. DP Reference Source reads DPCD 0xE0000 to 0xE000F and verifies the followings values: (10.4.4.6#1)
  - a. 0xE0002 – 0xE0000 IEEE\_OUI = non zero
  - b. 0xE0008 – 0xE0003 Device Identification String – non zero
  - c. 0xE0009 – Hardware Revision – non zero
  - d. 0xE000A – Firmware Major Revision – non Zero
  - e. 0xE000B – Firmware Minor Revision – Don't care
  - f. 0xE000D – DP Tunneling and Panel Replay

- i. DP\_Tunneling\_Support (Bit 0) – Set to 1b. (10.4.4.6#2)
    - ii. For Version 2 Routers: Panel\_Replay\_Tunneling\_Optimization\_Support (Bit 6) – Equal to DP IN Adapter DP\_COMMON\_CAP. *Panel Replay Tunneling Optimization Support*
    - iii. For Version 2 Routers: DP\_IN\_BW\_Allocation\_Mode\_Support (Bit7) – Equal to DP\_LOCAL\_CAP. *DP IN BW Allocation Mode Support* (10.7.1#2)
    - iv. All other bits are equal 0b
  - g. 0xE000E – DP\_IN\_ADAPTER\_INFO
    - i. For Version 1 Routers: Equal to 0h
    - ii. For Version 2 Routers: Equal to the DP IN Adapter number the Path was set to
  - h. 0xE000F – USB4\_DRIVER\_ID
    - i. For Version 1 Routers: Equal to 0h
    - ii. For Version 2 Routers: Equal to 0x0F
- 5. For Version 2 Routers: DP Reference Source reads DPCD 0xE001B to 0xE008F and verifies the followings values: (10.4.4.6#1)
  - a. 0xE001B – 0xE001F – USB4\_ROUTER\_TOPOLOGY\_ID – Equal to {Router\_CS\_3.TopologyID High, Router\_CS\_2.TopologyID Low}
    - i. 0xE001B equal to Router\_CS\_2.TopologyID Low[5:0]
    - ii. 0xE001C equal to Router\_CS\_2.TopologyID Low[13:8]
    - iii. 0xE001D equal to Router\_CS\_2.TopologyID Low[21:16]
    - iv. 0xE001E equal to Router\_CS\_2.TopologyID Low[29:24]
    - v. 0xE001F equal to Router\_CS\_3.TopologyID High[5:0]
  - b. 0xE0020 – USB4\_DRIVER\_BW\_CAPABILITY
    - i. USB4\_Driver\_BW\_Allocation\_Mode\_Support (Bit 7) – Equal to ADP\_DP\_CS\_2.CM BW Allocation Mode Support (10.7.1#3)
    - ii. All other bits equal to 0b
  - c. 0xE0021 - DP\_IN\_ADAPTER\_TUNNEL\_INFORMATION
    - i. Group\_ID (Bits 2:0) – Equal to 7h
    - ii. All other bits are equal to 0h
  - d. 0xE0022 - DP\_BW\_GRANULARITY
    - i. Granularity (Bits 1:0) – Equal to 2h
    - ii. All other bits are equal to 0h
  - e. 0xE0023 - ESTIMATED\_BW
    - i. Equal to 30d
  - f. 0xE0024 - ALLOCATED\_BW
    - i. Equal to 30d
  - g. 0xE0027-0xE0026 – Reserved – Equal to 0h
  - h. 0xE0028h - DP\_TUNNELING\_MAX\_LINK\_RATE is equal to ADP\_DP\_CS\_2.NRD Max Link Rate (Bits 9:7) according to the following:

- i. 0h in *NRD\_Max\_Link\_Rate* translates to 06h in DPCD register
  - ii. 1h in *NRD\_Max\_Link\_Rate* translates to 0Ah in DPCD register
  - iii. 2h in *NRD\_Max\_Link\_Rate* translates to 14h in DPCD register
  - iv. 3h in *NRD\_Max\_Link\_Rate* translates to 1Eh in DPCD register
- i. 0xE0029 - DP\_TUNNELING\_MAX\_LANE\_COUNT is equal to ADP\_DP\_CS\_2.NRD Max Lane Count (Bits 2:0) according to the following:
  - i. 0h in *NRD\_Max Lane Count* translates to 01h in DPCD register
  - ii. 1h in *NRD\_Max Lane Count* translates to 02h in DPCD register
  - iii. 2h in *NRD\_Max Lane Count* translates to 04h in DPCD register
- j. 0xE002A - USB4\_CL1Exit\_time
  - i. USB4\_CL1Exit\_time (Bits 5:0) - If DP\_LOCAL\_CAP.ALPM Support is set to 1b then equal to 0x3E else equal to 0h
  - ii. All other bits equal to 0h
- k. 0xE002B - DP\_TUNNELING\_MAIN\_LINK\_CHANNEL\_CODING
  - i. 128b132b\_DP\_SUPPORTED (Bit 0) - Equal to 1b if DPRX set 128b/132b\_SUPPORTED bit to 1b and DP\_COMMON\_CAP.128b/132b Link Layer & 10Gbps/Lane Support is set to 1b, else equal to 0.
  - ii. All other bits equal to 0b
- l. 0xE002C - DP\_TUNNELING\_128b132b\_LINK\_RATE
  - i. 10Gbps per Lane Support (Bit 0) - Equal to 1b if DPRX set 10Gbps/Lane Support bit to 1b and DP\_COMMON\_CAP.128b/132b Link Layer & 10Gbps/Lane Support is set to 1b, else equal to 0.
  - ii. 20Gbps per Lane Support (Bit 1) - Equal to 1b if DPRX set 20Gbps/Lane Support bit to 1b and DP\_COMMON\_CAP.20Gbps/Lane Support is set to 1b, else equal to 0.
  - iii. 13.5Gbps per Lane Support (Bit 2) - Equal to 1b if DPRX set 13.5Gbps/Lane Support bit to 1b and DP\_COMMON\_CAP.13.5Gbps/Lane Support is set to 1b, else equal to 0.
  - iv. All other bits equal to 0b
- m. 0xE002E-0xE002F – Equal to 0h
- n. 0xE0034-0xE008F – Equal to 0h

## TD 10.008 DP IN Adapter with HDCP TD\_DP IN\_8

### A. Purpose:

- Verify that the DP IN Adapter passes DP HDCP CTS tests (if supported)

### B. Asserts:

- 10#1
- 10#2
- 10.1.3#1
- 10.5.6#1
- 10.5.6#2

### C. Setup:

- AN\_HOST\_DFP1—DPIN\_01
- AN\_DEV\_UFP1—DPIN\_03
- AN\_HUB\_UFP1—DPIN\_05

### D. Repetitions:

- Repeat the tests for every link type:
  - 8b/10b SST
  - 8b/10b MST (If Supported)
  - 128b/132b (If Supported)

### E. Procedure:

USB4 CV performs the following steps:

#### Part 1 – USB4 DP CTS HDCP Downstream Procedure with Receiver

1. Connect the setup
2. Run the tests 1A-XX Source Device HDCP Downstream procedure with Receiver define in HDCP CTS for DP reference above
3. Follow plug/unplug for pair/teardown the tunnel
4. Verify that the UUT passes all tests (10#1, 10#2, 10.1.3#1, 10.5.6#1, 10.5.6#2)

#### Part 2 – USB4 DP CTS HDCP Downstream Procedure with Repeater

5. Connect the setup
6. Run the tests 1B-XX Source Device HDCP Downstream Procedure with Repeater define in HDCP CTS for DP reference above
7. Follow plug/unplug for pair/teardown the tunnel
8. Verify that the UUT passes all of the tests (10#1, 10#2, 10.1.3#1, 10.5.6#1, 10.5.6#2)



## TD 10.101 DP IN Adapter Link Bring Up

### A. Purpose:

- Verify Init Adapter flow, Link Training flow & DP Clock Sync Packets prior to SR/LLCP

### B. Asserts:

- TBD

### C. Setup:

- AN\_HOST\_DFP1—DPIN\_01
- AN\_DEV\_UFP1—DPIN\_03
- AN\_HUB\_UFP1—DPIN\_05

### D. Repetitions:

Repeat the tests for the following permutations:

- a. Version 2 Link Partner, 128b/132b (If Supported)
  - No Downstream LTTPRs
  - Two Downstream LTTPRs
- b. Version 2 Link Partner, 8b/10b SST
  - No Downstream LTTPRs
  - Two Downstream LTTPRs
- c. Version 2 Link Partner, 8b/10b MST (If Supported)
  - No Downstream LTTPRs
  - Two Downstream LTTPRs
- d. Version 1 Link Partner, 8b/10b SST
- e. Version 1 Link Partner, 8b/10b MST (If Supported)

### E. Procedure:

USB4 CV performs the following steps:

#### Part 1 – Link Bring up till first High-Speed Tunneled Packet

1. Connect the setup
2. Start Analyzer recording
3. Setup the DP Paths
4. Both Adapters are Version 2 if the UUT is a Version 2 Router, AND
  - a. Link Partner is a Host Router: DP\_REMOTE\_CAP.*Protocol Adapter Version* is equal to 5
  - b. Link Partner is a Device Router: DP\_LOCAL\_CAP.*Protocol Adapter Version* is equal to 5
5. Verify the DP IN responds with an ACK Tunnel Packet after it received the HPD Tunneled Packet
  - a. The ACK Tunnel Packet is sent within 4uSec

- b. The *Type* field in the ACK Tunnel Packet Payload is 8h
- 6. Verify the DP IN Adapter sends a SET\_MFDP SET\_CONFIG Packet with the *MFDP Enable* bit set to 0b
- 7. Verify the DP IN Adapter sends a AUX\_INIT SET\_CONFIG Packet with the *MSG\_Data* field set to 01h
- 8. If both Adapters are Version 2
  - a. Verify that the DP IN Adapter sends a CABLE\_DISCOVERY SET\_CONFIG Packet has the *Cable Type* field set to 0h.
  - b. Verify the DP IN responds with an ACK Tunnel Packet after it received a CABLE\_DISCOVERY SET\_CONFIG Packet
    - i. The ACK Tunnel Packet is sent within 4uSec
    - ii. The *Type* field in the ACK Tunnel Packet Payload is 0h
- 9. Verify that no AUX Tunneled Packets were sent by the DP IN Adapter up to this point
- 10. Verify that the first SET\_LTTTPR\_MODE SET\_CONFIG Packet has the *LTTTPR\_Mode* field set to 0h
- 11. Record the number of Downstream LTTTPRs by the value return from AUX Read of address F0002h.
  - a. A Value of 0h = 0 LTTTPRs, 80h = 1 LTTTPR, 40h = 2 LTTTPRs etc...
- 12. Verify that additional SET\_LTTTPR\_MODE SET\_CONFIG Packets has the right *MSG\_Data*:
  - a. *LTTTPR\_Mode* field equal to 0b if the last AUX Write to address F0003h had 0x55 value (LTTTPR Transparent)
  - b. *LTTTPR\_Mode* field equal to 1b if the last AUX Write to address F0003h had 0xAA value (LTTTPR Non-Transparent)
  - c. For Version 2 format: *Downstream\_LTTTPRs\_Valid* bit is set to 1b
  - d. For Version 2 format: *Downstream\_LTTTPRs* equal to the saved number of Downstream LTTTPRs

#### **For 8b/10b**

- 13. For MST: Verify that the *Mode* bit in the SET\_STREAM\_MODE SET\_CONFIG Packet is set to 1b
- 14. Verify that the *DP Link Training Mode* bit in the 8b10b\_SET\_LINK SET\_CONFIG Packet is set to 0b for LTTTPR Transparent or 1b for LTTTPR Non-Transparent
- 15. If LTTTPR Non-Transparent. Verify all steps occur in order. Note that other SET\_CONFIG and AUX Packets may be present
  - a. Verify the DP IN Adapter sends at least 9 DP Clock Sync Packets
    - i. All of their *Window Count* fields are in between the Minimum and Maximum columns of Table 4
    - ii. The difference between the maximum value and the minimum value of the *Window Count* field is smaller than 2 ppm as defined in Table 4
  - b. Verify the *TS* field in the SET\_TRAINING SET\_CONFIG Packets sequence sent by the DP IN Adapter
    - i. First packet: *TS* = 0xFF
    - ii. Second packet: *TS* = 0x01
    - iii. Third packet: *TS* = 0x02 or 0x03 or 0x04
      - 1. Steps ii follow by step iii appear the number of (*Downstream\_LTTTPRs* + 1)
    - iv. Last packet: *TS* = 0x00
- 16. Else (Transparent). Verify all steps occur in order. Note that other SET\_CONFIG and AUX Packets may be present
  - a. The DP OUT Adapter sends 8b10b\_CR\_STATUS\_DONE SET\_CONFIG Packet with MSG Data Bits [3:0] are not equal to 0h and bit 7 is equal to 0b
  - b. Verify DP IN Adapter sends at least 9 DP Clock Sync Packets
    - i. All of their *Window Count* fields are in between the Minimum and Maximum columns of Table 4
    - ii. The difference between the maximum value and the minimum value of the *Window Count* field is smaller than 2 ppm as defined in Table 4
  - c. The DP OUT Adapter sends 8b10b\_SET\_LINK SET\_CONFIG Packet
    - i. Steps b and c can come in any order.
- 17. Verify the DP IN Adapter sends the first Tunneled Packet type over the Main-Link Path (besides DP Clock Sync Packets) is:
  - i. SST: Blank Start Tunnel Packet with the SR bit in the Blank Start Header set to 1b
  - ii. MST: First Sub-MTP TU values:
    - 1. *Data Count* = 0h
    - 2. *Type* = 1h (SR MTPH)
    - 3. *Slot Number* = 0h

#### **For 128b/132b.** Verify all steps occur in order

- 18. Start Link Training step: Verify the DP IN Adapter sends 128b132b\_SET\_LINK SET\_CONFIG Packet with
  - a. *LINK\_BW\_SET* field set to 01h, 02h or 04h

- b. *LANE\_COUNT\_SET* field set to 01h, 02h or 04h
- 19. The DP OUT Adapter sends 128b132b\_EQ\_DONE SET\_CONFIG Packet with
  - a. *Local EQ\_DONE* bit set to 1b
  - b. *128b/132b\_DPRX\_EQ\_INTERLANE\_ALIGN\_DONE* bit set to 1b
  - c. *128b/132b\_LT\_FAILED* bit set to 0b
- 20. Verify the DP IN Adapter sends 128b132b\_CDS SET\_CONFIG Packet
- 21. Verify DP IN Adapter sends at least one DP Clock Sync Packet. Verify for all DP Clock Sync Packets:
  - a. All of their *Window Count* fields are in between the Minimum and Maximum columns of Table 4
  - b. The difference between the maximum value and the minimum value of the *Window Count* field is smaller than 2 ppm as defined in Table 4
- 22. The DP OUT Adapter sends 128b132b\_CDS\_DONE SET\_CONFIG Packet
- 23. Verify the DP IN Adapter didn't send any AUX Tunneled Packet between Start Link Training step till this point
- 24. Verify the DP IN Adapter sends 128b132b\_SWITCH\_TO\_1BIT\_CDI SET\_CONFIG Packet
- 25. Verify DP IN Adapter sends AUX Tunnel Packet writing 102h address with value 0h
- 26. The DP OUT Adapter sends 128b132b\_SWITCH\_TO\_1BIT\_CDI\_DONE SET\_CONFIG Packet
- 27. Verify the DP IN Adapter sends the first Tunneled Packet type over the Main-Link Path (besides DP Clock Sync Packets) is LLCP Tunneled Packet

## Part 2 – General Checks

- 28. Verify the gap between two SET\_CONFIG Packets sent by the DP IN Adapter is at least 50 uSec
- 29. If both Adapters are Version 2
  - a. Verify all SET\_CONFIG Packets has V2 bit set to 1b (Version 2 format)
- 30. Else, Verify all SET\_CONFIG Packets has V2 bit set to 0b (Version 1 format)
- 31. Verify correct ECC field in all SET\_CONFIG Packets sent by the DP IN Adapter
- 32. Verify correct CRC32 field in all AUX Tunnel Packets sent by the DP IN Adapter

F. Purpose:

- Verify Window Count and Filtered Lifetime Count values

G. Asserts:

- TBD

H. Setup:

- AN\_HOST\_DFP1—DPIN\_01
- AN\_DEV\_UFP1—DPIN\_03
- AN\_HUB\_UFP1—DPIN\_05

I. Repetitions:

Repeat the tests for all the supported Link Rates:

- a. Link Rate RBR
- b. Link Rate HBR
- c. Link Rate HBR2
- d. Link Rate HBR3
- e. Link Rate UHBR 10
- f. Link Rate UHBR 20
- g. Link Rate UHBR 13.5

J. Procedure:

USB4 CV performs the following steps:

1. Connect the setup
2. Start Analyzer recording
3. Setup the DP Paths
4. Verify that the *Window Count* field in all of the DP Clock Sync Packets are in between the Minimum and Maximum columns in Table 4
5. Verify that the difference between the maximum value and the minimum value of the *Window Count* field in all of the DP Clock Sync Packets is smaller than 2 ppm as defined in Table 4
6. Verify that every time the Host Router Time advances in 2mSec (i.e. when bit 21 of the *Nanosecond* field of the Host Router Time changes polarity) a DP Clock Sync Packets is sent within a 100uSec.
7. Verify the following between every two consecutive DP Clock Sync Packets
  - a.  $FLC_N = Window\ Count_N + FLC_{N-1}$

**Table 4 – DP Clock Sync Window Count Range**

	<b>Window Count Range</b>		
<b>Link Rate</b>	<b>Maximum (+300 ppm)</b>	<b>Minimum (-2800ppm)</b>	<b>2 ppm</b>
RBR (1.62 Ghz)	87008487	86720292	174
HBR (2.7 Ghz)	145013975	144533990	290
HBR2 (5.4 Ghz)	145013975	144533990	290
HBR3 (8.1 Ghz)	217520834	216801113	435
UHBR10 (10 Ghz)	167840208	167284751	336
UHBR13.5 (13.5 Ghz)	226584191	225834503	454
UHBR20 (20 Ghz)	335680160	334569758	672

A. Purpose:

- Verify High Speed Encapsulation

B. Asserts:

- TBD

C. Setup:

- AN\_HOST\_DFP1—DPIN\_01
- AN\_DEV\_UFP1—DPIN\_03
- AN\_HUB\_UFP1—DPIN\_05

D. Repetitions:

Repeat the tests for the following permutations:

- a. 128b/132b (If supported): 1,2 & 4 DP Lanes
- b. 8b/10b SST: 1,2 & 4 DP Lanes
- c. 8b/10b MST (If supported): 1,2 & 4 DP Lanes

E. Procedure:

USB4 CV performs the following steps:

1. Connect the setup.
2. Set the DP Reference Sink to operate according to the iteration.
3. Start Analyzer recording:
  - a. Trigger is the first Packet sent over the DP Main Path
  - b. Recording includes only DP Main Path
4. Setup the DP Paths
5. Stop Analyzer recording, 500ms after the trigger.
6. Verify there is a stable video.
7. Start Audio to speakers on the DPRX/Test equipment.
8. Verify sound is stable for 10 seconds.
9. For 8b/10b iterations: Start Analyzer; wait 200ms; Stop Analyzer

**128b/132b**

10. Verify that the first DP Main Path Packet, besides the DP Clock Sync Packets, is an LLCP Packet (PDF = 8h) with the following:
  - a. *Allocated Slots* field equals 0
  - b. *Gap Counter* field equals to 0
11. Verify that for the rest of the LLCP Packets in the trace, *Gap Counter* field equals 65540
12. Verify that there is at least one LLCP Packet with *Allocated Slots* field different than 0
13. Verify that for the first LLCP Packet that had *Allocated Slots* field different than 0, the *ACT* bit is set to 1b.
  - a. Verify that before the above LLCP Packet there were no 128b/132b Control and Data Packet (PDF = 9h) and no 128b/132b Data Packet (PDF = Ah)
14. Verify that every 128b/132b Control and Data Packet and 128b/132b Data Packet in the trace adheres to one of the below rules:

- a. The Payload size is 252 or 248 Bytes.
  - b. The number of time slots described by the Packet is  $2 \times \text{Allocated Slots}$
  - c. The next Packet is an LLCP Packet
15. Verify that every 128b/132b Control and Data Packet and 128b/132b Data Packet in the trace does not describe more than  $2 \times \text{Allocated Slots}$
16. Verify that the sum of all the described time slots by the 128b/132b Control and Data Packets and 128b/132b Data Packets between two LLCP Packets equals to  $1024 \times \text{Allocated Slots}$

### **8b/10b SST**

17. Verify that the first DP Main Path Packet, besides the DP Clock Sync Packets, is a Blank Start Packet (PDF = 2h) with the *SR* bit set to 1b.
18. Verify that all Blank Start Packets payload size is 16.
19. Verify that there is at least one Video Data Packet (PDF = 1) followed by a Blank Start Packet.
20. Verify that the next Packet after a Video Data Packet is either another Video Data Packet or a Blank Start Packet with *Fill Count* field set to 0
21. Verify that there is at least one Main Stream Attribute Packet (PDF = 3).
22. Verify that all Main Stream Attribute Packets payload size is 40.
23. Verify that all Video Data Packets contains 1 to 16 TU Sets.
- a. Verify that all TU Headers are DW aligned within the payload.
24. Verify that the first DW in all Video Data Packets is a TU Header. Verify that the ECC is correct.
25. For the iteration where compression is used, verify that there is at least one FEC\_DECODE Packet (PDF=7).
26. Verify that all FEC\_DECODE Packets adhere to the following rules:
- a. Packet payload size is 20.
  - b. All 3 FEC Commands DWs within a FEC\_DECODE Packet are identical.
  - c. Both Reserved DWs equal to 0
  - d. SR Count in FEC Command DW does not equal to 0.
  - e. One and only one of the two bits, FEN & FDS, are set in the FEC Command DW.
27. For the Audio capture Verify that there are multiple Secondary Data Packets (PDF=4).
- a. Verify that the first DW in all Secondary Data Packets is a Secondary TU Header. Verify that the ECC is correct.
  - b. For 4 DP Lanes iterations verify the *Secondary Count* filed in every Secondary TU Header does not equal to 0 or 63
  - c. Verify that if *NSE* bit is set to 1b, then in the same Secondary TU Header, the *L* bit is also set to 1b
  - d. Verify that if *NSE* bit is set to 1b, then in the following Secondary TU Header the *NSS* bit is set to 1b

### **8b/10b MST**

28. Verify that the first DP Main Path Packet, besides the DP Clock Sync Packets, is an MST Packet (PDF = 6h) with the following:
- a. 1<sup>st</sup> Sub MTP TU: *Slot Number* = 0; *Type* = 01h (SR MTPH)
  - b. 2<sup>nd</sup> Sub MTP TU: *Slot Number* = 1; *Type* = 0Fh (Unallocated)
29. Verify that there is an ACT sequence which consist of the following 8 Sub MTP TUs:
- a. 1<sup>st</sup> Sub MTP TU: *Slot Number* = 0; *Type* = 08h (1 K-Symbol); 1 Byte *Parameter* = 0h
  - b. 2<sup>nd</sup> Sub MTP TU: *Slot Number* = 1; *Type* = 0Fh (Unallocated)
  - c. 1<sup>st</sup> Sub MTP TU: *Slot Number* = 0; *Type* = 08h (1 K-Symbol); 1 Byte *Parameter* = 1h
  - d. 2<sup>nd</sup> Sub MTP TU: *Slot Number* = 1; *Type* = 0Fh (Unallocated)
  - e. 1<sup>st</sup> Sub MTP TU: *Slot Number* = 0; *Type* = 08h (1 K-Symbol); 1 Byte *Parameter* = 1h
  - f. 2<sup>nd</sup> Sub MTP TU: *Slot Number* = 1; *Type* = 0Fh (Unallocated)
  - g. 1<sup>st</sup> Sub MTP TU: *Slot Number* = 0; *Type* = 08h (1 K-Symbol); 1 Byte *Parameter* = 0h
  - h. 2<sup>nd</sup> Sub MTP TU: *Slot Number* = 1; *Type* **\*not equal to\*** 0Fh (Unallocated)
30. Verify that every MST Packet in the trace does not describe more than 1088 time slots
31. Verify that if an MST Packet payload size is smaller than 230 bytes, it describes at least 960 time slots.
32. For the iteration where compression is used, verify that there is at least one FEC\_DECODE Packet (PDF=7).
33. Verify that all FEC\_DECODE Packets adhere to the following rules:
- a. Packet payload size is 20.
  - b. All 3 FEC Commands DWs within a FEC\_DECODE Packet are identical.
  - c. Both Reserved DWs equal to 0
  - d. SR Count in FEC Command DW does not equal to 0.

- e. One and only one of the two bits, FEN & FDS, are set in the FEC Command DW.
- 34.

#### TD 10.104 DP IN Adapter BW Allocation TD\_DP IN\_103

- A. Purpose:
- Verify DP BW Allocation Mode operates correctly
- B. Asserts:
- TBD
- C. Setup:
- AN\_HOST\_DFP1—DPIN\_07
- D. Repetitions: None
- E. Procedure:

USB4 CV performs the following steps:

##### Part 0 – Setup

1. Connect the setup
2. Read LANE\_AD\_P\_CS\_1 from Lane 0 Adapter CS in the Router where DP IN Adapter is located, and calculate the *Available BW for DP* according to Table 5

##### Part 1 – Successful Single stream – Full bandwidth

##### **Setup DP BW and DP Path (Steps 3 to 6)**

3. Setup DP BW Allocation Mode to the DP IN Adapter with the lowest Adapter Number
  - a. Set ADP\_DP\_CS\_2.CM BW Allocation Mode Support to 1b
  - b. Set ADP\_DP\_CS\_2.Group\_ID to 0h
  - c. Set ADP\_DP\_CS\_2.NRD\_Maximal\_Link\_Rate to the DP\_LOCAL\_CAP.Maximal\_Link\_Rate of the DP IN Adapter or DP OUT Adapter (whichever is lower)
  - d. Set ADP\_DP\_CS\_2.NRD\_Maximal\_Lane\_Count to the DP\_LOCAL\_CAP.Maximal\_Lane\_Count of the DP IN Adapter or DP OUT Adapter (whichever is lower)
  - e. Set ADP\_DP\_CS\_2.Estimated BW = Available BW for DP.
  - f. Set ADP\_DP\_CS\_2.Granularity to 2h (1 Gbps)
  - g. Set DP\_STATUS.Allocated BW to 0h
  - h. Set ADP\_DP\_CS\_2.CM Ack to 0b
4. Setup a DP Path between the above DP IN Adapter to the DP OUT Adapter with the lowest Adapter Number
5. Verify that a DP\_BW notification arrives within 10 seconds, and verify the following with in the notification
  - a. The *Route String* contains the Topology ID of the Router that includes the DP IN Adapter
  - b. The *Event Info* field equals to the DP IN Adapter number
6. Read ADP\_DP\_CS\_8 and verify
  - a. DPTX BW Allocation Mode Enable is set to 1b
  - b. DPTX Req is set to 1b
  - c. Requested BW is larger than 0h and not larger than ADP\_DP\_CS\_2.Estimated BW



7. Save the ADP\_DP\_CS\_8. *Requested BW* as the First Original Requested BW
8. Write DP\_STATUS.Allocated BW to the value of ADP\_DP\_CS\_8. *Requested BW*

#### **Finalize Handshake and Verify BW**

9. Write ADP\_DP\_CS\_2.CM Ack to 1b
10. Verify there is a stable image within 5 seconds
11. Read ADP\_DP\_CS\_8 and verify *DPTX Req* is set to 0b
12. Write ADP\_DP\_CS\_2.CM Ack to 0b
13. Start Analyzer
14. Wait 20 mSec
15. Stop Analyzer
16. Verify that the DP Main Path didn't consume more than the Allocated BW
17. Tear down the DP Path

#### Part 2 – Successful Single stream – 75% Requested BW, then, enlarge Estimated

18. Setup DP BW and DP Path (steps are listed in Part 1) with the following change:
  - a. Set ADP\_DP\_CS\_2.Estimated BW = 75% of the First Original Requested BW
19. Write DP\_STATUS.Allocated BW to the value of ADP\_DP\_CS\_8. *Requested BW*
20. Finalize Handshake and Verify BW (Steps are listed in Part 1)
21. Set ADP\_DP\_CS\_2.Estimated BW = Available BW for DP
22. If a DP\_BW notification arrives within 10 seconds continue, otherwise tear down DP Path and end Part 2
23. Read ADP\_DP\_CS\_8 and verify
  - a. *DPTX BW Allocation Mode Enable* is set to 1b
  - b. *DPTX Req* is set to 1b
  - c. *Requested BW* is larger than 0h and not larger than ADP\_DP\_CS\_2.Estimated BW
24. Write DP\_STATUS.Allocated BW to the value of ADP\_DP\_CS\_8. *Requested BW*
25. Finalize Handshake and Verify BW (Steps are listed in Part 1)
26. Tear down the DP Path

#### Part 3 – Failure Single stream

27. Setup DP BW and DP Path (steps are listed in Part 1) with the following changes:
  - a. Use the DP IN Adapter with the **highest** Adapter Number
  - b. Use the DP OUT Adapter with the **highest** Adapter Number
  - c. Set ADP\_DP\_CS\_2.Estimated BW = **2 x** (Available BW for DP).
  - d. Set ADP\_DP\_CS\_2.Granularity to **1h (0.5 Gbps)**
28. Save the (ADP\_DP\_CS\_8. *Requested BW*) / 2 as the Second Original Requested BW
29. Write DP\_STATUS.Allocated BW to the value of **75% of ADP\_DP\_CS\_8. *Requested BW***
30. Write ADP\_DP\_CS\_2.CM Ack to 1b
31. Verify that a DP\_BW notification arrives within 10 seconds, and verify the following with in the notification
  - a. The *Route String* contains the Topology ID of the Router that includes the DP IN Adapter
  - b. The *Event Info* field equals to the DP IN Adapter number
32. Read ADP\_DP\_CS\_8 and verify
  - a. *DPTX BW Allocation Mode Enable* is set to 1b
  - b. *DPTX Req* is set to 1b
  - c. *Requested BW* is larger than 0h and not larger than **DP\_STATUS.Allocated BW**
33. Finalize Handshake and Verify BW (Steps are listed in Part 1)
34. Tear down the DP Path

#### Part 4 –Two streams – Different Groups

35. If Router Under Test has only one DP IN Adapter finish Part 4 and skip Part 5, else continue.
36. The Available BW for DP = First Original Requested BW + 50% of Second Original Requested BW
37. Setup DP BW and DP Path (steps are listed in Part 1) with the following changes:

- a. Set ADP\_DP\_CS\_2.Estimated BW = 4 x (Available BW for DP)
- b. Set ADP\_DP\_CS\_2.Granularity to 0h (0.25 Gbps)
38. Write DP\_STATUS.Allocated BW to the value of ADP\_DP\_CS\_8.Requested BW
39. Finalize Handshake and Verify BW (Steps are listed in Part 1) for first stream
40. Setup DP BW and DP Path (steps are listed in Part 1) with the following changes:
  - a. Use the DP IN Adapter with the **highest** Adapter Number
  - b. Use the DP OUT Adapter with the **highest** Adapter Number
  - c. Set ADP\_DP\_CS\_2.Estimated BW = 4 x (50% of Second Original Requested BW)
  - d. Set ADP\_DP\_CS\_2.Granularity to 0h (0.25 Gbps)
41. Lower the estimated of first stream: Set ADP\_DP\_CS\_2.Estimated BW = 4 x (Available BW for DP – 50% of Second Original Requested BW)
42. Write DP\_STATUS.Allocated BW to the value of ADP\_DP\_CS\_8.Requested BW
43. Finalize Handshake and Verify BW (Steps are listed in Part 1) for second stream
44. Tear down the first DP Path
45. Enlarge the Estimated BW for the remaining DP Path
  - a. Set ADP\_DP\_CS\_2.Estimated BW = 4 x (Available BW for DP)
46. If a DP\_BW notification arrives within 10 seconds continue, otherwise tear down DP Path and end Part 4
47. Read ADP\_DP\_CS\_8 and verify
  - a. DPTX BW Allocation Mode Enable is set to 1b
  - b. DPTX Req is set to 1b
  - c. Requested BW is larger than 0h and not larger than ADP\_DP\_CS\_2.Estimated BW
48. Write DP\_STATUS.Allocated BW to the value of ADP\_DP\_CS\_8.Requested BW
49. Finalize Handshake and Verify BW (Steps are listed in Part 1) for second stream
50. Tear down the DP Path

#### Part 5 –Two streams – Same Group

51. The Available BW for DP = First Original Requested BW + 50% of Second Original Requested BW
52. Setup DP BW and DP Path (steps are listed in Part 1) with the following changes:
  - a. Set ADP\_DP\_CS\_2.Estimated BW = 4 x (Available BW for DP)
  - b. Set ADP\_DP\_CS\_2.Granularity to 0h (0.25 Gbps)
53. Write DP\_STATUS.Allocated BW to the value of ADP\_DP\_CS\_8.Requested BW
54. Finalize Handshake and Verify BW (Steps are listed in Part 1) for first stream
55. Setup DP BW and DP Path (steps are listed in Part 1) with the following changes:
  - a. Use the DP IN Adapter with the **highest** Adapter Number
  - b. Use the DP OUT Adapter with the **highest** Adapter Number
  - c. Set ADP\_DP\_CS\_2.Estimated BW = 4 x (50% of Second Original Requested BW)
  - d. Set ADP\_DP\_CS\_2.Granularity to 0h (0.25 Gbps)
  - e. Set ADP\_DP\_CS\_2.Group\_ID to **1h** for **both** of the DP IN Adapters
56. DPTX may balance the two streams, by first reducing the BW of the first stream, then requesting more BW for the second stream
  - a. In case DPTX lowers the BW for the first stream, enlarge the Estimated BW of the second stream by the amount that was lowered.
57. When all BW Requests handshake are done, Finalize Handshake and Verify BW for both streams.
58. Tear down both of the DP Paths

**Table 5 – Availabe BW for DP Tunneling**

<b>Current Link Speed[19:16]</b>	<b>Negotiated Link Width[25:20]</b>	<b>Available BW for DP</b>
8h (Gen2)	1h (1x Tx)	90% (10Gbps x 1) = 9 Gbps
	2h (2x Tx)	90% (10Gbps x 2) = 18 Gbps
4h (Gen3)	1h (1x Tx)	90% (20Gbps x 1) = 18 Gbps
	2h (2x Tx)	90% (20Gbps x 2) = 36 Gbps
2h (Gen4)	1h or 8h (1x Tx)	90% (40Gbps x 1) = 36 Gbps
	2h (2x Tx)	90% (40Gbps x 2) = 72 Gbps
	4h (3x Tx)	90% (40Gbps x 3) = 108 Gbps

## DP OUT Adapter tests

### TD 10.009 DP OUT Adapter Configuration Capability TD\_DP OUT\_1

#### A. Purpose:

- Verify that a DP OUT Adapter contains the correct values in the Adapter Configuration Space Basic and DP Configuration Capability

#### B. Asserts:

- 10.2.1#1
- 10.2.2#1
- 10.3.2.2#1
- 10.4.2.1#5
- 10.4.2.2#1
- 
- 8.2.2.6.2#9

#### C. Setup:

- AN\_HOST\_DFP1—DPOUT\_01
- AN\_DEV\_UFP1—DPOUT\_02
- AN\_DEV\_UFP1—DPOUT\_04
- AN\_HUB\_UFP1—DPOUT\_06
- AN\_HUB\_UFP1—DPOUT\_08

#### D. Procedure:

USB4 CV performs the following steps:

##### Part 1 – Verify Default Values

1. Connect the test setup. For AN\_DEV\_UFP1—DPOUT\_02 and AN\_HUB\_UFP1-DPOUT\_06 do not connect the DP Reference Sink
2. Read the Adapter Configuration Space of the DP OUT Adapter on the UUT
3. Verify that the Basic Attributes have the values in the Default Value column in Table 6 (10.2.1#1, 10.2.2#2)
4. Verify that the DP Configuration Capability has the values in the Default Value column in Table 7 (10.2.1#1, 10.2.2#2)
5. For AN\_DEV\_UFP1—DPOUT\_02 and AN\_HUB\_UFP1-DPOUT\_06, connect the DP Reference Sink to the DP OUT Adapter in the UUT
6. Configure DP path, after UUT sends a Hot Plug Event Packet for the DP OUT Adapter after detecting the connection, according to Universal Serial Bus 4 (USB4™) Connection Manager Guide section 5.4.
7. It is a test failure if the DPRX capabilities Read Done bit is not 1b within 5 sec.
8. Read the Adapter Configuration Space of the DP OUT Adapter on the UUT
9. Verify that the Basic Attributes has the same values as the Paired column in Table 6 (10.2.2#2)
10. Verify that the DP Configuration Capability has the same values as the Paired column in Table 7 (10.2.2#2, 10.4.2.1#5)

## Part 2 – USB4 Verify Specific Configuration Bits

11. Wait for the DP link to be stable
12. Start the Analyzer
13. Wait 2 seconds and set the SWLI bit to 1b in the DP OUT Adapter in the UUT
14. Stop the Analyzer
15. Verify that Link training was Re-initiated by detecting an 8b10\_SET\_LINK or a 128b132b\_SET\_LINK SET\_CONFIG Tunnel Packet with Lane Count field set to a non zero value. (8.2.2.6.2#9)
16. Wait for the DP link to be stable

## Part 3 – Verify Default Values After Path Teardown

17. For AN\_DEV\_UFP1—DPOUT\_02 and AN\_HUB\_UFP1-DPOUT\_06:
  - a. Disconnect the DP Reference Sink from the KG Device Router
  - b. After receiving a Hot Unplug Event Packet from the DP OUT Adapter continue to the next step
18. Tear down the DP Path as described in Section 5.4 of the Universal Serial Bus 4 (USB4™) Connection Manager Guide
19. Read the Adapter Configuration Space of the DP OUT Adapter in the UUT
20. Verify the that the Basic Attributes have the values described in the Default Value column of Table 6 (10.4.2.2#1)
21. Verify that the DP Configuration Capability has the values described in the Default Value column of Table 7 (10.4.2.2#1)

**Table 6 – Adapter Configuration Space Basic Attributes**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value		Paired
0	ADP_CS_0	31:0	Vendor Defined	VD	Vendor Defined		Same as Default Value
1	ADP_CS_1	7:0	Next Capability Pointer	RO	Vendor Defined		
		18:8	Max Counter Sets	RO	Vendor Defined		
		19	Counters Configuration Space (CCS) Flag	RO	Vendor Defined		
		20	Bytes Counter Supported	V1: Rsvd V2: RO	V1: 0 V2: Vendor Defined		
		21	Received Bytes Counter Enable	V1: Rsvd V2: RW	0		
		22	Lock Bytes Counter with TimeOffsetFromHR Low Supported	V1: Rsvd V2: RO	V1: 0 V2: Vendor Defined		
		23	Lock Bytes Counter with TimeOffsetFromHR Low Enable	V1: Rsvd V2: RW	0		
		31:24	Reserved	Rsvd	0		
2	ADP_CS_2	7:0	Adapter Type Sub-type	RO	IN 01h	OUT 02h	
		15:8	Adapter Type Version	RO	01h		
		23:16	Adapter Type Protocol	RO	0Eh		
		31:24	Reserved	Rsvd	01h		
3	ADP_CS_3	19:0	Reserved	Rsvd	0		
		25:20	Adapter Number	RO	Vendor Defined		
		28:26	Reserved	Rsvd	0		
		29	HEC Error (HE)	R/Clr	0		
		30	Flow Control Error (FCE)	R/Clr	0		

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	Paired
		31	Shared Buffering Capable (SBC)	RO	Vendor Defined	
4	ADP_CS_4	9:0	Non-Flow Controlled Buffers	R/W	Vendor Defined	
		19:10	Reserved	Rsvd	0	
		29:20	Total Buffers	RO	Vendor Defined	
		30	Plugged	RO	0	
		31	Lock (LCK)	R/W	0	1
5	ADP_CS_5	10:0	Max Input HopID	RO	Vendor Defined	Same as Default Value
		21:11	Max Output HopID	R/W	Vendor Defined	
		28:22	Link Credits Allocated	R/W	0	
		29	HEC Error Enable (HEE)	R/W	0	
		30	Flow Control Error Enable (FCEE)	R/W	0	
		31	Disable Hot Plug Events (DHP)	R/W	0	
6	ADP_CS_6	31:0	HEC Errors	W/Clr	0	
7	ADP_CS_7	31:0	Invalid HopID Errors	W/Clr	0	
8	ADP_CS_8	31:0	ECC Errors	W/Clr	0	

**Table 7 – DP OUT Adapter Configuration Capability Fields**

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After paired
0	ADP_DP_CS_0	7:0	Next Capability pointer	RO	Vendor Defined	Same as Default Value
		15:8	Capability ID	RO	04h	
		26:16	Video HopID	RO	9	
		29:27	Reserved	Rsvd	0	
		30	AUX enable (AE)	R/W	0	1

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After paired
		31	Video Enable (VE)	R/W	0	1
1	ADP_DP_CS_1	10:0	AUX Tx HopID	RO	8	Same as Default Value
		21:11	AUX Rx HopID	RO	8	
		31:22	Reserved	Rsvd	0	
2	ADP_DP_CS_2	2:0	Reserved	Rsvd	0	1
		3	SW Link Init (SWLI)	R/W	0	
		5:4	Reserved	RsvdZ	0	
		6	HPD Status	RO	0	Same as Default Value
		7	Reserved	Rsvd	0	
		23:8	Maximum Accumulation Cycles	RO	Vendor Defined	
		31:24	Reserved	Rsvd	0	
3	ADP_DP_CS_3	31:0	Vendor Defined	VD	Vendor Defined	Vendor Defined
4	DP_LOCAL_CAP	3:0	Protocol Adapter Version	RO	Version 1: 4 Version 2: 5	Same as Default Value
		7:4	Maximal DPCD Rev	RO	Vendor Defined	
		11:8	8b10b Maximal Link Rate	RO	Vendor Defined	
		14:12	Maximal Lane Count	RO	Vendor Defined	
		15	8b10b MST Capability	RO	Vendor Defined	
		16	Panel Replay Tunneling Optimization Support	RO	Version 1: 0 Version 2: Vendor Defined	
		17	128b/132b Link Layer & 10Gbps/Lane Support	RO	Version 1: 0 Version 2: Vendor Defined	
		18	20Gbps/Lane Support	RO	Version 1: 0 Version 2: Vendor Defined	



DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After paired
		19	13.5Gbps/Lane Support	RO	Version 1: 0 Version 2: Vendor Defined	
		20	ALPM Support	RO	Version 1: 0 Version 2: Vendor Defined	
		21	Reserved	Rsvd	0	
		22	8b10b TPS3 Capability	RO	Vendor Defined	
		23	Reserved	Rsvd	1	
		24	8b10b TPS4 Capability	RO	Vendor Defined	
		25	8b10b FEC Not Supported	RO	0b if <i>DSC Not Supported</i> is 0b or <i>Panel Replay Tunneling Optimization Support</i> is 1b, else Vendor Defined	
		26	Secondary Split Capability	RO	Version 1: Vendor Defined Version 2: 1	
		27	LTTTPR Not Supported	RO	Version 1: Vendor Defined Version 2: 0	
		28	Reserved	Rsvd	0	
		29	DSC Not Supported	RO	0 if <i>128b/132b Link Layer &amp; 10Gbps/Lane Support</i> is 1b else Vendor Defined	
		31:30	Reserved	Rsvd	0	
5	DP_REMOTE_CAP	3:0	Protocol Adapter Version	R/W	0	The value written by USB4CV during Path Setup
		7:4	Maximal DPCD Rev	R/W	0	
		11:8	8b10b Maximal Link Rate	R/W	0	

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After paired
		14:12	Maximal Lane Count	R/W	0	
		15	8b10b MST Capability	R/W	0	
		16	Panel Replay Tunneling Optimization Support	R/W	0	
		17	128b/132b Link Layer & 10Gbps/Lane Support	R/W	0	
		18	20Gbps/Lane Support	R/W	0	
		19	13.5Gbps/Lane Support	R/W	0	
		20	ALPM Support	R/W	0	
		21	Reserved	RsvdZ	0	0
		22	8b10b TPS3 Capability	R/W	0	The value written by USB4CV during Path Setup
		23	Reserved	VD	VD	VD
		24	8b10b TPS4 Capability	R/W	0	The value written by USB4CV during Path Setup
		25	8b10b FEC Not Supported	R/W	0	
		26	Secondary Split Capability	R/W	0	
		27	LTPR Not Supported	R/W	0	
		28	Reserved	RsvdZ	0	0
		29	DSC Not Supported	RO	0	The value written by USB4CV during Path Setup
		31:30	Reserved	RsvdZ	0	0
6	DP_STATUS	2:0	Lane Count	RO	0	NA (Debug)
		7:3	Reserved	Rsvd	0	0

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After paired
		11:8	Link Rate	RO	0	NA (Debug)
		24:12	Reserved	Rsvd	0	0
		25	CM Handshake (CMHS)	R/W	0	0
		26	DP IN Adapter USB4 Flag (UF)	R/W	0	1
		31:27	Reserved	Rsvd	0	0
7	DP_COMMON_CAP	3:0	Protocol Adapter Version	RO	0	The lower value of this field between DP IN and DP OUT DP_LOCAL_C AP
		7:4	Maximal DPCD Rev	RO	0	3
		11:8	8b10b Maximal Link Rate	RO	0	The lower value of this field between DP IN and DP OUT DP_LOCAL_C AP
		14:12	Maximal Lane Count	RO	0	
		15	8b10b MST Capability	RO	0	
		16	Panel Replay Tunneling Optimization Support	RO	0	
		17	128b/132b Link Layer & 10Gbps/Lane Support	RO	0	
		18	20Gbps/Lane Support	RO	0	
		19	13.5Gbps/Lane Support	RO	0	
		20	ALPM Support	RO	0	
		21	Reserved	Rsvd	0	0
		22	8b10b TPS3 Capability	RO	0	The AND of this bit between DP IN and DP OUT DP_LOCAL_C AP
		23	Reserved	VD	VD	VD

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value	After paired
		24	8b10b TPS4 Capability	RO	0	The AND of this bit between DP IN and DP OUT DP_LOCAL_C AP
		25	8b10b FEC Not Supported	RO	0	The OR of this bit between DP IN and DP OUT DP_LOCAL_C AP
		26	Secondary Split Capability	RO	0	The AND of this bit between DP IN and DP OUT DP_LOCAL_C AP
		27	LTTPr Not Supported	RO	0	The OR of this bit between DP IN and DP OUT DP_LOCAL_C AP
		28	Reserved	Rsvd	0	0
		29	DSC Not Supported	RO	0	The OR of this bit between DP IN and DP OUT DP_LOCAL_C AP
		31:30	Reserved	Rsvd	0	0
8	ADP_DP_CS_8	31:0	Reserved	Rsvd	0	0

## TD 10.010 DP OUT Adapter DP CTS LL Test TD\_DP OUT\_2

*Note: This test does not require the use of the USB4 CV. It can be run with the USB4 CV or any other software-based Connection Manager.*

### A. Purpose:

- Verify that the DP OUT Adapter passes the compliance tests defined in the DP Link CTS

### B. Asserts:

- 10#3
- 10#4
- 10.1.3#1

### C. Setup:

- AN\_HOST\_DFP1—DPOUT\_01
- AN\_DEV\_UFP1—DPOUT\_02
- AN\_DEV\_UFP1—DPOUT\_04
- AN\_DEV\_UFP1—DPOUT\_05
- AN\_HUB\_UFP1—DPOUT\_06
- AN\_HUB\_UFP1—DPOUT\_08
- AN\_HUB\_UFP1—DPOUT\_09

### D. Procedure:

- For a DP OUT Adapter with an exposed connector, both of the below setups shall be executed:
  - AN\_DEV\_UFP1—DPOUT\_02 & AN\_HUB\_UFP1—DPOUT\_06 setup
    - The DP Link Layers tests to be executed are the ones marked as ‘Yes’ in the “DP OUT Adapter UUT” column for Source Testing in Table 8 to Table 13.
  - AN\_DEV\_UFP1—DPOUT\_05 & AN\_HUB\_UFP1—DPOUT\_09 setup
    - The DP Link Layers tests to be executed are the ones marked as ‘Yes’ in the “DP Tunneling only” column for Sink Testing in Table 14 to Table 19.
- For the following setups AN\_DEV\_UFP1—DPOUT\_04 & AN\_HUB\_UFP1—DPOUT\_08 & AN\_HOST\_DFP1—DPOUT\_01, where a DP OUT Adapter is connected directly to an embedded DPRX the below tests shall be executed
  - The DP Link Layers tests for Sink Testing that are defined in Table 14 to Table 19 are executed. If the only method to utilize the DPRX is through DP Tunneling, then the executed tests are the ones marked as ‘Yes’ in the “DP Tunneling Only” column, otherwise the executed tests are the ones marked as ‘Yes’ in the “DP Tunneling Subset” column.

### Part 1 – Source/Sink Device Services Test Procedures

1. Connect test setup
2. Run the tests in Table 8/Table 14
3. Follow plug/unplug for pair/teardown the tunnel
4. Verify that the UUT passes all of the tests in Table 8/Table 14 (10#3, 10#4, 10.1.3#1)

#### Part 2 – Source/Sink Device Link Services Test Procedures

5. Connect test setup
6. Run the tests in Table 9/Table 15
7. Follow plug/unplug for pair/teardown the tunnel
8. Verify that the UUT passes all of the tests in Table 9/Table 15 (10#3, 10#4, 10.1.3#1)

#### Part 3 – Source/Sink Isochronous Transport Services Test Procedures

9. Connect test setup
10. Run the tests in Table 10/Table 16
11. Follow plug/unplug for pair/teardown the tunnel
12. Verify that the UUT passes all of the tests in Table 10/Table 16 (10#3, 10#4, 10.1.3#1)

#### Part 4 – Source/Sink Device FEC Test Procedures

13. Connect test setup
14. Run the tests in Table 11/Table 17
15. Follow plug/unplug for pair/teardown the tunnel
16. Verify that the UUT passes all of the tests in Table 11/Table 17 (10#3, 10#4, 10.1.3#1)

#### Part 5 – Source/Sink Devices DSC Test Procedures

17. Connect test setup
18. Run the tests in Table 12/Table 18
19. Follow plug/unplug for pair/teardown the tunnel
20. Verify that the UUT passes all of the tests in Table 12/Table 18 (10#3, 10#4, 10.1.3#1)

#### Part 6 – Source/Sink Device Embedded LTTTPR Test Procedures

21. Connect test setup
22. Run the tests in Table 13/Table 19
23. Follow plug/unplug for pair/teardown the tunnel
24. Verify that the UUT passes all of the tests in Table 13/Table 19 (10#3, 10#4, 10.1.3#1)

## TD 10.011 DP OUT Adapter LTTTPR test TD\_DP OUT\_3

*Note: This test does not require the use of the USB4 CV. It can be run with the USB4 CV or any other software-based Connection Manager.*

*Note: This test is only relevant for a DP OUT Adapter that is connected to an exposed connector*

### A. Purpose:

- Verify that the DP OUT Adapter passes the compliance tests defined in the DP Link CTS for LTTTPR

### B. Asserts:

- 10#3
- 10#4
- 10.1.3#1
- 10.3.1.1#2

### C. Setup:

- AN\_DEV\_UFP1—DPOUT\_02
- AN\_HUB\_UFP1—DPOUT\_06

In the above setups, the Known Good GPU is replaced by a Reference Source. The Reference Source and Reference Sink may reside in the same testing equipment, creating a loopback.

### D. Procedure:

- The DP Link Layers tests to be executed are the ones marked as ‘Yes’ in the “DP OUT Adapter” column for LTTTPR Device Testing in Table 20

#### Part 1

25. Connect test setup
26. Run the tests in Table 20
27. Follow plug/unplug for pair/teardown the tunnel
28. Verify that the UUT passes all of the tests in Table 20 marked as ‘Yes’ in the “DP OUT Adapter” column (10#3, 10#4, 10.1.3#1, 10.3.1.1#2)

## TD 10.012 DP OUT Adapter MST Test TD\_DP OUT\_4

### A. Purpose:

- Verify DP OUT Adapter DP MST functionality (if supported)

B. Asserts:

- 10.5.2.4#5

C. Setup:

- AN\_DEV\_UFP1—DPOUT\_02
- AN\_HUB\_UFP1—DPOUT\_06

D. Repetitions:

- At each iteration Configure the DP Reference Sink as MST with the following parameters:
  - Link: HBR2 x 4 Lanes ; Monitors: Two FHD (1080p)
  - Link: HBR3 x 4 Lanes ; Monitors: Two 4K 8 bpc
  - Link: HBR2 x 2 Lanes ; Monitors: One FHD (1080p)
  - Link: RBR x 4 Lanes ; Monitors: One FHD (1080p)
  - Link: HBR3 x 1 Lane ; Monitors: One FHD (1080p)

E. Procedure:

USB4 CV performs the following steps:

1. Configure the DP Reference Sink as MST with the maximal Lane Count and Link Rate according to the iteration parameters
2. Configure the DP Reference Sink to support the Monitors according to the iteration.
3. Verify that the streams were activated and are stable over the DP Reference Sink (10.5.2.4#5)
4. For the cases of two monitors, configure the Reference Sink to disconnect one of the monitors and verify that the other stream is stable over the DP Reference Sink. (10.5.2.4#5)



## TD 10.013 DP OUT Sink count TD\_DP OUT\_5

### A. Purpose:

- Verify that the DP OUT Adapter correctly follows sink\_count

### B. Asserts:

- 10.4.6.3#3
- 10.4.6.3#4
- 10.4.6.3#5
- 10.4.6.3#6

### C. Setup:

- AN\_DEV\_UFP1—DPOUT\_03
- AN\_HUB\_UFP1—DPOUT\_07

### D. Procedure:

USB4 CV performs the following steps:

#### Part 1 – Teardown Tunnel upon Sink Count Equal 0

1. Connect the setup with the DP dongle, but without the monitor
2. Enumerate the Routers
3. Verify the reception, within 5 seconds, of a Hot Plug Event Packet with: (10.4.6.3#5, 10.4.6.3#6)
  - a. UPG field = 0b
  - b. Topology ID = Routing ID if the Router where the DP OUT Adapter resides
  - c. Adapter Number = DP OUT Adapter where the dongle connects to
4. Start the Analyzer
5. Set up the Paths between the DP IN Adapter and the DP OUT Adapter
6. Verify the reception, within 5 seconds, of a Hot Plug Event Packet with the same parameters as step 3, but with UPG field = 1b (10.4.6.3#3, 10.4.6.3#4)
7. Stop the Analyzer
8. Teardown the Path
9. Verify in the trace that after seeing AUX Request to read DPCD address 00200h and AUX Response with data = 0, the DP IN Adapter sends a SET\_SINK\_COUNT SET\_CONFIG Packet with the *SINK\_COUNT* field set to 0b

#### Part 2 – Pair upon Monitor Connect to Dongle

10. Connect the monitor to the DP dongle
11. Verify the reception, within 5 seconds, of a Hot Plug Event Packet with the same parameters as step 3 (10.4.6.3#5, 10.4.6.3#6)
12. Set up the Paths between the DP IN Adapter and the DP OUT Adapter

13. Verify that the picture on the monitor is stable

#### Part 3 – Teardown Tunnel when Sink Count Goes to 0

1. Start the Analyzer
2. Disconnect the monitor from the DP dongle
3. Verify the reception, within 5 seconds, of a Hot Plug Event Packet with the same parameters as step 3, but with UPG field = 1b (10.4.6.3#3, 10.4.6.3#4)
4. Stop the Analyzer
5. Teardown the Path
6. Verify in the trace that after seeing AUX Request to read DPCD address 00200h and AUX Response with data = 0, the DP IN Adapter sends a SET\_SINK\_COUNT SET\_CONFIG Packet with the *SINK\_COUNT* field set to 0b

## TD 10.014 DP OUT MFDP TD\_DP OUT\_6

### A. Purpose:

- Verify that the DP OUT Adapter reduces number of lanes to 2 with MFDP (if exposed connector is a USB Type-C connector)

### B. Asserts:

- 10.4.5.1#2
- 10.4.5.1#3

### C. Setup:

- AN\_DEV\_UFP1—DPOUT\_03
- AN\_HUB\_UFP1—DPOUT\_07

*Note: DP LSPCON is a Multi-Function DP Dongle*

### D. Procedure:

USB4 CV performs the following steps:

Part 1 – USB4 DP Teardown Tunnel upon Sink Count Equal 0

1. Connect the setup
2. Before setting up the DP Paths, read DP\_LOCAL\_CAP register from DP OUT Adapter and verify that *Maximal Lane Count* field is set to 1h (2 lanes). (10.4.5.1#3)
3. Verify that the DP IN Adapter and DP OUT Adapter are paired and Path is set between them
4. Verify that the DP OUT Adapter sends SET\_CONFIG Packet of type SET\_MFDP with *MFDP Enable* bit set to 1b. (10.4.5.1#2)
5. Verify that the number of lanes is 2 by reading DP\_STATUS.Lane Count (bits 2:0) in both DP Adapters. Value is set to 2h. (10.4.5.1#3)
6. Verify that the picture on the monitor is stable

## TD 10.015 DP OUT Adapter with HDCP TD\_DP OUT\_7

### A. Purpose:

- Verify that the DP OUT Adapter pass DP HDCP CTS tests (if supported)

### B. Asserts:

- 10#3
- 10#4
- 10.1.3#1
- 10.5.6#3

### C. Setup:

- AN\_DEV\_UFP1—DPOUT\_02
- AN\_HUB\_UFP1—DPOUT\_06

### D. Repetitions:

- Repeat the tests for every link type:
  - 8b/10b SST
  - 8b/10b MST (If Supported)
  - 128b/132b (If Supported)

### E. Procedure:

USB4 CV performs the following steps:

#### Part 1 – USB4 DP CTS HDCP Downstream Procedure with Receiver

1. Connect the setup
2. Run the tests 1A-XX Source Device HDCP Downstream procedure with Receiver define in HDCP CTS for DP reference above
3. Follow plug/unplug for pair/teardown the tunnel
4. Verify that the UUT passes all tests (10#3, 10#4, 10.1.3#1, 10.5.6#3)

#### Part 2 – USB4 DP CTS HDCP Downstream Procedure with Repeater

5. Connect the setup
6. Run the tests 1B-XX Source Device HDCP Downstream Procedure with Repeater define in HDCP CTS for DP reference above
7. Follow plug/unplug for pair/teardown the tunnel
8. Verify that the UUT passes all of the tests (10#3, 10#4, 10.1.3#1, 10.5.6#3)

#### Part 3 – USB4 DP CTS HDCP Upstream procedure with Transmitter

9. Connect the setup
10. Run the tests 2C-XX Sink Device HDCP Upstream procedure with Transmitter define in HDCP CTS for DP reference above

11. Follow plug/unplug for pair/teardown the tunnel
12. Verify that the UUT passes all of the tests (10#3, 10#4, 10.1.3#1, 10.5.6#3)

#### TD 10.105 DP OUT Adapter Link Bring Up

A. Purpose:

- Verify Init Adapter flow, Link Training flow

B. Asserts:

- TBD

C. Setup:

- AN\_HOST\_DFP1—DPOUT\_01
- AN\_DEV\_UFP1—DPOUT\_02
- AN\_DEV\_UFP1—DPOUT\_04
- AN\_HUB\_UFP1—DPOUT\_06
- AN\_HUB\_UFP1—DPOUT\_08

D. Repetitions:

Repeat the tests for the following permutations:

- a. Version 2 Link Partner, 128b/132b (If Supported)
  - No Downstream LTTPrs
  - Two Downstream LTTPrs
- b. Version 2 Link Partner, 8b/10b SST
  - No Downstream LTTPrs
  - Two Downstream LTTPrs
- c. Version 2 Link Partner, 8b/10b MST (If Supported)
  - No Downstream LTTPrs
  - Two Downstream LTTPrs
- d. Version 1 Link Partner, 8b/10b SST
- e. Version 1 Link Partner, 8b/10b MST (If Supported)

E. Procedure:

USB4 CV performs the following steps:

##### Part 1 – Link Bring up till first High-Speed Tunneled Packet

1. Connect the setup
2. Start Analyzer recording
3. Setup the DP Paths
4. Both Adapters are Version 2 if the UUT is a Version 2 Router, AND

- a. Link Partner is a Host Router: DP\_REMOTE\_CAP.*Protocol Adapter Version* is equal to 5
  - b. Link Partner is a Device Router: DP\_LOCAL\_CAP.*Protocol Adapter Version* is equal to 5
5. Verify the DP OUT Adapter sends HPD Status Packet (PDF = 1h) with *P* bit set to 1b.
6. Verify the DP OUT Adapter sends a SET\_MFDP SET\_CONFIG Packet with the *MFDP Enable* bit set to 0b
  - a. Verify it sent the Packet within tDPInit time after receiving a SET\_MFDP SET\_CONFIG Packet from DP IN Adapter
7. If both Adapters are Version 2
  - a. Verify that the DP OUT Adapter sends a CABLE\_DISCOVERY SET\_CONFIG Packet within tDPInit from receiving a CABLE\_DISCOVERY SET\_CONFIG Packet

#### **For 8b/10b**

8. If a DP IN Adapter sends a SET\_STREAM\_MODE SET\_CONFIG Packet, Verify the DP OUT sends in reply a SET\_STREAM\_MODE SET\_CONFIG Packet within tDPInit time.
9. DP IN Adapter sends an 8b\_10b\_SET\_LINK SET\_CONFIG Packet with the *DP Link Training Mode* bit set to 0b for LTTPR Transparent or 1b for LTTPR Non-Transparent.
  - a. USB4CV stores the *LC* and *LR* fields as original Link parameters.
10. If LTTPR Transparent. Verify all steps occur in order. Note that other SET\_CONFIG and AUX Packets may be present
  - a. Verify DP OUT sends CR\_STATUS SET\_CONFIG Packet with MSG Data Bits [3:0] are not equal to 0h and bit 7 is equal to 0b
  - b. Verify DP OUT sends 8b10b\_SET\_LINK SET\_CONFIG Packet with the same *LC* and *LR* fields as received from DP IN Adapter

#### **For 128b/132b.** Verify all steps occur in order

11. The DP IN Adapter sends 128b132b\_SET\_LINK SET\_CONFIG Packet with
  - a. *LINK\_BW\_SET* field set to 01h, 02h or 04h
  - b. *LANE\_COUNT\_SET* field set to 01h, 02h or 04h
12. Verify the DP OUT Adapter sends 128b132b\_EQ\_DONE SET\_CONFIG Packet with
  - a. *Local EQ\_DONE* bit set to 1b
  - b. *128b/132b DPRX\_EQ\_INTERLANE\_ALIGN\_DONE* bit set to 1b
  - c. *128b/132b\_LT\_FAILED* bit set to 0b
13. The DP IN Adapter sends 128b132b\_CDS SET\_CONFIG Packet
14. The DP IN Adapter sends at least one DP Clock Sync Packet.
15. Verify the DP OUT Adapter sends 128b132b\_CDS\_DONE SET\_CONFIG Packet within 20ms
16. The DP IN Adapter sends 128b132b\_SWITCH\_TO\_1BIT\_CDI SET\_CONFIG Packet
17. The DP IN Adapter sends AUX Tunnel Packet writing 102h address with value 0h
18. Verify the DP OUT Adapter sends 128b132b\_SWITCH\_TO\_1BIT\_CDI\_DONE SET\_CONFIG Packet

#### **Part 2 – General Checks**

19. Verify the gap between two SET\_CONFIG Packets sent by the DP OUT Adapter is at least 50 uSec
20. If both Adapters are Version 2
  - a. Verify all SET\_CONFIG Packets has *V2* bit set to 1b (Version 2 format)
21. Else, Verify all SET\_CONFIG Packets has *V2* bit set to 0b (Version 1 format)
22. Verify that all ACK Packets sent by the DP OUT Adapter
  - a. Sent within 4uSec after receiving a SET\_CONFIG Packet
  - b. The *Type* field in the ACK Tunnel Packet Payload is 0h
23. Verify correct *ECC* field in all SET\_CONFIG Packets sent by the DP OUT Adapter
24. Verify correct *CRC32* field in all AUX Tunnel Packets sent by the DP OUT Adapter

## TBT3-Compatibility Tests

### TBT3 DP IN Adapter LTTPR Test TD\_TBT3\_DP IN\_1

*Note: This test is only run on routers that are TBT3 Compatible.*

#### A. Purpose:

- Verify that a TBT3-Compatible DP IN Adapter works with DP OUT Adapter that Only Supports Non-LTTPR Mode

#### Asserts:

- 13.8.1.1#3

#### Setup:

- AN\_HOST\_DFP1-DPIN\_01
- AN\_DEV\_UFP1-DPIN\_03
- AN\_HUB\_UFP1-DPIN\_05

#### Procedure:

USB4 CV performs the following steps:

1. Connect test setup
2. Disable LTTPR functionality by setting the *Protocol Adapter Version* fields to 3h:
  - a. When copying DP\_LOCAL\_CAP to DP\_REMOTE\_CAP set the *Protocol Adapter Version* field to 3h for both DP Adapters.
3. Start Analyzer
4. Setup DP Paths
5. Wait for 5 seconds and stop Analyzer
6. Verify that the picture on the screen is stable
7. Verify the DP IN Adapter didn't send any AUX Transaction to addresses F0000h-F02FFh. (13.8.1.1#3)

## DP CTS Link Layer Tests

Below is the meaning of the tests classifications:

- Yes – The test is required to run as part of the Compliance certification.
- Skipped – The test is not required to run as part of the Compliance certification, but there should not be any technical barrier to execute it over DP Tunneling setup.
- NA – The test cannot be executed over DP Tunneling

## Source Testing Tables

- For DP IN Adapter UUT:
  - If the DPTX can be tested in a manner other than DP Tunneling, then the full Source Testing according to VESA CTS shall be used in the alternative manner and the test to run as part of DP Tunneling CTS are the tests which states ‘Yes’ in the “DP Tunneling Subset” column, otherwise the tests to run are the tests which states ‘Yes’ in the “DP Tunneling Only”.
- For DP OUT Adapter UUT:
  - The test to run as part of DP Tunneling CTS are the tests which states ‘Yes’ in the “DP OUT Adapter UUT” column.



**Table 8 – Source Device Services Test Procedures**

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>	<b>DP OUT Adapter UUT</b>
<b>4.2.1 AUX Reads after HPD Plug Event</b>				
4.2.1.1	Source DUT Retry on No-Reply During AUX Read after HPD Plug Event	Yes	Yes	Yes
4.2.1.2	Source Retry on Invalid Reply During AUX Read after HPD Plug Event	Skipped	Yes	Yes
4.2.1.3	Source Device HPD Event Pulse Length Test	Skipped	Yes	Yes
4.2.1.4	Source Device IRQ HPD Pulse Length Test	Skipped	Yes	Yes
4.2.1.5	Source Device Inactive HPD / Inactive AUX Test	Skipped	Yes	Yes
<b>4.2.2 EDID and DPCD Reads</b>				
4.2.2.1	DPCD Receiver Capability and EDID Read upon HPD Plug Event	Yes	Yes	Yes
4.2.2.2	DPCD Extended Receiver Capability and EDID Read upon HPD Plug Event	Yes	Yes	Yes
4.2.2.3	EDID Read	Deprecated		
4.2.2.4	EDID Read Failure #1: I2C-Over-AUX NACK	Yes	Yes	Skipped
4.2.2.5	EDID Read Failure #2: I2C-Over-AUX DEFER	Yes	Yes	Skipped
4.2.2.6	EDID Corruption Detection	Deprecated		
4.2.2.7	Branch Device Detection upon HPD Plug Event	Skipped	Yes	Skipped
4.2.2.8	EDID Read on IRQ HPD Event after Branch Device Detection	Yes	Yes	Yes
4.2.2.9	E-DDC Four Block EDID Read	Deprecated		
4.2.2.10	Link Status/Adjust Request AUX read interval during Link Training	Yes	Yes	Yes
4.2.2.11	Various UHBR AUX read interval verification in first EQ loop	Skipped	Skipped	Yes
4.2.2.12	UHBR Link Status/Adjust different FFE Request, different AUX read interval for 10 EQ loop	Skipped	Skipped	Yes

**Table 9 – Source Device Link Services Test Procedures**

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>	<b>DP OUT Adapter UUT</b>
<b>4.3.1 Link Training</b>				
4.3.1.1	Successful Link Training at All Supported Lane Counts and Link Speeds	Yes	Yes	Yes
4.3.1.2	Successful Link Training Upon HPD Plug Event	Skipped	Yes	Skipped
4.3.1.3	Successful Link Training with Request of Higher Differential Voltage Swing during Clock Recovery Sequence	Skipped	Yes	Yes
4.3.1.4	Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing	Yes	Yes	Yes
4.3.1.5	Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing	Yes	Skipped	Yes
4.3.1.6	Successful Link Training with Request of a Higher Pre-emphasis Setting during Channel Equalization Sequence	Yes	Skipped	Yes
4.3.1.7	Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock during Channel Equalization Sequence	Yes	Yes	Yes
4.3.1.8	Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing	Yes	Yes	Yes
4.3.1.9	Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing	Yes	Yes	Yes
4.3.1.10	Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5)	Yes	Yes	Yes
4.3.1.11	Successful Link Training with Simultaneous Request for Differential Voltage Swing and Pre-emphasis during Clock Recovery Sequence	Yes	Yes	Yes
4.3.1.12	Source Device Link Training CR Fallback Test	Skipped	Yes	Yes
4.3.1.13	Source Device Link Training EQ Fallback Test	Skipped	Yes	Yes
4.3.1.14	Successful Link Training at All Supported Lane Counts and UHBR Link Speeds	Yes	Yes	Yes
4.3.1.15	Successful Link Training Upon HPD Plug Event for UHBR speed	Skipped	Yes	Skipped

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.3.1.16	Successful Link Training when EQ done at 20th loop during channel EQ phase	Skipped	Yes	Yes
4.3.1.17	Successful Link Training to a Lower Bandwidth, when CHANNEL_EQ_DONE bits not set in 20 loops during channel EQ phase	Yes	Yes	Yes
4.3.1.18	Successful Link Training to a Lower Bandwidth. When LT Failed received in middle of 20 loop (random value 1 to 19) during channel EQ Done	Yes	Yes	Yes
4.3.1.19	Successful Link Training to a Lower Bandwidth. When LT Failed received at 20th loop during channel EQ Done	Yes	Yes	Yes
4.3.1.20	Successful Link Training to a Lower Bandwidth. When LT Failed received at after EQ done	Yes	Yes	Yes
4.3.1.21	Successful Link Training to a Lower Bandwidth. When EQ_INTERLANE_ALIGN_DONE bit not set during EQ phase	Yes	Yes	Yes
4.3.1.22	Successful Link Training to a Lower Bandwidth. When Symbols not locked during CDS phase.	Yes	Yes	Yes
4.3.1.23	Successful Link Training to a Lower Bandwidth. When CDS_INTERLANE_ALIGN_DONE bit not set during CDS phase.	Yes	Yes	Yes
4.3.1.24	UHBR Fallback rate table validation	Skipped	Yes	Yes
4.3.2 Link Maintenance				
4.3.2.1	Successful Link Re-training after IRQ_HPD Pulse Due to Loss of Symbol Lock	Yes	Yes	Yes
4.3.2.2	Successful Link Re-training after IRQ_HPD Pulse Due to Loss of Clock Recovery Lock	Yes	Yes	Yes
4.3.2.3	Successful Link Re-training after IRQ_HPD Pulse Due to Loss of Inter-lane Alignment Lock	Yes	Yes	Yes
4.3.2.4	Handling of IRQ_HPD Pulse with No Error Status Bits Set	Skipped	Yes	Skipped
4.3.2.5	Lane Count Reduction	NA	NA	NA
4.3.3 Video Time Stamp Generation				

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.3.3.1	8b/10b DP Rate Video Time Stamp Generation	Yes*	Yes*	Yes*
4.3.3.2	UHBR Video Time Stamp Generation	Yes	Yes	Yes

\* Not include empty TU: VIC=1 over HBR3\*4L, HBR3\*2L, HBR2\*4L

**Table 10 – Source Isochronous Transport Services Test Procedures**

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.4.1 Main Stream Data Mapping				
4.4.1.1	8b/10b DP Rate Pixel Data Packing and Steering	Yes	Yes	Yes
4.4.1.2	8b/10b DP Rate Main Stream Data Packing and Stuffing– Least Packed TU	Yes*	Yes*	Yes*
4.4.1.3	8b/10b DP Rate Main Stream Data Packing and Stuffing – Most Packed TU	Yes	Yes	Yes
4.4.1.4	UHBR Rate Pixel Data Packing and Steering	Yes	Yes	Yes
4.4.1.5	UHBR Rate Main Stream Data Packing and Stuffing – Least Packed MTP	Yes	Yes	Yes
4.4.1.6	UHBR Rate Main Stream Data Packing and Stuffing – Most Packed MTP	Yes	Yes	Yes
4.4.2 Main Video Stream Format Change Handling				
4.4.2.1	8b/10b DP Rate Main Video Stream Format Change Handling	Yes	Yes	Yes
4.4.2.2	UHBR Rate Main Video Stream Format Change Handling	Yes	Yes	Yes
4.4.3	Power Management	NA	NA	NA
4.4.4 Audio Stream Transmission over Secondary Packets				
4.4.4.1	Configuring Video and Audio Parameters	Skipped	Yes*	Skipped
4.4.4.2	Audio Stream Header Synchronization	Skipped	Yes*	Skipped
4.4.4.3	Audio Time Stamp Generation	Yes*	Yes*	Yes
4.4.4.4	Audio INFOFRAME Packet	Skipped	Yes*	Skipped

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.4.4.5	Audio Stream Transmission	Yes*	Yes*	Yes
4.4.4.6	Audio Start Sequence	Skipped	Yes*	Yes
4.4.4.7	DSC (RB2 Timing) Audio Stream Transmission	Yes*	Yes*	Yes

\* Not include empty TU: VIC=1 over HBR3\*4L, HBR3\*2L, HBR2\*4L

**Table 11 – Source Device FEC Test Procedures**

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.5.1 Source FEC Protocol				
4.5.1.1	FEC Enable Verification for All Supported Lane Count and Link Speed	Yes	Yes	Yes
4.5.1.2	FEC Ready Verification for Non FEC Capable Sink	Skipped	Yes	Skipped

**Table 12 – Source Device DSC Test Procedures**

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.6.1 Source DSC Protocol				
4.6.1.1	DSC enable sequence verification	Skipped	Yes	Yes
4.6.1.2	DSC PPS block prediction flag verification	Skipped	Yes	Yes
4.6.1.3	DSC PPS convert RGB flag verification	Yes	Yes	Yes
4.6.1.4	DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification	Skipped	Yes	Yes
4.6.1.5	DSC PPS Simple 4:2:2 flag verification	Skipped	Yes	Yes
4.6.1.6	DSC PPS Native 4:2:2 flag verification	Skipped	Yes	Yes
4.6.1.7	DSC PPS Native 4:2:0 flag verification	Yes	Yes	Yes
4.6.1.8	DSC PPS convert RGB flag verification for DSC Algorithm Revision 1.1	Skipped	Yes	Yes

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.6.1.9	DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification for DSC Algorithm Revision 1.1	Skipped	Yes	Yes

**Table 13 – Source Device LTTTPR Test Procedures**

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.9.1 Source Embedded LTTTPR protocol				
4.9.1.1	With 1 emulated LTTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	Yes	Yes	Yes
4.9.1.2	With 2 emulated LTTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	Yes	Yes	Yes
4.9.1.3	With 3 emulated LTTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	Yes	Yes	Yes
4.9.1.4	With 4 emulated LTTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	Yes	Yes	Yes
4.9.1.5	With 5 emulated LTTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	Yes	Yes	Yes
4.9.1.6	With 6 emulated LTTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	NA	NA	NA
4.9.1.7	With random[1-6] number of emulated LTTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds, Sink support 4 lane and all rates	Yes	Yes	Skipped
4.9.1.8	With random[1-6] number of emulated LTTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds, LTTTPR support 4 lane and all rates	Skipped	Yes	Skipped
4.9.1.9	With random[1-6] number of emulated LTTTPR, Successful Link Training (Higher Differential Voltage Swing during Clock Recovery).	Skipped	Skipped	Yes
4.9.1.10	With random[1-6] number of emulated LTTTPR, Successful Link Training to a Lower Link Rate/BW #1: Iterate at Maximum Voltage Swing	Skipped	Skipped	Yes

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>	<b>DP OUT Adapter UUT</b>
4.9.1.11	With random[1-6] number of emulated LTTTPR, Successful Link Training to a Lower Link Rate/BW #2: Iterate at Minimum Voltage Swing	Yes	Yes	Yes
4.9.1.12	With random[1-6] number of emulated LTTTPR, Successful Link Training (Higher Pre-emphasis Setting during Channel Equalization).	Yes	Yes	Yes
4.9.1.13	With random[1-6] number of emulated LTTTPR, Successful Link Training (Lower Link Rate/BW During Channel Equalization).	Skipped	Skipped	Yes
4.9.1.14	With random[1-6] number of emulated LTTTPR, Successful Link Training when EQ done at 20th loop during channel EQ phase	Skipped	Skipped	Yes
4.9.1.15	With random[1-6] number of emulated LTTTPR, Successful Link Training to a Lower Bandwidth, when CHANNEL_EQ_DONE bits not set in 20 loops during channel EQ phase	Yes	Yes	Yes
4.9.1.16	With random[1-6] number of emulated LTTTPR, Successful Link Training to a Lower Bandwidth. When LT Failed received in middle of 20 loop (random value 1 to 19) during channel EQ Done	Skipped	Skipped	Yes
4.9.1.17	With random[1-6] number of emulated LTTTPR, Successful Link Training to a Lower Bandwidth. When LT Failed received at 20th loop during channel EQ Done	Skipped	Skipped	Yes
4.9.1.18	With random[1-6] number of emulated LTTTPR, Successful Link Training to a Lower Bandwidth. When LT Failed received at after EQ done	Yes	Yes	Yes
4.9.1.19	With random[1-6] number of emulated LTTTPR, Successful Link Training to a Lower Bandwidth. When EQ_INTERLANE_ALIGN_DONE bit not set during EQ phase	Yes	Yes	Yes
4.9.1.20	With random[1-6] number of emulated LTTTPR, Successful Link Training to a Lower Bandwidth. When Symbols not locked during CDS phase	Skipped	Skipped	Yes
4.9.1.21	With random[1-6] number of emulated LTTTPR, Successful Link Training to a Lower Bandwidth. When CDS_INTERLANE_ALIGN_DONE bit not set during CDS phase	Yes	Yes	Yes





## Sink Testing Tables

If the DPRX can be tested in a manner other than DP Tunneling, then the full Sink Testing according to VESA CTS shall be used in the alternative manner and the test to run as part of DP Tunneling CTS are the tests which states ‘Yes’ in the “DP Tunneling Subset” column, otherwise the tests to run are the tests which states ‘Yes’ in the “DP Tunneling Only”.

**Table 14 – Sink Device Services Test Procedures**

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only
5.2.1 AUX_CH Protocol			
5.2.1.1	Read One Byte from Valid DPCD Address	Deprecated	
5.2.1.2	DPCD Receiver Capability Read (Read 12 Bytes from Valid DPCD Address)	Deprecated	
5.2.1.3	Write One Byte to Valid DPCD Address	Deprecated	
5.2.1.4	Write Nine Bytes to Valid DPCD Addresses	Deprecated	
5.2.1.5	Write EDID Offset (One Byte I2C-over-AUX Write)	Deprecated	
5.2.1.6	Read One EDID Byte (One Byte I2C-over-AUX Read)	Deprecated	
5.2.1.7	EDID Read (1 Byte I2C -over-AUX Segment Write, 1 Byte I2C-over-AUX Offset Write, 128 Byte I2C-over-AUX Read)	Deprecated	
5.2.1.8	Illegal AUX Request Syntax	Skipped	Skipped
5.2.1.9	Glitch Rejection	Skipped	Skipped
5.2.1.10	Interleaved EDID and DPCD Receiver Capability Read	Yes	Yes
5.2.1.11	Downstream Stop on MOT Reset	Skipped	Yes
5.2.1.12	Downstream Stop on Timeout	Skipped	Yes
5.2.2 Sink Device DPCD Field Implementation			
5.2.2.1	Sink Organizationally Unique Identifier (OUI)	Skipped	Yes
5.2.2.2	Sink Count	Skipped	Yes
5.2.2.3	Sink Status	Skipped	Yes

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>
5.2.2.4	Sink Error Count (Deprecated)	Deprecated	
5.2.2.5	DPCD Address Range	Skipped	Yes
5.2.2.6	Number of Receiver Ports	Skipped	Yes
5.2.2.7	Main-Link Channel Coding	Skipped	Yes
5.2.2.8	ESI Field Mapping	Skipped	Yes
5.2.2.9	Sink Device Symbol Error Count	Skipped	Skipped

**Table 15 – Sink Device Link Services Test Procedures**

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>
<b>5.3.1 Link Training</b>			
5.3.1.1	Successful Link Training at All Supported Lane Counts and Link Speeds	Yes	Yes
5.3.1.2	Successful Link Training with Request of Higher Differential Voltage Swing during Clock Recovery Sequence	NA	NA
5.3.1.3	Successful Link Training to a Lower Link Rate Due to Clock Recovery Lock Failure during Clock Recovery Sequence	NA	NA
5.3.1.4	Successful Link Training with Request of a Change to Pre-Emphasis and/or Voltage Swing Setting during Channel Equalization Sequence	NA	NA
5.3.1.5	Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock during Channel Equalization Sequence	Skipped	Skipped
5.3.1.6	Lane Count Reduction	NA	NA
5.3.1.7	Lane Count Increase	NA	NA
5.3.1.8	Sink Device 2-Lane Link Training CR/EQ Fallback Test	Skipped	Skipped

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>
5.3.1.9	Sink Device 1-Lane Link Training CR/EQ Fallback Test	Skipped	Skipped
5.3.1.10	Successful Link Training at All Supported Lane Counts and UHBR Link Speeds	Yes	Yes
5.3.1.11	Successful Link Training to lower bandwidth, due to failure in EQ Phase of UHBR	Yes	Yes
5.3.1.12	Successful Link Training to lower bandwidth, due to failure in CDS Phase of UHBR	Yes	Yes
5.3.1.13	Successful Link Training to lower bandwidth, due to no start of CDS sequence Phase of UHBR Link Training	Yes	Yes
5.3.1.14	2-Lane UHBR Link Training EQ Fallback Test	Skipped	Skipped
5.3.1.15	1-Lane UHBR Link Training EQ Fallback Test	Skipped	Skipped
<b>5.3.2 Link Maintenance</b>			
5.3.2.1	IRQ_HPDP Pulse Due to Loss of Symbol Lock and Clock Recovery Lock	Yes	Yes
5.3.2.2	IRQ_HPDP Pulse Due to Loss of Inter-lane Alignment Lock	NA	NA

**Table 16 – Sink Isochronous Transport Services Test Procedures**

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>
<b>5.4.1 Main Video Stream Reconstruction</b>			
5.4.1.1	8b/10b DP Rate Pixel Data Reconstruction	Yes	Yes
5.4.1.2	8b/10b DP Rate Main Stream Data Unpacking and Unstuffing – Least Packed TU	Yes	Yes
5.4.1.3	8b/10b DP Rate Main Stream Data Unpacking and Unstuffing – Most Packed TU	Yes	Yes
5.4.1.4	8b/10b DP Rate Pixel Clock Recovery	Yes	Yes
5.4.1.5	UHBR Pixel Data Reconstruction	Yes	Yes

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>
5.4.1.6	UHBR Main Stream Data Unpacking and Unstuffing – Least Packed MTP	Yes	Yes
5.4.1.7	UHBR Main Stream Data Unpacking and Unstuffing – Most Packed MTP	Yes	Yes
5.4.1.8	UHBR Pixel Clock Recovery	Yes	Yes
5.4.2.1	8b/10b DP Rate Main Video Stream Format Change Handling	Yes	Yes
5.4.2.2	UHBR Main Video Stream Format Change Handling	Yes	Yes
<b>5.4.3 Power Management</b>			
5.4.3.1	Entering and Exiting Power Save Mode	Yes	Yes
5.4.3.2	Resumption of Main-Link Activity after Extended Idle	Yes	Yes
<b>5.4.4 Main Audio Stream Reconstruction</b>			
5.4.4.1	Audio Test Patterns	Yes	Yes
5.4.4.2	Audio Startup and Format Change	Yes	Yes
5.4.4.3	RS Error Correction	Yes	Yes
5.4.4.4	Audio INFOFRAME Packet	Yes	Yes
5.4.4.5	Audio Clock Recovery	Yes	Yes
5.4.4.6	Audio Stream Reception	Yes	Yes

**Table 17 – Sink Device FEC Test Procedures**

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>
<b>5.5.1 Sink FEC Protocol</b>			
5.5.1.1	Sink Device FEC Capability Verification	Skipped	Skipped
5.5.1.2	Successful Link Training at All Supported Lane Counts and 8b/10b DP Link Rates with FEC Enable	Yes	Yes

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>
5.5.1.3	Uncorrectable Block Error Count	Skipped	Skipped
5.5.1.4	Correctable Block Error Count	Skipped	Skipped
5.5.1.5	Correctable Bit Error Count	Skipped	Skipped
5.5.1.6	Correctable Parity Block Error Count	Skipped	Skipped
5.5.1.7	Correctable Parity Bit Error Count	Skipped	Skipped
5.5.1.8	Aggregated Uncorrectable Block error count	Skipped	Skipped
5.5.1.9	Aggregated Correctable Block error count	Skipped	Skipped
5.5.1.10	Aggregated Correctable Bit error count	Skipped	Skipped
5.5.1.11	Aggregated Correctable Parity Block error count	Skipped	Skipped
5.5.1.12	Aggregated Correctable Parity Bit error count	Skipped	Skipped

**Table 18 – Sink Device DSC Test Procedures**

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>
5.6.1 Sink DSC Protocol			
5.6.1.1	DSC capability verification	Skipped	Yes
5.6.1.2	DSC RGB Color Depth Test	Skipped	Yes
5.6.1.3	DSC RGB Block Prediction Test	Skipped	Yes
5.6.1.4	DSC RGB bits-per-pixel Test	Yes	Yes
5.6.1.5	DSC RGB slice Test	Yes	Yes
5.6.1.6	DSC RGB lane Test	Yes	Yes
5.6.1.7	DSC YCbCr 4:4:4 Color Depth Test	Skipped	Yes
5.6.1.8	DSC YCbCr 4:4:4 Block Prediction Test	Skipped	Yes
5.6.1.9	DSC YCbCr 4:4:4 bits-per-pixel Test	Skipped	Yes

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>
5.6.1.10	DSC YCbCr 4:4:4 slice Test	Skipped	Yes
5.6.1.11	DSC YCbCr 4:4:4 lane Test	Skipped	Yes
5.6.1.12	DSC Simple 4:2:2 Color Depth Test	Skipped	Yes
5.6.1.13	DSC Simple 4:2:2 Block Prediction Test	Skipped	Yes
5.6.1.14	DSC Simple 4:2:2 bits-per-pixel Test	Skipped	Yes
5.6.1.15	DSC Simple 4:2:2 slice Test	Skipped	Yes
5.6.1.16	DSC Simple 4:2:2 lane Test	Skipped	Yes
5.6.1.17	DSC Native 4:2:2 Color Depth Test	Skipped	Yes
5.6.1.18	DSC Native 4:2:2 Block Prediction Test	Skipped	Yes
5.6.1.19	DSC Native 4:2:2 bits-per-pixel Test	Yes	Yes
5.6.1.20	DSC Native 4:2:2 slice Test	Yes	Yes
5.6.1.21	DSC Native 4:2:2 lane Test	Yes	Yes
5.6.1.22	DSC Native 4:2:0 Color Depth Test	Skipped	Yes
5.6.1.23	DSC Native 4:2:0 Block Prediction Test	Skipped	Yes
5.6.1.24	DSC Native 4:2:0 bits-per-pixel Test	Yes	Yes
5.6.1.25	DSC Native 4:2:0 slice Test	Yes	Yes
5.6.1.26	DSC Native 4:2:0 lane Test	Yes	Yes
<b>5.6.2 Sink DSC Protocol Extension for 8b/10b DP Rate</b>			
5.6.2.1	DSC Height Test	Skipped	Yes
5.6.2.2	DSC Padding Test	Yes	Yes
5.6.2.3	DSC RGB min and max bits-per-pixel Test	Yes	Yes
5.6.2.4	DSC YCbCr 4:4:4 min and max bits-per-pixel Test	Skipped	Yes
5.6.2.5	DSC Simple 4:2:2 min and max bits-per-pixel Test	Skipped	Yes

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP Tunneling Subset</b>	<b>DP Tunneling Only</b>
5.6.2.6	DSC Native 4:2:2 min and max bits-per-pixel Test	Yes	Yes
5.6.2.7	DSC Native 4:2:0 min and max bits-per-pixel Test	Yes	Yes
5.6.2.8	DSC RGB most pack Test	Yes	Yes
5.6.2.9	DSC Native 4:2:2 most pack Test	Yes	Yes
5.6.2.10	DSC Native 4:2:0 most pack Test	Yes	Yes
5.6.2.11	DSC one corrupt slice Test	Skipped	Yes
5.6.2.12	DSC interrupt test for Chunk Length error	Skipped	Yes
5.6.2.13	DSC interrupt test for RC buffer under-run error	Skipped	Yes
5.6.2.14	DSC interrupt test for RC buffer overflow error	Skipped	Yes
5.6.2.15	Sink device handling of per slice rates and slice count capability	Skipped	Yes
5.6.2.16	DSC Validation for 1/16 BPP at 8b/10b DP Rate	Skipped	Yes
<b>5.6.3 Sink DSC Protocol Extension for UHBR Rates</b>			
5.6.3.1	DSC Validation at UHBR Rates	Skipped	Yes
5.6.3.2	UHBR Rate DSC RGB most pack test	Skipped	Yes
5.6.3.3	UHBR Rate DSC Native 4:2:2 most pack test	Skipped	Yes
5.6.3.4	UHBR Rate DSC Native 4:2:0 most pack test	Skipped	Yes
5.6.3.5	Sink device handling of per slice rates and slice count capability for UHBR rate	Skipped	Yes
5.6.3.6	DSC Validation for 1/16 BPP at UHBR Rate	Skipped	Yes

**Table 19 – Sink Device Embedded LTTTPR Test Procedures**

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only
5.9.1 Sink Embedded LTTTPR protocol			
5.9.1.1	LTTTPR global configuration verification	Skipped	Yes
5.9.1.2	LTTTPR configuration and status field verification	Skipped	Yes
5.9.1.3	LTTTPR AUX read/write reply time budget verification	Skipped	Yes
5.9.1.4	LTTTPR 8b10b transparent link training for lane count and link rate	Yes	Yes
5.9.1.5	LTTTPR 8b10b non-transparent link training for lane count and link rate	Yes	Yes
5.9.1.6	LTTTPR 128b132b non-transparent link training for lane count and link rate	Yes	Yes
5.9.1.7	LTTTPR 8b10b transparent successful Link Training (Higher Differential Voltage Swing during Clock Recovery)	Skipped	Yes
5.9.1.8	LTTTPR 8b10b non-transparent successful Link Training (Higher Differential Voltage Swing during Clock Recovery)	Skipped	Yes
5.9.1.9	LTTTPR 8b10b transparent successful Link Training (Lower Link bandwidth During Clock Recovery)	Skipped	Yes
5.9.1.10	LTTTPR 8b10b non-transparent successful Link Training (Lower Link bandwidth During Clock Recovery)	Skipped	Yes
5.9.1.11	LTTTPR 8b10b transparent successful Link Training (Lower Link Bandwidth Channel Equalization)	Skipped	Yes
5.9.1.12	LTTTPR 8b10b non-transparent successful Link Training (Lower Link Bandwidth Channel Equalization)	Skipped	Yes
5.9.1.13	LTTTPR 128b132b non-transparent successful Link Training to Lower Link Rate, due to failure in EQ Phase of UHBR	Yes	Yes
5.9.1.14	LTTTPR 128b132b non-transparent successful Link Training to Lower Link Rate, due to failure in CDS Phase of UHBR	Yes	Yes
5.9.1.15	LTTTPR 128b132b non-transparent successful Link Training to lower bandwidth, due to no start of CDS sequence Phase of UHBR Link Training	Yes	Yes



**Table 20 – LTPR and DP Tunnel Device Test Procedures**

<b>DP CTS Test Number</b>	<b>Test Name</b>	<b>DP IN Adapter</b>	<b>DP OUT Adapter</b>
<b>7.1 LTPR Device Test Procedures</b>			
7.1.1	LTPR Device Capabilities validation tests	Yes	Yes
7.1.2	LTPR 8b/10b DP Transparent Link Training validation tests	Yes	Yes
7.1.3	LTPR 8b/10b DP Non-transparent Link Training validation tests	Yes	Yes
7.1.4	LTPR 128b/132b DP Non-transparent Link Training validation tests	Yes	Yes
7.1.5	LTPR 8b/10b DP Symbol error validation tests	Yes	Skipped
7.1.6	LTPR 8b/10b DP FEC status and error validation tests	Yes	Skipped
7.1.7	LTPR 128b/132b DP FEC status and error validation tests	Yes	Skipped
7.1.8	LTPR 8b/10b DP Non-LTPR Link Training validation tests	Yes	Yes
7.1.9	LTPR Link Maintenance validation tests	Yes	Yes
7.1.10	LTPR DSC validation tests for SST and MST	Yes	Yes
7.1.11	LTPR HDCP validation tests for SST and MST	Yes	Yes
7.1.12	LTPR Split SDP validation tests	Yes	Yes
<b>7.2 DP Tunnel Device Test Procedures</b>			
7.2.1	DP Tunnel error counter validation tests	Yes	Skipped

## Known Good GPU(s) Capabilities

The test coverage provided by DP Link Layer Compliance Tests executed in Test Setups that make use of a Known Good (KG) GPU highly depends on the capabilities of the KG GPU(s) (or DP Source). The KG GPU(s) (or DP Source) used for testing shall support the capabilities outlined in Table 21.

**Table 21 – Known Good GPU(s) or DP Source Capabilities Requirements**

Capability	Support Level
Maximum Supported Lane Count	4 (Lanes 0, 1, 2, 3)
Maximum Supported Link Rate	8.1Gbps/lane (HBR3)
Device Test Automation DPCD extension	Yes
Spread-spectrum Clocking (SSC)	Yes
Video format change without link retraining	Yes
Supported Pixel Encoding/Colorimetry Formats	RGB YCbCr 4:4:4 YCbCr 4:2:2 YCbCr 4:2:0
Maximum bits per component (bpc)	16 bpc
FEC	Yes
Audio Transmission with Video	Yes
Audio Sample Rates Supported	32 kHz 44.1 kHz 48 kHz 88.2 kHz 96 kHz 176.4 kHz 192 kHz
DSC Support	Yes
DSC Colorimetry	RGB YCbCr 4:4:4 Simple 4:2:2 Native 4:2:2 Native 4:2:0

Capability	Support Level
DSC Maximum BPC	12
HDCP and CP_IRQ	Yes

## Window Count Calculation

	Window time in nS														
	Nominal	Max [+100ppm]	Min [-100ppm]												
	2097152	2097370	2096934												
Calculation using UI															
	UI Time [nS]			Lifetime Counter Increment time [nS]			Window Count Decimal (w/ fraction)			Window Count Hex			2		
Link Rate [GHz]	Nominal	Max [+300ppm]	Min [-2800ppm]	Nominal	Max [+300ppm]	Min [-2800ppm]	Nominal	Max	Min	Nominal	Max	Min	PPM From Max WC		
1.62	0.617283951	0.617098765	0.619012346	6.172839506	6.170987654	6.190123457	86973088	87008231	86721227	52F1A9F	52FA3E7	52B42CB	175	AF	
2.7	0.37037037	0.370259259	0.371407407	3.703703704	3.702592593	3.714074074	144955146	145013719	144535379	8A3D70A	8A48BD6	89D6F53	291	123	
5.4	0.185185185	0.18512963	0.185703704	3.703703704	3.702592593	3.714074074	144955146	145013719	144535379	8A3D70A	8A48BD6	89D6F53	291	123	
8.1	0.12345679	0.123419753	0.123802469	2.469135802	2.468395062	2.476049383	217432719	217520578	216803069	CF5C28F	CF719C1	CEC26FC	436	184	
10	0.1	0.09997	0.10028	3.2	3.19904	3.20896	167772160	167839952	167286318	A000000	A0108CF	9F8962E	336	150	
13.5	0.074074074	0.074051852	0.074281481	2.37037037	2.369659259	2.377007407	226492416	226583935	225836530	D800000	D81657F	D75FDF1	454	1C6	
20	0.05	0.049985	0.05014	1.6	1.59952	1.60448	335544320	335679904	334572637	14000000	1402119F	13F12C5C	672	2A0	
Calculation using Frequency															
	Freq [GHz]			Lifetime Counter increment Freq [GHz]			Window Count Decimal (w/ fraction)			Window Count Hex			2		
Link Rate [GHz]	Nominal	Max [+300ppm]	Min [-2800ppm]	Nominal	Max [+300ppm]	Min [-2800ppm]	Nominal	Max	Min	Nominal	Max	Min	PPM From Max WC		
1.62	1.62	1.620486	1.615464	0.162	0.1620486	0.1615464	86973088	87008223	86720548	52F1A9F	52FA3DF	52B4023	175	AF	
2.7	2.7	2.70081	2.69244	0.27	0.270081	0.269244	144955146	145013705	144534246	8A3D70A	8A48BC9	89D6AE5	291	123	
5.4	5.4	5.40162	5.38488	0.27	0.270081	0.269244	144955146	145013705	144534246	8A3D70A	8A48BC9	89D6AE5	291	123	
8.1	8.1	8.10243	8.07732	0.405	0.4051215	0.403866	217432719	217520558	216801369	CF5C28F	CF719AE	CEC2058	436	184	
10	10	10.003	9.972	0.3125	0.31259375	0.311625	167772160	167839937	167285007	A000000	A0108C0	9F8910E	336	150	
13.5	13.5	13.50405	13.4622	0.421875	0.422001563	0.42069375	226492416	226583915	225834759	D800000	D81656A	D75F707	454	1C6	
20	20	20.006	19.944	0.625	0.6251875	0.62325	335544320	335679874	334570014	14000000	14021181	13F1221D	672	2A0	
Final: Max from UI +256, Min from Freq -256															
Link Rate [GHz]							Window Count Decimal (w/ fraction)			Window Count Hex					
1.62							Nominal	Max	Min	Nominal	Max	Min			
2.7							86973088	87008487	86720292	52F1A9F	52FA4E7	52B3F23			
5.4							144955146	145013975	144533990	8A3D70A	8A48CD6	89D69E5			
8.1							144955146	145013975	144533990	8A3D70A	8A48CD6	89D69E5			
10							217432719	217520834	216801113	CF5C28F	CF71AC1	CEC1F58			
13.5							167772160	167840208	167284751	A000000	A0109CF	9F8900E			
20							226492416	226584191	225834503	D800000	D81667F	D75F607			
							335544320	335680160	334569758	14000000	1402129F	13F1211D			