

USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: DP SR Counter Clarification

Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:

Fixes the terms about SR Count counter, as it was written from a DP IN Adapter point of view. Splits the description for DP IN Adapter and DP OUT Adapter:

- DP IN Adapter – The Counter starts when it receives SR.
- DP OUT Adapter - The Counter starts when it transmits SR.

Benefits as a result of the changes:

Avoids confusions for DP OUT implementers.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

None

An analysis of the hardware implications:

None

An analysis of the software implications:

None

An analysis of the compliance testing implications:

None

USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Actual Change

(a). 10.5.3.1 SR Count

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A DP Adapter shall implement the SR Count counter, which counts the number of cycles that have elapsed since between the last received SR, and the first cycle of the FEC_DECODE_EN or FEC_DECODE_DIS sequences. A DP IN Adapter uses this counter to measure and report to the DP OUT Adapter, the number of cycles from the last SR it received to the first cycle of the FEC_DECODE_EN or FEC_DECODE_DIS sequences. A DP OUT Adapter uses this counter to count the number of cycles which elapsed since the last SR it transmitted in order to recreate the FEC_DECODE_EN or FEC_DECODE_DIS sequences at the same cycle as the DP IN Adapter has received.

A DP IN Adapter shall initiate The the SR Count is initiated at the first cycle after receiving ~~the~~ an SR. A DP OUT Adapter shall initiate the SR Count at the first cycle after transmitting an SR according to the DisplayPort 1.4a Specification. For SST, the count starts after receiving or transmitting all four Enhanced Framing Mode Symbols. SR Count counts any link clock cycle, including cycles which carry FEC-related symbols.

(b). 10.5.3.3 DP OUT Adapter Requirements

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A DP OUT Adapter shall:

- Implement FEC Encoding as defined in the **Error! Reference source not found.**
- Apply majority voting for the repeated fields with in the FEC_DECODE Packet.
 - SR Count.
 - FEN.
 - FDS.
- Generate FEC_DECODE_EN and FEC_DECODE_DIS upon reception of a FEC_DECODE Packet.
 - FEC_DECODE_EN sequence shall be generated if *FEN* field in the FEC_DECODE Packet is 1b.
 - FEC_DECODE_DIS sequence shall be generated if *FDS* fields in the FEC_DECODE Packet is 1b.
 - The first symbol of the FEC_DECODE_EN and FEC_DECODE_DIS sequences shall be transmitted according to the *SR Count* field of the FEC_DECODE Packet, i.e. the FEC_DECODE_EN and FEC_DECODE_DIS sequence shall be transmitted SR Count link clock cycles after the most recently transmitted SR.
 - When a FEC_DECODE Packet is received, a DP OUT Adapter compares the Packet SR Count and the Counter SR Count as follows:

USB4 1.0 ENGINEERING CHANGE NOTICE FORM

- If Packet SR Count > Counter SR Count the DP OUT Adapter waits for the Counter SR Count to be equal to Packet SR Count then generate the FEC sequence.
- Else, a DP OUT Adapter waits for next SR to be transmitted, then waits for the Counter SR Count to be equal to Packet SR Count then generate the FEC sequence.