Universal Serial Bus Type-C and Power Delivery
Source Power Requirements Test Specification

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Revision: 0.78

Revision History

Revision	Issue Date	Comments
0.51	Oct 23, 2015	
0.52	Oct 26, 2015	Updates to neighbor port droop/drop checks, specific transition times
0.7	Dec 30, 2015	Revision updated for initial publication
0.71	March 1, 2017	Revision updated to add PD 3.0 asserts and PD PPS tests
0.72	May 20, 2017	Editorial fixes to PPS tests
0.73	Oct 23, 2017	Update CF test to CL test, include PD 3.0 PPS ECNs through September 2017
0.74	Jan 3, 2018	Clarify the 8mV minimum increase/decrease during PPS voltage step
0.75	June 1, 2018	Update OC test to use VIF fields
0.77	November 6, 2019	Update OC test for varied implementations, add Shared Capacity Test
0.78	May 1, 2020	Add iPpsCLTolerance checks

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1 Introduction

This test document applies to Vbus source-capable USB Type-C connector ports. The test definitions cover droop/drop, connect, disconnect, and USB PD voltage transitions, current transitions and over current protection.

The following tables show the USB documents that are referenced for test requirements, and the terms and abbreviations used in this test specification.

Table 1: USB Specifications Referenced

Test Suite	Document Information
USB PD 3.0	USB Power Delivery Rev. 3.0 v2 https://usb.org/document-library/usb-power-delivery
USB PD 2.0	USB Power Delivery Rev. 2.0 v1.3 https://usb.org/document-library/usb-power-delivery
USB Type-C	USB Type-C Cable and Connector Specification Revision 2 https://usb.org/document-library/usb-type-cr-cable-and-connector-specification-revision-20-august-2019
USB 3.2	USB 3.2 Specification Revision 1.0 and ECNs https://usb.org/document-library/usb-32-specification-released-september-22-2017-and-ecns
USB 2.0	USB 2.0 Specification https://usb.org/document-library/usb-20-specification

Table 2: Terms and Abbreviations

APDO	Alternative Power Delivery Object as defined in the USB PD 3.0 Specification
DUT	Device Under Test
LcurrMax	5.5 A. The maximum load each port on the SPT can draw
RDO	Request Data Object as defined in the USB PD Specification
pMaxDUT	The cumulative maximum power in Watts the DUT advertises it is capable of sourcing on its ports by adding concurrently-sourced pMaxPDO from each port.
pMaxSPTport	100 Watts. The maximum power each port on the SPT can handle
pMaxSPT	320 Watts. The maximum cumulative power the SPT can handle across its 4 ports.
RDO	Request Data Object as defined in the USB PD Specification

The following tables show the USB documents that are referenced for test requirements, and the terms and abbreviations used in this test specification.

2 Test Assertions

Compliance criteria are provided as a list of assertions that describe specific characteristics or behaviors that must be met. Each assertion provides a reference to the USB Power Delivery specification or other documents from which the assertion was derived. In addition, each assertion provides a reference to the specific test description(s) where the assertion is tested.

Each test assertion is formatted as follows:

Assertion #	Test #	Assertion Description

Assertion#: Unique identifier for each spec requirement. The identifier is in the form SPEC_SECTION_NUMBER#X, where X is a unique integer for a requirement in that section.

Assertion Description: Specific requirement from the specification

Test #: A label for a specific test description in this specification that tests this requirement. Test # can have one of the following values:

NT This item is not explicitly tested in a test description. Items can be labeled NT for several reasons – including items that are not testable, not important to test for interoperability, or are indirectly tested by other operations performed by the compliance test.

X.X This item is covered by the test described in test description X.X in this specification.

BC This assertion is applied as a background check in all test descriptions.

PD This assertion is verified by the USB-IF Power Delivery Test Suite.

Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

The following Tables present the USB PD r2.0 Specification and USB PD r3.0 Specification relevant asserts.

2.1 USB PD 2.0 Assertions

Assertion #	Test Name	Assertion Description
Chapter 6: Protocol Layer		
6.4 Data Message		
6.4.1 Capabilities Message		
6.4.1.2 Source_Capabiltiies Message		
6.4.1.2.1 Management of the Power Reserve		

Assertion #	Test Name	Assertion Description
6.4.1.2.1#1	SPT.4	Where a Power Reserve has been allocated to a Sink the Source shall indicate the Power Reserve as part of every Source_Capabilities Message it sends.
6.4.1.2.1#2	SPT.4	When the same Power Reserve is shared between several Sinks the Source shall indicate the Power Reserve as part of every Source_Capabilities Message it sends to every Sink.
6.4.1.2.1#3	SPT.4	When the Reserve is temporarily used by a GiveBack capable Sink the Source shall indicate the Power Reserve as available in every Source_Capabilities Message it sends.
6.4.1.2.1#4	SPT.4	When the Reserve is temporarily used by a GiveBack capable Sink, when the Power Reserve is requested by another Sink, the Source shall return a Wait Message while it retrieves this power using a GotoMin Message.
6.4.1.2.1#5	SPT.4	Once the additional power has been retrieved the Source shall send a new Source_Capabilities Message in order to trigger a new request from the Sink requesting the Power Reserve.
6.4.1.2.1#6	SPT.4	The Power Reserve may be de-allocated by the Source at any time, but the de-allocation shall be indicated to the Sink or Sinks using the Power Reserve by sending a new Source_Capabilities Message.
Chapter 7: Power Supply		
7.1 Source Requirements		
7.1.4 Positive Voltage Transitions		
7.1.4#1	BC	During the positive transition the Source shall be able to supply the Sink standby power and the transient current to charge the total bulk capacitance on Vbus.
7.1.4#2	SPT.1 SPT.2	The slew rate of the positive transition shall not exceed vSrcSlewPos.
7.1.4#3	SPT.1 SPT.2	The transitioning Source output voltage shall settle within vSrcNew by tSrcSettle.
7.1.4#4	SPT.1 SPT.2	The source shall be able to supply the negotiated power level at the new voltage by tSrcReady
7.1.4#5	SPT.1 SPT.2	The positive voltage transition shall remain monotonic while the transitioning voltage is below vSrcValid min and shall remain within the vSrcValid range upon crossing vSrcValid min.
7.1.4#6	SPT.1 SPT.2	At the start of the positive voltage transition the Vbus voltage level shall not droop vSrcValid min below either vSrcNew or vSafe5V as applicable.
7.1.6 Response to Hard Resets		
7.1.6#1	SPT.3	After establishing the vSafe0V voltage condition on Vbus, the Source shall wait tSrcRecover before restoring Vbus to vSafe5V.
7.1.6#4	SPT.3	From the start of the voltage transition, the Source shall meet vSafe5V max within tSafe5V and shall meet vSafe0V within tSafe0V.
7.1.8 Safe Operating Considerations		
7.1.8.3 Over-Current Protection		
7.1.8.3#1	SPT.5	Sources shall implement over-current protection (OCP) mechanisms.
7.1.8.3#2	SPT.5	The port level OCP mechanism shall not respond sooner than tSrcOcPresent and the over-current condition on the port shall not be present for more than tSrcOcPresent max.
7.1.9 Output Voltage Tolerance and Range		
7.1.9#1	SPT.1 SPT.2	After a voltage transition is complete and during static load conditions the Source output voltage shall remain within the vSrcNew limits.

Assertion #	Test Name	Assertion Description
7.1.9#2	SPT.1 SPT.2	After a voltage transition is complete and during transient load conditions the Source output voltage shall not go beyond the range specified by vSrcValid.
7.1.9#3	SPT.1 SPT.2	The amount of time the Source output voltage can be in the band between vSrcNew and vSrcValid shall not exceed tSrcTransient.
7.1.9#4	NT	The Source output voltage shall be measured at the connector receptacle.
7.1.9#5	BC	The stability of the Source shall be tested in 25% load step increments from minimum load to maximum load and also from maximum load to minimum load.
7.1.9#6	BC	The time between each step shall be sufficient to allow for the output voltage to settle between load steps.
7.4 Electrical Parameters		
7.4.1 Source Electrical Parameters		
7.4.1#17	SPT.3	The most negative voltage allowed during a voltage transition is -0.3 V and called vSrcNeg.
Chapter 8: Device Policy		
8.2 Device Policy Manager		
8.2.5 Managing Power Requirements		
8.2.5#1	SPT.4	The Device Policy Manager in a Provider shall be aware of the power requirements of all devices connected to its Source Ports.
8.2.5.1 Managing the Power Reserve		
8.2.5.1#2	SPT.4	It shall be the Device Policy Manager's responsibility to allocate power and maintain a Power Reserve so as not to over-subscribe its available power resource.
8.2.5.1#3	SPT.4	A Device with multiple ports such as a Hub shall always be able to meet the incremental demands of the Port requiring the highest incremental power from its Power Reserve.

2.2 USB PD 3.0 Assertions

Assertion #	Test Name	Assertion Description
Chapter 6: Protocol Layer		
6.4 Data Message		
6.4.1 Capabilities Message		
6.4.1.2 Source_Capabiltiies Message		
6.4.1.2.1 Management of the Power Reserve		
6.4.1.2.1#1	SPT.4	Where a Power Reserve has been allocated to a Sink the Source shall indicate the Power Reserve as part of every Source_Capabilities Message it sends.
6.4.1.2.1#2	SPT.4	When the same Power Reserve is shared between several Sinks the Source shall indicate the Power Reserve as part of every Source_Capabilities Message it sends to every Sink.
6.4.1.2.1#3	SPT.4	When the Reserve is temporarily used by a GiveBack capable Sink the Source shall indicate the Power Reserve as available in every Source_Capabilities Message it sends.

Assertion #	Test Name	Assertion Description
6.4.1.2.1#4	SPT.4	When the Reserve is temporarily used by a GiveBack capable Sink, when the Power Reserve is requested by another Sink, the Source shall return a Wait Message while it retrieves this power using a GotoMin Message.
6.4.1.2.1#5	SPT.4	Once the additional power has been retrieved the Source shall send a new Source_Capabilities Message in order to trigger a new request from the Sink requesting the Power Reserve.
6.4.1.2.1#6	SPT.4	The Power Reserve may be de-allocated by the Source at any time, but the de-allocation shall be indicated to the Sink or Sinks using the Power Reserve by sending a new Source_Capabilities Message.
6.5 Extended Message		
6.5.10 PPS_Status Message		
6.5.10#1	SPT.6 SPT.7	The PPS_Status Message shall be sent in response to a Get_PPS_Status Message.
6.5.10.3 Real Time Flags Field		
6.5.10.3#2	SPT.6 SPT.7	The OMF (Operating Mode Flag) shall provide a real time indication of the Source's operating mode (constant voltage or current foldback).
Chapter 7: Power Supply		
7.1 Source Requirements		
7.1.3 Types of Sources		
7.1.3#5	BC	The output voltage of the Programmable Power Supply shall remain within a range defined by the relative tolerance vPpsNew and the absolute band vPpsValid.
7.1.4 Source Transitions		
7.1.4.1 Fixed Supply Positive Voltage Transitions		
7.1.4.1#1	BC	The Source shall transition Vbus from the starting voltage to the higher new voltage in a controlled manner.
7.1.4.1#2	BC	During the positive transition the Source shall be able to supply the Sink standby power and the transient current to charge the total bulk capacitance on Vbus.
7.1.4.1#3	SPT.1 SPT.2	The slew rate of the positive transition shall not exceed vSrcSlewPos.
7.1.4.1#4	SPT.1 SPT.2	The transitioning Source output voltage shall settle within vSrcNew by tSrcSettle.
7.1.4.1#5	SPT.1 SPT.2	The source shall be able to supply the negotiated power level at the new voltage by tSrcReady
7.1.4.1#6	SPT.1 SPT.2	The positive voltage transition shall remain monotonic while the transitioning voltage is below vSrcValid min and shall remain within the vSrcValid range upon crossing vSrcValid min.
7.1.4.1#7	SPT.1 SPT.2	At the start of the positive voltage transition the Vbus voltage level Shall Not droop vSrcValid min below either vSrcNew (i.e. if the starting Vbus voltage level is not vSafe5V) or vSafe5V as applicable.
7.1.4.3 Programmable Power Supply Voltage Transitions		
7.1.4.3#1	BC	The Programmable Power Supply (PPS) shall transition Vbus over the defined voltage range in a controlled manner.
7.1.4.3#2	SPT.6	The Output Voltage value in the Programmable RDO defines the nominal value of the PPS output voltage after completing a voltage change and shall settle within the limits defined by vPpsNew by tPpsSrcTransSmall for steps smaller than or equal to vPpsSmallStep, or else, within the limits defined by vPpsNew by tPpsSrcTransLarge.

Assertion #	Test Name	Assertion Description
7.1.4.3#3	SPT.6	Any undershoot or overshoot beyond vPpsNew shall not exceed vPpsValid at any time.
7.1.4.3#4	SPT.6	The PPS output voltage may change in a step-wise or linear manner and the slew rate of either type of change shall not exceed vPpsSlewPos for voltage increases or vPpsSlewNeg for voltage decreases.
7.1.4.3#6	SPT.6	A PPS shall be able to supply the negotiated current level as it changes its output voltage to the requested level.
7.1.4.3#7	SPT.6	All PPS voltage increases shall result in a voltage that is greater than the previous PPS output voltage.
7.1.4.3#8	SPT.6	Likewise, all PPS voltage decreases shall result in a voltage that is less than the previous PPS output voltage.
7.1.4.3#9	SPT.6	For voltage transitions that result in an output voltage step larger than vPpsSmallStep, a PS_RDY message shall be sent within tPpsSrcTransLarge
7.1.4.3#10	SPT.6	For voltage transitions that result in an output voltage step less than or equal to vPpsSmallStep (including, for insance, a large RDO voltage step that resulted in a small output voltage change due to CL mode entered), a PS_RDY message shall be sent within tPpsSrcTransSmall
7.1.4.3#11	SPT.6	If the sink negotiates for a new PPS APDO, then the transition between the two PPS APDOs shall occur as described in Section 7.3.18.
7.1.4.4 Programmable Power Supply Current Foldback		
7.1.4.4#1	SPT.7	The Programmable Power Supply shall limit its output current to the Operating Current value in the Programmable RDO when the sink attempts to draw more current than the Output Current level.
7.1.4.4#2	SPT.7	All programming changes of the Operating Current shall settle to the new Operating Current value within tPpsCLProgramSettle.
7.1.4.4#3	SPT.7	A source that supports PPS shall support Current Limit programmability between iPpsCLMin and the Maximum Current value in the PPS APDO.
7.1.4.4#4	SPT.7	Any current overshoot or undershoot that occurs due to a load change during Current Limit shall not exceed iPpsCLTransient and shall settle to the Operating Current value within tPpsCLSettle.
7.1.4.4#5	SPT.7	Voltage overshoot or undershoot caused by a transition from Current Limit mode to Constant Voltage mode shall not exceed vPpsCLCVTransient and shall settle to the Operating Voltage value within tPpsCLCVTransient.
7.1.4.4#6	SPT.7	Current overshoot or undershoot caused by a transition from Constant Voltage mode to Current Limit mode shall not exceed iPpsCVCLTransient and shall settle to the Operating Current value within tPpsCVCLTransient.
7.1.4.4#7	SPT.7	The PPS source shall maintain its output voltage within the Minimum Voltage and Maximum Voltage values advertised in the PPS aPDO for all static and dynamic load conditions during Current Limit operation.
7.1.4.4#8	SPT.7	If the load condition results in an output voltage that is lower than the Minimum Voltage value advertised in the PPS APDO, the source shall send Hard Reset signaling and discharge Vbus to vSafe0V then resume default operation at vSafe5V.
7.1.4.4#9	SPT.7	When the sink attempts to draw more current than the Operating Current in the RDO, the source shall limit its output current.
7.1.4.4#10	NT	The current available from the source during Current Limit mode shall meet iPpsCLNew plus iPpsCLOperating.
7.1.4.4#11	NT	The source shall not shutdown or otherwise disrupt the available output power while in Current Limit mode unless another protection mechanism as outline in Section 7.1.7 is engaged to protect the source from damage.

Assertion #	Test Name	Assertion Description
7.1.4.4#12	SPT.7	In Figure 7-7, the Current Limit flag shall be set or cleared within the region defined by points a and b.
7.1.4.4#13	SPT.7	In Current Limit mode when the load resistance decreases the output current of the source shall never decrease nor increase more than iPpsCLOperating.
7.1.4.4#14	SPT.7	In Current Limit mode when the load resistance increases the output current of the source shall not increase.
7.1.4.4#15	SPT.7	The amount of allowable increase and decrease Shall Not exceed iPpsCLTolerance relative to a straight line drawn between points b and e as illustrated in Figure 7-8.
7.1.4.4.1 Constant Power Mode		
7.1.4.4.1#1	SPT.7	In Constant Power mode (when the PPS Power Limited bit is set) the Source shall limit its output current so that the product of the output current times the output voltage does not exceed the source's PDP.
7.1.5 Response to Hard Resets		
7.1.5#2	SPT.3	After establishing the vSafe0V voltage condition on Vbus, the Source shall wait tSrcRecover before restoring Vbus to vSafe5V.
7.1.5#5	SPT.3	From the start of the voltage transition, the Source shall meet vSafe5V max within tSafe5V and shall meet vSafe0V within tSafe0V.
7.1.7 Robust Source Operation		
7.1.7.1 Output Over Current Protection		
7.1.7.1#1	SPT.5	Sources shall implement output over current protection to prevent damage from output current that exceeds the current handling capability of the Source.
7.1.7.1#3	SPT.5	The response to over current shall not interfere with the negotiated Vbus current level.
7.1.7.1#4	SPT.5	The Source shall renegotiate with the Sink (or Sinks) after choosing to resume default operation.
7.1.7.1#5	SPT.5	The Source shall prevent continual system or port cycling if over current protection continues to engage after initially resuming either default operation or renegotiation.
7.1.7.1#6	SPT.5	During the over current response and subsequent system or port shutdown, all affected Source ports operating with Vbus greater than vSafe5V shall discharge Vbus to vsSafe5V by the time tSafe5V and vSafe0V by the time tSafe0V.
7.1.7.4 Detach		
7.1.7.4#1	BC	When the Source is Detached the Source shall transition to vSafe0V by tSafe0V relative to when the Detach event occurred.
7.1.8 Output Voltage Tolerance and Range		
7.1.8#1	SPT.1 SPT .2	After a voltage transition is complete (tSrcReady) and during static load conditions the Source output voltage shall remain within the vSrcNew limits.
7.1.8#2	SPT.1 SPT.2	After a voltage transition is complete (tSrcReady) and during transient load conditions the Source output voltage shall not go beyond the range specified by vSrcValid.
7.1.8#3	SPT.1 SPT.2	The amount of time the Source output voltage can be in the band between vSrcNew and vSrcValid shall not exceed tSrcTransient.
7.1.8#5	NT	The Source output voltage shall be measured at the connector receptacle.

Assertion #	Test Name	Assertion Description
7.1.8#6	BC	The stability of the Source shall be tested in 25% load step increments from minimum load to maximum load and also from maximum load to minimum load.
7.1.8#7	BC	The time between each step shall be sufficient to allow for the output voltage to settle between load steps.
7.1.8.1 Programmable Power Supply Output Voltage Tolerance and Range		
7.1.8.1#1	SPT.6	After a voltage transition of a Programmable Power Supply is complete (tPpsSrcTransition) and during static load conditions the Source output voltage shall remain within the vPpsNew limits.
7.1.8.1#2	SPT.6	After a voltage transition is complete (tPpsSrcTransition) and during transient load conditions the Source output voltage shall not go beyond the range specified by vPpsValid.
7.1.8.1#3	SPT.6	The amount of time the Source output voltage can be in the band between vPpsNew and vPpsValid shall not exceed tPpsTransient.
7.3 Transitions		
7.3.18 Change the Source PDO or APDO		
7.3.18#1	BC	The Source voltage as the transition starts shall be any voltage within the Valid Vbus range of the previous Source PDO or APDO
7.3.18#2	BC	The Source voltage after the transition is complete shall be any voltage within the Valid Vbus range of the new Source PDO or APDO
7.3.18#5	NT – under review	The Source transition to the new PDO or APDO Vbus voltage shall be completed by tSrcTransition
7.4 Electrical Parameters		
7.4.1 Source Electrical Parameters		
7.4.1#17	SPT.3	The most negative voltage allowed during a voltage transition is -0.3 V and called vSrcNeg.
Chapter 8: Device Policy		
8.2 Device Policy Manager		
8.2.5 Managing Power Requirements		
8.2.5#1	SPT.4	The Device Policy Manager in a Provider shall be aware of the power requirements of all devices connected to its Source Ports.
8.2.5.1 Managing the Power Reserve		
8.2.5.1#1	SPT.4	It shall be the Device Policy Manager's responsibility to allocate power and maintain a Power Reserve so as not to over-subscribe its available power resource.
8.2.5.1#2	SPT.4	A Device with multiple ports such as a Hub shall always be able to meet the incremental demands of the Port requiring the highest incremental power from its Power Reserve.

2.3 USB Type-C Assertions

Assertion #	Test Name	Assertion Description
Chapter 4: Functional		
4.8 Power Sourcing and Charging		
4.8.6 USB Type-C Multi-Port Chargers		

Assertion #	Test Name	Assertion Description
4.8.6.1 General Requirements		
4.8.6.1#1	SPT.8	Individual source ports shall always comply with power negotiation and rules set forth by the USB Type-C and USB Power Delivery specifications, adjusted as needed when available resources change as other ports take more or less power.
4.8.6.1#2	SPT.8	The minimum capability of all individual USB Type-C ports of a USB Type-C Multi-Port Charger shall be 5V @ 1.5 A independent of how many of the other ports are in use.
4.8.6.1#3	SPT.8	When a USB Type-C Charger includes charging ports that are based on USB Standard-A receptacles, the USB Standard-A ports shall implemented as an independent group, i.e. USB Standard-A ports shall not be included in a group of USB Type-C ports behaving as a Shared Capacity Charger
4.8.6.1#4	SPT.8	When a USB Type-C Charger includes charging ports that are based on USB Standard-A receptacles, the minimum capability of all USB Standard-A ports shall be 5V @ 500 mA independent of how many other ports are in use.
4.8.6.2 Multi-Port Charger Behaviors		
4.8.6.2#1	SPT.1-7	Each Source port of Assured Capacity Chargers shall, by design, behave independently and be unaffected by the status and loading of the other port. (exception of safety due to unexpected behavior on any port)
4.8.6.2#2	SPT.8	For Shared Capacity Groups, each of the exposed Ports shall have the same power capabilities.
4.8.6.2#3	SPT.8	For Shared Capacity Groups, each port of the charger shall be capable of the same maximum capability, minimum capability, and be able to draw from shared power equally.
4.8.6.2#4	SPT.8	For Shared Capacity Groups, all exposed USB PD unattached Source Ports shall have the same power capabilities.
4.8.6.2#5	SPT.8	Ports shall have the ability to supply the available shared capacity power up to the port's maximum power.
4.8.6.2#6	SPT.8	A shared capacity charger's ports may offer less than the port's maximum power, but shall increase the offer up to the maximum power when the Sink sets the Capabilities Mismatch bit in its response. This may be done in multiple steps, but all ports in the Shared Capacity Group shall reach the maximum power within three seconds.
4.8.6.2#7	SPT.8	Whenever a power contract is made or changed on any port, the available shared capacity shall be re-computed and the source shall send updated Source Capability messages as needed.
4.8.6.2#8	SPT.8	As ports of a Shared Capacity Group are connected, each remaining unattached Source Port shall be capable of advertising the lower of the Maximum Capability of the port OR the Total Shared Capacity - the contracted power for the attached ports - (the number of unattached port - 1) * the minimum port power.
4.8.6.2#9	SPT.8	USB PD capable port shall offer at least 7.5W
4.8.6.2#10	SPT.8	When calculating the available shared capacity for ports in a Fixed Supply power contract, the shared capacity charger shall use the Voltage times the Maximum Current in the PDO as the power the port is supplying regardless of the actual Operating Current requested in the RDO request.
4.8.6.2#11	SPT.8	When calculating the available shared capacity for ports in a PPS power contract, the shared capacity charger shall use the Maximum Voltage

Assertion #	Test Name	Assertion Description
		times the Maximum Current in the APDO as the power the port is supplying regardless of the actual voltage and current in the RDO request.
4.8.6.2#12	SPT.8	Ports when not in a PD contract shall follow the rules for a shared USB Type-C Current source unless there is sufficient remaining power for each port to advertise 15W.
4.8.6.2#13	SPT.8	All exposed USB Type-C Current ports shall have the ability to offer the same power capabilities.
4.8.6.2#14	SPT.8	All exposed USB Type-C Current port shall initially offer 1.5A
4.8.6.2#15	SPT.8	USB Type-C Current ports shall increase to 3A after attach if they have sufficient available shared capacity within one second.
4.8.6.2#16	SPT.8	USB Type-C Current ports shall never offer less than 1.5A
4.8.6.3 Multi-Port Charger Port Labeling		
4.8.6.3#1	SPT.8	Multi-port chargers shall have OEM-designed port labeling - For Assured Capacity Chargers, each exposed Source port shall be labeled to indicate the PDP of the port.
4.8.6.3#2	SPT.8	Multi-port chargers shall have OEM-designed port labeling - For Shared Capacity Chargers, each Source port shall be labeled to indicate the same PDP.
4.8.6.3#3	SPT.8	Multi-port chargers shall have OEM-designed port labeling - For Shared Capacity Chargers, the charger shall have a label that, with a minimum of equal visual prominance, indicates the total power delivery capacity being shared across all of the ports identified as a group.
4.8.6.3#4	SPT.8	A Multi-Port Charger that offers in a single product separate groupings of charging ports, each grouping shall be clearly identified as a separate grouping and each grouping shall be individualy labeled consistent with that group's behavior model, either as an Assured Capacity Charger or Shared Capacity Charger.
4.8.6.4 Multi-Port Charger that include USB Data Hub Functionality		
4.8.6.4#1	SPT.8	Multi-Port chargers that also incorporate USB data hub capabilities shall meet the same requirements as standalone chargers.
4.8.6.4#2	SPT.8	Charging-capable hubs shall be self-powered and shall fully operate as a charger independent of the state of the USB data bus connections.
4.8.6.4#3	SPT.8	When the upstream-facing port is sharing capacity with the downstream-facing ports, the PDP of the upstream-facing port can differ from the downstream-facing ports.

3 Tests

At the beginning of each test run, the SPT(s) determines the number of ports to be serviced and records each port's advertised Source Capabilities. It then disconnects from all ports and mirrors its Sink Capabilities to match the DUTs Source Capabilities.

The SPT maximum power draw capability is 100W per port, and 320W cumulative across ports (pMaxSPT). For the duration of the test run, the SPT does not cumulatively draw more than pMaxSPT from the Source, even if a higher current has been negotiated.

Some tests are only applicable if the number of PD source-capable ports on the DUT is greater than 1, or if at least 1 PD source port supports multiple Source Capabilities or APDO Capabilities. Such requirements are noted in the test purpose.

For the duration of the test run, the SPT calculates pMaxDUT, the maximum cumulative power the Source advertises. At the end of the test run, the tester verifies that the reported pMaxDUT is lower than the included Power Supply with the DUT. The DUT fails if its Power Supply advertises lower power output than pMaxDUT.

For PPS tests (SPT 2.6 and 2.7) the SPT assumes that the PPS capable Source is plugged in to Port 1 on the SPT. The SPT records and reports min, max and average voltage and average current for each voltage transition and current transition throughout each test. The SPT collects samples at 50kHz and collects for at least 50ms or at least 10k samples for each transition.

For PPS CL Mode the SPT uses a Constant Resistance (CR) load. Test SPT.7 uses a set load mechanism that calculates the resistance to apply based on V = IR and the new I target.

Note: The Power Delivery Specification defines that Source output voltage shall be measured at the connector receptacle (7.1.9#4). The USB-IF Power Delivery Compliance Committee has decided that for Compliance Testing it is acceptable to use a small cable with a known IR Drop to measure Source voltage. That methodology may be used with this test specification.

SPT.1 Load Test

A. Purpose:
   1. The Load test verifies that when each port is fully loaded at voltage V the Source can still deliver voltage in the tolerance range of vSrcNew or vSafe5V.
   2. This test is required for all USB Type-C source-capable ports.

B. Asserts Covered:

USB PD 2.0	USB PD 3.0
7.1.4#2	7.1.4.1#3
7.1.4#3	7.1.4.1#4
7.1.4#4	7.1.4.1#5
7.1.4#5	7.1.4.1#6
7.1.4#6	7.1.4.1#7
7.1.4#7	7.1.8#1
7.1.4#8	7.1.8#2
7.1.9#1	7.1.8#3
7.1.9#2	
7.1.9#3	

C. Procedure
   1. For each attached port the SPT connects and utilizes a Sink Capability of 5V, 0 A
   2. During each port attach process the SPT verifies:
      a. If the Source voltage initially droops, it shall not fall below vSrcNeg.
      b. After the Source transitions its voltage out of vSafe0V range, its voltage increases monotonically under vSrcSlewPos rate until the voltage passes vSafe5V min.
      c. The Source voltage remains within vSafe5V once it crosses vSafe5V min.
      d. The Source settles into vSafe5V within tSrcSettle from its initial transition out of vSafe0V range.
      e. The remaining attached ports do not droop more than 330mV or for longer than tSrcTransient
   3. For the first port Px with which the SPT establishes a contract:
      a. The SPT requests max current for the next untested Source Capability PDO (let V be the Voltage of this PDO):
         1. The SPT sends a Request for the PDO
         2. The SPT verifies:
            a. If the Source voltage initially droops, it shall not fall below vSafe5VTransition.
            b. After the Source transitions its voltage out of vSafe5V range, its voltage increases monotonically under vSrcSlewPos rate until the voltage passes vSrcValid min.
            c. The Source voltage remains within vSrcValid range once it crosses vSrcValid min.

d. The Source settles into vSrcNew within tSrcSettle from its transition out of vSafe5V range.
e. The remaining attached ports do not droop more than 330mV or for longer than vSrcTransient.

3. After tSrcReady from the initial voltage transition, the SPT enables the max load in 25% increments.
4. The SPT verifies:
    a. If the Source voltage leaves vSrcNew range, it stays within vSrcValid and returns to vSrcNew within tSrcTransient.
    b. The remaining ports do not droop below max (330mV, vSrcNew) or droop for longer than vSrcTransient.

b. If nNumPorts > 1, then for each remaining port Py:
    1. If the port supports PD:
        a. The SPT requests max current for the Source Capability PDO at voltage V.
            i. If the PDO at V does not exist, skip the port and continue with the next port at step C.2.b.1
            ii. The SPT sends a Request for the PDO.
            iii. The SPT verifies:
                1. If the Source voltage initially droops, it shall not fall below vSafe5VTransition.
                2. After the Source transitions its voltage out of vSafe5V range, its voltage increases monotonically under vSrcSlewPos rate until the voltage passes vSrcValid min.
                3. The Source voltage remains within vSrcValid range once it crosses vSrcValid min.
                4. The Source settles into vSrcNew within tSrcSettle from its transition out of vSafe5V range.
                5. The remaining attached ports do not droop more than max (330mV, vSrcNew) or for longer than tSrcTransient.
            iv. After tSrcReady from the initial voltage transition, the SPT enables the max load in 25% increments.
            v. The SPT verifies:
                1. If the Source voltage leaves the vSrcNew range, it stays within vSrcValid and settles to vSrcNew within tSrcTransient.
                2. The remaining ports do not droop below max (330mV, vSrcNew) or droop for longer than tSrcTransient.

2. If the port does not support PD the SPT loads the max current advertised on Rp.
    a. The SPT verifies:
        i. The Source voltage does not droop more than 330mV or for longer than tSrcTransient.

        ii. The remaining ports do not droop below max (330mV, vSrcNew) or droop for longer than tSrcTransient.
3. Move to step C.2.b.1 for the next remaining port.

c. For each port Py loaded in step C.2.b.
    1. The SPT disables the load in 25% increments.
    2. The SPT verifies:
        a. If the Source voltage leaves the vSrcNew range, it stays within vSrcValid and settles to vSrcNew within tSrcTransient.
        b. The remaining ports do not leave vSafe5V or vSrcNew range.
    3. Move to step C.2.c for the next loaded port.
d. For port Px loaded in step C.2.a:
    1. The SPT disables the load in 25% increments.
    2. The SPT verifies:
        a. If the Source voltage leaves the vSrcNew range, it stays within vSrcValid and settles to vSrcNew within tSrcTransient.
        b. The remaining ports do not leave vSafe5V or vSrcNew range.
e. If the Source Capability PDO (at voltage V) on Port Px advertised peak current capability, return to step C.2.a.1, Request the PDO again and step through the test while utilizing the peak current with operating current at 2/3 max current advertised on Port Px.
f. Move to step C.2 to test the next Source Capability PDO.

4. If no port supports USB PD:
    a. For each port Px:
        1. The SPT loads the max current advertised on Rp.
        2. The SPT verifies:
            a. If the Source voltage does not droop or drop below 330mV or for longer than tSrcTransient.
            b. The remaining ports do not droop more than 330mV during the transient load on the port Px or for longer than tSrcTransient.

SPT.2 Capabilities Test

A. Purpose:
   1. The Capabilities Test verifies that each port can simultaneously provide a different advertised voltage.
   2. This test is required for MultiPort products with at least one PD port that supports more than one Source Capability.

B. Asserts Covered:

USB PD 2.0	USB PD 3.0
7.1.4#2	7.1.4.1#3
7.1.4#3	7.1.4.1#4
7.1.4#5	7.1.4.1#5
7.1.4#6	7.1.4.1#6
7.1.4#7	7.1.4.1#7
7.1.9#1	7.1.8#1
7.1.9#2	7.1.8#2
7.1.9#3	7.1.8#3

C. Test Procedure:
   1. For each attached port the SPT connects and utilizes a Sink Capability of 5V, 0A.
   2. For the first port Px with which the SPT establishes a contract:
      a. Let y = 1
      b. Request the max current for the highest voltage Source Capability PDO (let the voltage be Xy)
      c. The SPT verifies:
         1. If the Source voltage initially droops, it shall not fall below vSafe5VTransition.
         2. After the Source transitions its voltage out of vSafe5V range, its voltage increases monotonically under vSrcSlewPos rate until the voltage passes vSrcValid min.
         3. The Source voltage remains within vSrcValid range once it crosses vSrcValid min.
         4. The Source settles into vSrcNew within tSrcSettle from its transition out of vSafe5V range.
         5. The remaining ports do not droop more than max(330mV, vSrcNew) or for longer than tSrcTransient.
      d. After tSrcReady from the initial voltage transition, the SPT enables the max load in 25% increments.
      e. The SPT verifies:
         1. If the Source voltage leaves the vSrcNew range, it stays within vSrcValid and settles to vSrcNew within tSrcTransient.
         2. The remaining ports do not droop more than max(330mV, vSrcNew) or for longer than tSrcTransient

f. If the number of USB PD capable ports is greater than 1, then for each remaining USB PD capable ports Px:
    1. Let y += 1
    2. The SPT Requests the max current for the highest voltage Source Capability PDO besides the PDOs with voltages in the set {V1, …, Vy}. (Let this voltage be V(y+1))
    3. If the DUT only has the voltage capabilities included in the set {V1,…,Vy} and vSafe5V, the SPT sends a Request for the Source Capability PDO with voltage V1.
    4. The SPT Verifies:
        a. If the Source voltage initially droops, it shall not fall below vSafe5VTransition.
        b. After the Source transitions its voltage out of vSafe5V range, its voltage increases monotonically under vSrcSlewPos rate until the voltage passes vSrcValid min.
        c. The Source voltage remains within vSrcValid range once it crosses vSrcValid min.
        d. The Source settles into vSrcNew within tSrcSettle from its transition out of vSafe5V range.
        e. The remaining ports do not droop below max (330mV, vSrcNew) or for longer than tSrcTransient.
    5. After tSrcReady from the initial voltage transition, the SPT enables the max load in 25% increments.
    6. The SPT verifies:
        a. If the Source voltage leaves the vSrcNew range, it stays within vSrcValid and settles to vSrcNew within tSrcTransient.
        b. The remaining ports do not droop below max (330mV, vSrcNew) or for longer than tSrcTransient.

SPT.3 Hard Reset Test

A. Purpose:
    1. The Hard Reset Test verifies that the PD Source port follows the voltage requirements for a PD Hard Reset.
    2. This test is required for any PD source-capable port.

B. Asserts Covered:

USB PD 2.0	USB PD 3.0
7.1.6#1	7.1.5#2
7.1.6#4	7.1.5#5
7.4.1#17	7.4.1#17

C. Test Procedure:
    1. The SPT attaches all ports and utilizes a Sink Capability of 5V, 0A.
    2. For each port with which the SPT establishes a PD contract:
        a. Request the max current for the highest voltage Source Capability PDO.
        b. The SPT verifies the PD request is accepted and a contract is established.
        c. The SPT applies the max load in 25% increments.
        d. The SPT sends a Hard Reset.
        e. The SPT verifies that from the start of the Source voltage transition:
            1. The Source voltage drops to vSafe5V within tSafe5V
            2. The Source voltage drops to vSafe0V within tSafe0V
        f. The SPT disables the load on the port.
        g. The SPT verifies:
            1. The Source voltage remains within vSafe0V for tSrcRecover
            2. The Source voltage does not dip below vSrcNeg for the duration of the Hard Reset.

SPT.4 GiveBack Test

A. Purpose:
   1. The GiveBack Test verifies that a DUTs Power Reserve is managed correctly
   2. This test is required for MultiPort products with multiple PD capable ports.

B. Asserts Covered:

USB PD 2.0	USB PD 3.0
6.4.1.2.1#1	6.4.1.2.1#1
6.4.1.2.1#2	6.4.1.2.1#2
6.4.1.2.1#3	6.4.1.2.1#3
6.4.1.2.1#4	6.4.1.2.1#4
6.4.1.2.1#5	6.4.1.2.1#5
6.4.1.2.1#6	6.4.1.2.1#6
8.2.5#1	8.2.5#1
8.2.5.1#2	8.2.5.1#2
8.2.5.1#3	8.2.5.1#3

C. Test Procedure:
   1. The SPT connects all attached ports and utilizes a Sink Capability of 5V, 0A.
   2. The SPT records the Source_Capability PDO voltage and current advertised for each port.
   3. For the first port with PD enabled (with which the SPT has established a contract):
      a. The SPT verifies that the Source_Capabilities returned match the PDOs for the port recorded in step C.2.
      b. The SPT Requests the highest voltage Source Capability PDO with:
         1. GiveBack flag set
         2. Min Operating Current set to 0
         3. Operating Current set to advertised Max Current for the PDO
      c. The SPT verifies that the contract is established.
      d. If the contract is accepted without GoToMin message:
         1. The SPT enables the max load in 25% increments.
         2. Continue to step C.3 for the next port with PD enabled.
      e. Else if a GoToMin message is received as part of the contract:
         1. Let the port be called Px
         2. The SPT Requests the highest voltage Source Capability PDO with:
            a. Operating Current and Max Current set to advertised Max Current
   4. The SPT verifies that:
      a. The DUT sends a Wait message to Px.
      b. The DUT sends GoToMin to one of the loaded ports. Let the port be called Py.
   5. The SPT transitions to min current on port Py.
   6. The SPT verifies:
      a. The DUT sends a PS_RDY to port Py.

b. The DUT sends a Source_Capabilities to port Px with the same PDOs.

7. The SPT requests the same max PDO on port Px.
8. The SPT verifies it establishes a contract for the PDO with the DUT on port Px.
9. The SPT enables the load requested in the PDO in 25% increments.
10. Wait 1 second.
11. The SPT disables the load requested in the PDO in 25% increments.
12. The SPT Requests an RDO at the same voltage but with 0 operating and max current.
13. The SPT verifies:
    a. It establishes a contract for the RDO with the DUT on port Px.
    b. The DUT sends a Source_Capabilities to port Py advertising the same PDOs.

SPT.5 Over Current Test

A. Purpose:
   1. The Over Current Test verifies that the PD Source port follows the overcurrent requirements.
   2. This test is required for any PD source-capable port.

B. Asserts Covered:

USB PD 2.0	USB PD 3.0
7.1.8.3#1	7.1.7.1#1
7.1.8.3#2	7.1.7.1#3
	7.1.7.1#4
	7.1.7.1#5
	7.1.7.1#6

C. Test Procedure:
   1. The SPT verifies that VIF field PD_OC_Protection is YES.
   2. If PD_OC_Protection is NO, skip the remainder of the test.
   3. The SPT attaches all ports and utilizes a Sink Capability of 5V, 0A.
   4. For each port with which the SPT establishes a PD contract:
      a. The SPT requests the max current for the negotiated source PDO
      b. The SPT applies the negotiated current load to the port in 25% increments
      c. The SPT increases the load by 100mA
      d. If the PDO drops to vSafe0V after this step, the SPT verifies that once Vbus starts the transition to vSafe0V:
         1. If the output voltage was higher than vSafe5V, it enters vSafe5V within tSafe5V
         2. The output voltage enters vSafe0V within tSafe0V
      e. Else if the load =< 5.5A, Repeat step C.4.c.
      f. If the load is > 5.5A and OCP has not triggered, the test fails.
      g. Disable the load
      h. The SPT informs the user of the value at which the over current condition triggered or the maximum current applied if it did not trigger.
      i. Repeat step C.4.a for the next advertised Source Capability PDO until no more exist

SPT.6 PPS Voltage Step Test

A. Purpose:
   1. The PPS Step Test verifies that when a source port makes a contract using an APDO its output follows the monotonicity and tolerance requirements from USB PD spec section 7.1.4.3.
   2. This test is required for all USB PD ports that advertise APDO capabilities.
   3. This is a single port test at this time.
   4. This is a USB PD 3.0 test only.

B. Asserts Covered:

USB PD 2.0	USB PD 3.0
	6.5.10#1
	6.5.10.3#2
	7.1.4.3#2
	7.1.4.3#3
	7.1.4.3#4
	7.1.4.3#6
	7.1.4.3#7
	7.1.4.3#8
	7.1.4.3#9
	7.1.4.3#10
	7.1.4.3#11
	7.1.4.3#12
	7.1.8#1
	7.1.8#2
	7.1.8#3

C. Step Size Conditions:
   1. 20mV
   2. 100mV
   3. 500mV

D. Operating Current Conditions:
   1. 1 A
   2. APDO Maximum Current / 2 + 500 mA
   3. APDO Maximum Current

E. Procedure
   1. The SPT connects its source terms and negotiates a default 5V contract.
   2. For each APDO capability advertised on the PUT:
      a. Set Icurr = the first Operating Current Condition from section D above.
      b. Set APDOcurr = the APDO source capability index
      c. Set Vmin = the APDO Minimum Operating Voltage
      d. Set Vmax = the APDO Maximum Operating Voltage
      e. The SPT sends a Request Message RDO [index: APDOcurr, voltage: Vmin, current: Icurr].

f. The SPT verifies:
    1. The source voltage was initially within vSafe5V or if transitioning from another APDO, within the range of its previous APDO contract
    2. The source voltage settles within tPpsSrcTransition to within vPpsNew
g. The SPT sets its load to 80% of Icurr
h. The SPT verifies that if the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.
i. The SPT sends a Get_PPS_Status message to the PUT.
j. The SPT verifies the PUT responds with OMF flag cleared.
k. For each Step Size Condition, Vstep, listed in C above:
    1. Let the last requested RDO Voltage be Vcurr. While Vcurr ≤ Vmax – Vstep:
        a. SPT sends a Request Message RDO [index: APDOcurr, voltage: Vnew = Vcurr + Vstep, current: Icurr].
        b. SPT verifies:
            i. The source settles to within vPPsNew by vPpsSrcTransition.
            ii. The source voltage remains within vPpsValid for the duration of the transition
            iii. The source voltage transition rate remains within vPpsSlewPos
            iv. The measured current level doesn't exceed its operating current
            v. After settling, the source voltage has increased at least 8mV compared to its value before the voltage transition.
        c. Set Vcurr = Vnew
    2. SPT sends a Request Message RDO [index: APDOcurr, voltage: Vmax, current: Icurr].
    3. SPT verifies:
        a. The source settles to within vPPsNew by vPpsSrcTransition.
        b. The source voltage remains within vPpsValid for the duration of the transition
        c. The source voltage transition rate remains within vPpsSlewPos
        d. Current level remains in its negotiated range for the duration of the transition
        e. After settling, the source voltage has increased at least 8 mV compared to its value before the voltage transition.
    4. The SPT sends a Get_PPS_Status message to the PUT.
    5. The SPT verifies the PUT responds with OMF flag cleared.
    6. Let the last requested RDO Voltage be Vcurr. While Vcurr ≥ Vmin + Vstep:
        a. SPT sends a Request Message RDO [index: APDOcurr, voltage: Vnew = Vcurr – STEPcurr, current: Icurr].
        b. SPT verifies:

i. The source settles to within vPPsNew by vPpsSrcTransition.
ii. The source voltage remains within vPpsValid for the duration of the transition
iii. The source voltage transition rate remains within vPpsSlewNeg
iv. Current level remains in its negotiated range for the duration of the transition
v. After settling, the source voltage has decreased at least 8 mV compared to its value before the voltage transition.

c. Set Vcurr = Vnew

7. SPT sends a Request Message RDO [index: APDOcurr, voltage: Vmin, current: Icurr]
8. SPT verifies:
   a. The source settles to within vPPsNew by vPpsSrcTransition.
   b. The source voltage remains within vPpsValid for the duration of the transition
   c. The source voltage transition rate remains within vPpsSlewNeg
   d. Current level remains in its negotiated range for the duration of the transition
   e. After settling, the source voltage has decreased at least 8 mV compared to its value before the voltage transition.

l. The SPT sends a Get_PPS_Status message to the PUT.

m. The SPT verifies the PUT responds with OMF flag cleared.

n. If Icurr is the APDO Maximum Current:
   1. The SPT sets its load to 0 and waits tPpsTransient.
   2. The SPT sets its load to Icurr
   3. The SPT verifies that if the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.
   4. The SPT sends a Request Message RDO [index: APDOcurr, voltage: Vmax, current: Icurr]
   5. SPT verifies:
      a. The source settles to within vPPsNew by vPpsSrcTransition.
      b. The source voltage remains within vPpsValid for the duration of the transition
      c. The source voltage transition rate remains with vPpsSlewPos
      d. Current level remains in its negotiated range for the duration of the transition
      e. After settling, the source voltage has increased at least 8 mV compared to its value before the voltage transition
   6. The SPT sets its load to 0.
   7. The SPT verifies that if the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.

8. The SPT sets its load to Icurr.
9. The SPT verifies that if the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.
10. The SPT sends a Request Message RDO [index: APDOcurr, voltage: Vmin, current: Icurr]
11. SPT verifies:
    a. The source settles to within vPPsNew by vPpsSrcTransition.
    b. The source voltage remains within vPpsValid for the duration of the transition
    c. The source voltage transition rate remains with vPpsSlewNeg
    d. Current level remains in its negotiated range for the duration of the transition
    e. After settling, the source voltage has decreased at least 8 mV compared to its value before the voltage transition

o. The SPT disables its load.
p. The SPT verifies that if the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.
q. Set Icurr = the next Operating Current Condition from section D above. The test is over if all Operating Current Conditions are exhausted or if the APDO Maximum Current is 1 A.
r. Continue to step E.2.b

SPT.7 PPS Current Limit Test

A. Purpose:
    1. The PPS Current Foldback Test verifies that when a source port makes a contract using an APDO and current reaches Operating Current level, its output follows the tolerance requirements from USB PD spec section 7.1.4.4.
    2. This test is required for all USB PD ports which source APDO capabilities.
    3. This is a single port test at this time.
    4. This is a USB PD 3.0 test only.

B. Asserts Covered:

USB PD 2.0	USB PD 3.0
	6.5.10#1
	6.5.10.3#2
	7.1.4.4#1
	7.1.4.4#2
	7.1.4.4#3
	7.1.4.4#4
	7.1.4.4#5
	7.1.4.4#6
	7.1.4.4#7
	7.1.4.4#8
	7.1.4.4#9
	7.1.4.4#12
	7.1.4.4#13
	7.1.4.4#14
	7.1.4.4#15

C. Operating Current Conditions:
    1. 1 A
    2. (Current APDO Max Current / 2) + 500 mA
    3. Current APDO Max Current

D. Operating Voltage Conditions:
    1. APDO Min Voltage
    2. (APDO Min Voltage + APDO Max Voltage) / 2
    3. APDO Max Voltage

E. Current Step Conditions:
    1. 500 mA
    2. 100 mA
    3. 50 mA

F. Procedure
    1. The SPT connects its source terms and negotiates a default 5V contract.
    2. Set APDOcurr to the first APDO capability advertised on the PUT.
    3. Set Vcurr = the first Operating Voltage Condition from D above.

4. Set Icurr = the first Operating Current Condition from C above.
5. For each Istep in Current Steps from Condition E above:
    a. Set Vlow[Istep_index] = 0. This will be the voltage reached before a Hard Reset occurs for the source
    b. The SPT sends a Request Message RDO [index: APDOcurr, voltage: Vcurr, current: Icurr].
    c. The SPT verifies the source voltage settles to within vPpsNew by tSrcReady or if transitioning from another APDO, by tPpsSrcTransSmall or tPpsSrcTransLarge as applicable.
    d. The SPT sets the load, Lcurr = Icurr
    e. The SPT sets the load, Lcurr = Icurr – 350 mA when Istep == 500 mA and Lcurr = Icurr – 250 mA when Istep == 50 mA or 100 mA.
    f. If the SPT receives a Hard Reset, the test fails and SPT continues to step 5 with Vcurr = Vcurr + 100 mV
    g. Set Vlow[Icurr_index] = SPT measured Vbus voltage
    h. SPT verifies that if there is no Hard Reset signaling, measured Vbus voltage is within APDO miniminum voltage range to APDO maximum voltage range.
    i. The SPT sets the load, Lcurr = Lcurr + Istep
    j. If the SPT receives a Hard Reset:
        1. The SPT verifies the source drops voltage to vSafe0V and resumes to vSafe5V.
        2. The SPT continues to step 5 with the next Istep
    k. If the SPT measured Vbus voltage < APDO minimum voltage * 1.05 (max), and Istep is the smallest step from Condition E above, and the “e” point has not been determined, then record this as “e” point (from Figure 7-8).
    l. The SPT continues to step 5.g
6. For each Istep in Current Steps from Condition E above:
    a. The SPT sends a Request Message RDO [index: APDOcurr, voltage: Vcurr, current: Icurr].
    b. While SPT measured source output voltage is greater than Vlow[Istep_index]:
        1. The SPT sets its load, Lcurr = Lcurr + Istep
        2. Set Lcurr = SPT measured Vbus current (due to CR load this may be different than target Lcurr)
        3. Set Vspt = SPT measured Vbus voltage (adjusts for cable drop to measure TP1)
        4. If Lcurr < iPpsCLNew minimum:
            a. The SPT verifies that if the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.
            b. SPT sends Get_PPS_Status to PUT
            c. SPT verifies PUT responds with OMF flag cleared
        5. If Lcurr > iPpsCLNew minimum and Vspt > vPpsNew minimum:
            a. The SPT records this transition as Tcurr
            b. SPT sends Get_PPS_Status

c. If the PUT responds with OMF flag cleared, and the previous response had OMF flag clear, the SPT verifies for Tcurr that if the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.
d. If the PUT responds with OMF flag set, and previous response had OMF flag cleared, the SPT verifies for Tcurr:
    i. If current leaves iPpsCLNew range during the CV to CL transition, it does not exceed iPpsCVCLTransient
    ii. Current settles to iPpsCLNew within tPpsCVCLTransient after the transition
e. If the PUT responds with OMF flag set, and the previous response had OMF flag set, the SPT verifies for Tcurr that the output current stays within iPpsCLTransient and settles to the Operating Current value within tPpsCLSettle.
f. If the PUT responds with OMF flag cleared, and the previous response had OMF flag set, the SPT verifies for Tcurr:
    i. If voltage leaves Operating Voltage range during the CL to CV transition, it does not exceed vPpsCLCVTransient
    ii. Voltage settles to Operating Current within tPpsCLCVTransient after the transition

6. If Vspt < vPpsNew minimum:
    a. If the PUT responded to the previous Get_PPS_Status with the OMF flag cleared, the SPT verifies:
        i. If current leaves Operating Current range during the CV to CF transition, it does not exceed iPpsCVCLTransient
        ii. Current settles to Operating Current within tPpsCVCLTransient after the transition
    b. If the PUT responded to the previous Get_PPS_Status with the OMF flag set, the PPS verifies that the output current stays within iPpsCLTransient and settles to the Operating Current value within tPpsCLSettle.
    c. SPT sends Get_PPS_Status to PUT
    d. SPT verifies PUT responds with OMF flag set
    e. If “b” point is not yet set, record this as “b” point (from Figure 7-8). SPT verifies PUT current remains within iPpsCLTolerance using the load line made between the points “b” and “e”, and using Vspt determined above.
        i. SPT verifies Lcurr does not breach iPpsCLTolerance high
        ii. SPT verifies Lcurr does not breach iPpsCLTolerance low
7. The SPT verifies it did not enter step 6.b.4 and step 6.b.6 since step 6.b

c. While Lcurr > 80% of the negotiated Operating Current:
    1. The SPT sets its load, Lcurr = Lcurr – Istep
    2. Set Lcurr = SPT measured Vbus current

3. Set Vspt = SPT measured Vbus voltage
4. If Vspt < vPpsNew minimum:
    a. The SPT verifies the output current stays within iPpsCLTransient and settles to the Operating Current value within tPpsCLSettle.
    b. SPT sends Get_PPS_Status to PUT
    c. SPT verifies PUT responds with OMF flag set
    d. SPT verifies PUT current remains within iPpsCLTolerance using the load line made between the points “b” and “e”, and using Vspt determined above.
        i. SPT verifies Lcurr does not breach iPpsCLTolerance high
        ii. SPT verifies Lcurr does not breach iPpsCLTolerance low
5. If Lcurr > iPpsCLNew minimum and Vspt > vPpsNew minimum:
    a. The SPT records this transition as Tcurr
    b. SPT sends Get_PPS_Status
    c. If the PUT responds with OMF flag set, and the previous response had OMF flag set, the SPT verifies for Tcurr that the output current stays within iPpsCLTransient and settles to the Operating Current value within tPpsCLSettle.
    d. If the PUT responds with OMF flag cleared, and the previous response had OMF flag set, the SPT verifies for Tcurr:
        i. If voltage leaves Operating Voltage range during the CF to CV transition, it does not exceed vPpsCLCVTransient
        ii. Voltage settles to Operating Voltage within tPpsCLCVTransient after the transition
    e. If the PUT responds with OMF flag set, and the previous response had OMF flag cleared, the SPT verifies for Tcurr:
        i. If current leaves Operating Current range during the CV to CF transition, it does not exceed iPpsCVCLTransient
        ii. Current settles to Operating Current within tPpsCVCLTransient after the transition
    f. If the PUT responds with OMF flag cleared, and the previous response had OMF flag cleared, the SPT verifies for Tcurr:
        i. If the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.
6. If Lcurr < iPpsCLNew minimum:
    a. If the PUT responded to the previous Get_PPS_Status with the OMF flag cleared, the SPT verifies that if the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.
    b. If the PUT responded to the previous Get_PPS_Status with the OMF flag set, the SPT verifies:
        i. If current leaves Operating Current range during the CV to CF transition, it does not exceed iPpsCVCLTransient

ii. Current settles to Operating Current within tPpsCVCLTransient after the transition

c. SPT sends Get_PPS_Status to PUT

d. SPT verifies PUT responds with OMF flag cleared

7. The SPT verifies it did not enter step 6.c.4 and step 6.c.6 since step 6.c

d. If Vcurr =! APDO min voltage, then SPT continues to step 6.h

e. Set Vnew = Vcurr

f. While Vnew < APDO Max Voltage:

1. Vnew = Vnew + 500 mV
2. The SPT sends RDO Request [index: APDOcurr, voltage: Vnew, current: Icurr].
3. Set Lcurr = SPT measured Vbus current
4. Set Vspt = SPT measured Vbus voltage
5. If Lcurr < iPpsCLNew minimum:
    a. SPT verifies:
        i. The source settles to within vPPsNew by vPpsSrcTransition.
        ii. The source voltage remains within vPpsValid for the duration of the transition
        iii. The source voltage transition rate remains within vPpsSlewPos
        iv. Current level remains in its negotiated range for the duration of the transition
        v. After settling, the source voltage has increased compared to its value before the voltage transition.
    b. SPT sends Get_PPS_Status to PUT
    c. SPT verifies PUT responds with OMF flag cleared
6. If Lcurr > iPpsCLNew minimum and Vspt > vPpsNew minimum:
    a. The SPT records this transition as Tcurr
    b. SPT sends Get_PPS_Status
    c. If the PUT responds with OMF flag cleared, and the previous response had OMF flag clear, the SPT verifies for Tcurr:
        i. The source settles to within vPPsNew by vPpsSrcTransition.
        ii. The source voltage remains within vPpsValid for the duration of the transition
        iii. The source voltage transition rate remains within vPpsSlewPos
        iv. Current level remains in its negotiated range for the duration of the transition
        v. After settling, the source voltage has increased compared to its value before the voltage transition.
    d. If the PUT responds with OMF flag set, and previous response had OMF flag cleared, the SPT verifies for Tcurr:

i. If current leaves Operating Current range during the CV to CL transition, it does not exceed iPpsCVCLTransient
ii. Current settles to Operating Current within tPpsCVCLTransient after the transition

e. If the PUT responds with OMF flag set, and the previous response had OMF flag set, the SPT verifies for Tcurr that the output current stays within iPpsCLTransient and settles to the Operating Current value within tPpsCLSettle.
f. If the PUT responds with OMF flag cleared, and the previous response had OMF flag set, the SPT verifies for Tcurr:
i. If voltage leaves Operating Voltage range during the CL to CV transition, it does not exceed vPpsCLCVTransient
ii. Voltage settles to Operating Current within tPpsCLCVTransient after the transition

7. If Vspt < vPpsNew minimum:
a. If the PUT responded to the previous Get_PPS_Status with the OMF flag cleared, the SPT verifies:
i. If current leaves Operating Current range during the CV to CF transition, it does not exceed iPpsCVCLTransient
ii. Current settles to Operating Current within tPpsCVCLTransient after the transition
b. If the PUT responded to the previous Get_PPS_Status with the OMF flag set, the PPS verifies that the output current stays within iPpsCLTransient and settles to the Operating Current value within tPpsCLSettle.
c. SPT sends Get_PPS_Status to PUT
d. SPT verifies PUT responds with OMF flag set
8. The SPT verifies it did not enter step 6.f.4 and step 6.f.6 since step 6.f

g. While Vnew > Vcurr:
1. Vnew = Vnew – 500 mV
2. The SPT sends RDO Request [index: APDOcurr, voltage: Vnew, current: Icurr].
3. Set Lcurr = SPT measured Vbus current
4. Set Vspt = SPT measured Vbus voltage
5. If Vspt < vPpsNew minimum:
a. The SPT verifies the output current stays within iPpsCLTransient and settles to the Operating Current value within tPpsCLSettle.
b. SPT sends Get_PPS_Status to PUT
c. SPT verifies PUT responds with OMF flag set
6. If Lcurr > iPpsCLNew minimum and Vspt > vPpsNew minimum:
a. The SPT records this transition as Tcurr
b. SPT sends Get_PPS_Status

c. If the PUT responds with OMF flag set, and the previous response had OMF flag set, the SPT verifies for Tcurr:
    i. SPT measured output current stays within iPpsCLTransient and settles to the Operating Current value within tPpsCLSettle.
    ii. Voltage does not exceed vPpsNew or vPpsValid for longer than tPpsTransient
d. If the PUT responds with OMF flag cleared, and the previous response had OMF flag set, the SPT verifies for Tcurr:
    i. If voltage leaves Operating Voltage range during the CF to CV transition, it does not exceed vPpsCLCVTransient
    ii. Voltage settles to Operating Voltage within tPpsCLCVTransient after the transition
e. If the PUT responds with OMF flag set, and the previous response had OMF flag cleared, the SPT verifies for Tcurr:
    i. If current leaves Operating Current range during the CV to CF transition, it does not exceed iPpsCVCLTransient
    ii. Current settles to Operating Current within tPpsCVCLTransient after the transition
    iii. Voltage does not exceed vPpsNew or vPpsValid for longer than tPpsTransient
f. If the PUT responds with OMF flag cleared, and the previous response had OMF flag cleared, the SPT verifies for Tcurr:
    i. The source settles to within vPPsNew by vPpsSrcTransition.
    ii. The source voltage remains within vPpsValid for the duration of the transition
    iii. The source voltage transition rate remains within vPpsSlewPos
    iv. Current level remains in its negotiated range for the duration of the transition
    v. After settling, the source voltage has increased compared to its value before the voltage transition.

7. If Lcurr < iPpsCLNew minimum:
    a. If the PUT responded to the previous Get_PPS_Status with the OMF flag cleared, the SPT verifies:
        i. The source settles to within vPPsNew by vPpsSrcTransition.
        ii. The source voltage remains within vPpsValid for the duration of the transition
        iii. The source voltage transition rate remains within vPpsSlewPos
        iv. Current level remains in its negotiated range for the duration of the transition

v. After settling, the source voltage has increased compared to its value before the voltage transition.

b. If the PUT responded to the previous Get_PPS_Status with the OMF flag set, the SPT verifies:
   i. If current leaves Operating Current range during the CV to CF transition, it does not exceed iPpsCVCLTransient
   ii. Current settles to Operating Current within tPpsCVCLTransient after the transition

c. SPT sends Get_PPS_Status to PUT

d. SPT verifies PUT responds with OMF flag cleared

8. The SPT verifies it did not enter step 6.g.4 and step 6.g.6 since step 6.g

h. If Icurr != APDO Maximum Current, then SPT continues to step 7

i. Set Inew = Icurr

j. While SPT measured source output voltage is greater than Vlow[Istep_index]:
   1. Inew = Inew – 500 mA
   2. The SPT sends RDO Request [index: APDOcurr, voltage: Vcurr, current: Inew].
   3. Set Lcurr = SPT measured Vbus current
   4. Set Vspt = SPT measured Vbus voltage
   5. If Lcurr < iPpsCLNew minimum:
      a. The SPT verifies that if the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.
      b. SPT sends Get_PPS_Status to PUT
      c. SPT verifies PUT responds with OMF flag cleared
   6. If Lcurr > iPpsCLNew minimum and Vspt > vPpsNew minimum:
      a. The SPT records this transition as Tcurr
      b. SPT sends Get_PPS_Status
      c. If the PUT responds with OMF flag cleared, and the previous response had OMF flag clear, the SPT verifies for Tcurr that if the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.
      d. If the PUT responds with OMF flag set, and previous response had OMF flag cleared, the SPT verifies for Tcurr:
         i. If current leaves Operating Current range during the CV to CL transition, it does not exceed iPpsCVCLTransient
         ii. Current settles to Operating Current within tPpsCVCLTransient after the transition
      e. If the PUT responds with OMF flag set, and the previous response had OMF flag set, the SPT verifies for Tcurr that the output current stays within iPpsCLTransient and settles to the Operating Current value within tPpsCLSettle.
      f. If the PUT responds with OMF flag cleared, and the previous response had OMF flag set, the SPT verifies for Tcurr:

i. If voltage leaves Operating Voltage range during the CL to CV transition, it does not exceed vPpsCLCVTransient
ii. Voltage settles to Operating Current within tPpsCLCVTransient after the transition

7. If Vspt < vPpsNew minimum:
    a. If the PUT responded to the previous Get_PPS_Status with the OMF flag cleared, the SPT verifies:
        i. If current leaves Operating Current range during the CV to CF transition, it does not exceed iPpsCVCLTransient
        ii. Current settles to Operating Current within tPpsCVCLTransient after the transition
    b. If the PUT responded to the previous Get_PPS_Status with the OMF flag set, the PPS verifies that the output current stays within iPpsCLTransient and settles to the Operating Current value within tPpsCLSettle.
    c. SPT sends Get_PPS_Status to PUT
    d. SPT verifies PUT responds with OMF flag set
8. The SPT verifies it did not enter step 6.j.4 and step 6.j.6 since step 6.j

k. While Inew < Icurr:
    1. Inew = Inew + 500 mV
    2. The SPT sends RDO Request [index: APDOcurr, voltage: Vcurr, current: Inew].
    3. Set Lcurr = SPT measured Vbus current
    4. Set Vspt = SPT measured Vbus voltage
    5. If Vspt > vPpsNew minimum:
        a. The SPT verifies the output current stays within iPpsCLTransient and settles to the Operating Current value within tPpsCLSettle.
        b. SPT sends Get_PPS_Status to PUT
        c. SPT verifies PUT responds with OMF flag set
    6. If Lcurr > iPpsCLNew minimum and Vspt > vPpsNew minimum:
        a. The SPT records this transition as Tcurr
        b. SPT sends Get_PPS_Status
        c. If the PUT responds with OMF flag set, and the previous response had OMF flag set, the SPT verifies for Tcurr that the output current stays within iPpsCLTransient and settles to the Operating Current value within tPpsCLSettle.
        d. If the PUT responds with OMF flag cleared, and the previous response had OMF flag set, the SPT verifies for Tcurr:
            i. If voltage leaves Operating Voltage range during the CF to CV transition, it does not exceed vPpsCLCVTransient
            ii. Voltage settles to Operating Voltage within tPpsCLCVTransient after the transition

e. If the PUT responds with OMF flag set, and the previous response had OMF flag cleared, the SPT verifies for Tcurr:
    i. If current leaves Operating Current range during the CV to CF transition, it does not exceed iPpsCVCLTransient
    ii. Current settles to Operating Current within tPpsCVCLTransient after the transition
f. If the PUT responds with OMF flag cleared, and the previous response had OMF flag cleared, the SPT verifies for Tcurr:
    i. If the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.

7. If Lcurr < iPpsCLNew minimum:
    a. If the PUT responded to the previous Get_PPS_Status with the OMF flag cleared, the SPT verifies that if the source leaves vPpsNew range, it stays within vPpsValid and returns to vPpsNew within tPpsTransient.
    b. If the PUT responded to the previous Get_PPS_Status with the OMF flag set, the SPT verifies:
        i. If current leaves Operating Current range during the CV to CF transition, it does not exceed iPpsCVCLTransient
        ii. Current settles to Operating Current within tPpsCVCLTransient after the transition
    c. SPT sends Get_PPS_Status to PUT
    d. SPT verifies PUT responds with OMF flag cleared
8. The SPT verifies it did not enter step 6.k.4 and step 6.k.6 since step 6.k

7. SPT continues to step 4 with the next Operating Current Condition from C above
8. SPT continues to step 3 with the next Operating Voltage Condition from D above
9. SPT continues to step 2 with the next APDO supported by the PUT

SPT.8 Shared Capacity Load Test

D. Purpose:

1. The Load test verifies that when each port is fully loaded at voltage V the Source can still deliver voltage in the tolerance range of vSrcNew or vSafe5V.
2. The Load test verifies as each port is fully loaded remaining ports correctly offer remaining shared power.
3. This test is required for all USB Type-C Shared Capacity charging-capable products.

E. Asserts Covered:

USB PD 2.0	USB PD 3.0	USB Type-C
7.1.4#2	7.1.4.1#3	4.8.6.1#1
7.1.4#3	7.1.4.1#4	4.8.6.1#2
7.1.4#4	7.1.4.1#5	4.8.6.1#3
7.1.4#5	7.1.4.1#6	4.8.6.1#4
7.1.4#6	7.1.4.1#7	4.8.6.2#2
7.1.4#7	7.1.8#1	4.8.6.2#3
7.1.4#8	7.1.8#2	4.8.6.2#4
7.1.9#1	7.1.8#3	4.8.6.2#5
7.1.9#2		4.8.6.2#6
7.1.9#3		4.8.6.2#7
		4.8.6.2#8
		4.8.6.2#9
		4.8.6.2#10
		4.8.6.2#11
		4.8.6.2#12
		4.8.6.2#13
		4.8.6.2#14
		4.8.6.2#15
		4.8.6.2#16
		4.8.6.4#1
		4.8.6.4#2

		4.8.6.4#3

F. Procedure

1. SPT reads VIF to set expectation of ports being tested.
2. SPT verifies that the VIF indicates each port in a shared capacity group has the same PDP and PDOs listed.
3. SPT performs this step one port at a time. When one port completes all substeps, the SPT performs this step on the next port under test.
   a. STP connects the port.
   b. If the port successfully completes a PD Contract, SPT sends Discover Identity Request and reads the port's identifier from its Discovery Identity Response.
      1. SPT sends RDO for max advertised PDO with Capability Mismatch bit set.
      2. SPT verifies that:
         a. The port offers at least 7.5W in any Source Capabilities message.
         b. Within 3 seconds the port settles to a PD contract at its PDP.
   c. Else if the VIF contains Type-C ports with no PD and does not contain Type-A ports, SPT assumes the port is a Type-C port.
      1. SPT verifies that the port initially advertises 1.5A current.
      2. If the VIF indicates the port's PDP is 15W, SPT waits 1 second and verifies the port advertises 3A.
      3. SPT prompts the test operator to indicate which Type-C port identifier from the VIF matches the port.
   d. Else if the VIF contains Type-A ports and does not contain Type-C ports with no PD, SPT assumes the port is a Type-A port. SPT prompts the test operator to indicate which Type-A port identifier from the VIF matches the port.
   e. Else SPT prompts the test operator to indicate which port identifier from the VIF matches the port.
      1. If the port is a Type-C connector:
         a. SPT verifies that the port initially advertises 1.5A over Type-C Current.
         b. If the VIF indicates the port's PDP is 15W, SPT waits 1 second and verifies the port advertises 3A.
   f. SPT loads to max current in 25% increments, maintains max current for 2 sec and then SPT releases load in 25% increments. At each increment, the SPT verifies if the Source voltage leaves vSrcNew range, it stays within vSrcValid and returns to vSrcNew within tSrcTransient.
   g. SPT disconnects the port.
4. If the product under test has more than one power gang or any assured ports:
   a. SPT connects to a port from each power gang.
   b. SPT verifies:
      1. For a PD port, SPT verifies within 3 seconds the port settles to a PD contract at its PDP
      2. For a Type-C port, SPT verifies within 1 second the port settles to an Rp value

c. SPT loads each connected port to their Maximum Current in 25% increments
d. At each increment, SPT verifies:
    1. If the Source voltage leaves vSrcNew range, it stays within vSrcValid and returns to vSrcNew within tSrcTransient.
    2. The remaining ports do not droop below max (330mV, vSrcNew) or droop for longer than vSrcTransient.

5. If the product under test includes any assured power ports:
    a. SPT connects to each assured port.
    b. SPT verifies PDP is offered upon connect
    c. SPT loads each port to their Maximum Current in 25% increments.
    d. At each increment, SPT verifies:
        1. If the Source voltage leaves vSrcNew range, it stays within vSrcValid and returns to vSrcNew within tSrcTransient.
        2. The remaining ports do not droop below max (330mV, vSrcNew) or droop for longer than vSrcTransient.
6. SPT disconnects all ports
7. SPT connects all Type-A ports and loads these ports to 500mA.
    a. SPT verifies these ports remain within vSafe5V for the remainder of the test.
8. SPT connects all Type-C ports with no PD.
    a. SPT verifies that each port initially offers 1.5A current
    b. If there is enough remaining shared power for X number of ports to advertise 3A:
        1. SPT Waits 1 second.
        2. SPT verifies that X number of ports advertise 3A Type-C Current
    c. SPT loads each port to max current in 25% increments. At each increment, the SPT verifies:
        1. If the Source voltage leaves vSrcNew range, it stays within vSrcValid and returns to vSrcNew within tSrcTransient.
        2. The remaining ports do not droop below max (330mV, vSrcNew) or droop for longer than vSrcTransient.
9. SPT connects all Type-C ports with PD. SPT sets RDOs for maximum advertised PDO voltage and current and with Capability Mismatch bit set to 1.
    a. SPT verifies that:
        1. Each of these ports always offers at least 7.5W in its Source Capabilities.
        2. Within 3 seconds all ports settle to contracts such that the total of all contract power is equal to the group shared power capacity (within 1W).
    b. SPT loads each port to its contract's max current in 25% increments. At each increment, the SPT verifies:
        1. If the Source voltage leaves vSrcNew range, it stays within vSrcValid and returns to vSrcNew within tSrcTransient.
        2. The remaining ports do not droop below max (330mV, vSrcNew) or droop for longer than vSrcTransient.
    c. SPT requests 5V 0A on one port.

d. SPT verifies that within 3 seconds all ports in that port's gang settle to contracts such that the total of all contract power is equal to the min(group shared power capacity, (num of ports – 1)* port PDP) (within 1W)
e. If the product under test has multiple gangs:
    1. SPT requests 5V 1.5A on one port on each PD power gang
    2. SPT verifies that for each gang, within 3 seconds of that gang's port contract changing, all ports in the gang settle to contracts such that the total of all contract power is equal to the min(group shared power capacity, ((num of ports -1) * PDP) – 7.5W) (within 1 W)
f. SPT loads each port to their Maximum Current in 25% increments.
g. At each increment, SPT verifies:
    1. If the Source voltage leaves vSrcNew range, it stays within vSrcValid and returns to vSrcNew within tSrcTransient.
    2. The remaining ports do not droop below max (330mV, vSrcNew) or droop for longer than vSrcTransient.

10. SPT disconnects all ports from all power gangs.
11. For each Type-C Current power gang, SPT connects all ports for those power gangs at once.
    a. SPT verifies:
        1. If the Available Shared power on a port is less than 15W, then the port initially advertises 1.5A Rp.
        2. Within 1 second, all ports in the gang must settle into Rp levels such that the total of all Rp advertisements is equal to the min(group shared power capacity, ((num of ports – 1) * PDP) – 7.5W)
12. For each USB PD power gang, SPT connects all ports for those power gangs at once.
    a. SPT verifies:
        1. The gang never has contracted more than Available Shared Capacity on any port (For each port, Available Shared Capacity is Total Shared Capacity – Other Ports Contracted Power – (num of other unattached ports * 7.5W))
        2. Within 3 seconds, all ports in the gang must settle into contracts such that the total of all contract power is equal to group Total Shared Capacity (within 1W)
        3. No port enters a contract for less than 7.5W.
    b. SPT loads each port to their Maximum Current in 25% increments.
    c. At each increment, SPT verifies:
        1. If the Source voltage leaves vSrcNew range, it stays within vSrcValid and returns to vSrcNew within tSrcTransient.
        2. The remaining ports do not droop below max (330mV, vSrcNew) or droop for longer than vSrcTransient.