USB Type-C ENGINEERING CHANGE NOTICE

Title: USB Type-C Chapter 6 including USB4 V2 LRD and OIAC updates
Applied to: USB Type-C Specification Release 2.1, May 2021

Brief description of the functional changes proposed:
1) Restructure USB-Type-C Specification Chapter 6 – to break out OIAC from Active Cable. 2) Reorganize Chapter 6, to Generic Active Cable Specification, Active Cables, and OIACs 3) Incorporated LRD section from ECR- USB4® V2 LRD Updates 4) Update OIAC section to clarify USB-PD filtering 5) Update OIAC section for USB4v2

Benefits as a result of the proposed changes:
1) Easier readability for active cable or OIAC manufacturer, as each section is separated out. 2) OIAC section is updated to USB4v2 with all related USB-PD commands

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
1) None

An analysis of the hardware implications:
N/a

An analysis of the software implications:
n/a

An analysis of the compliance testing implications:
N/a

Actual Change Requested

[EDITOR NOTE: Editorially, this ECN does not reflect what was finally incorporated into the USB Type-C Release 2.2 specification. Please refer to the published spec for the official update. Also, included at the end of this document is a new Appendix J which is referenced earlier in Section 6.1.2.5.3]

(a). Section X.X.X, Table/Figure X-XX (if applicable), Page X-XX

From Text:

To Text:

6 Active and Optically Isolated Active Cables

Active cables shall minimally support *USB 3.2* Gen 2x2. *USB4* active cables shall support ~~all *USB 3.2* rates and~~ *USB4* as well as all *USB 3.2* rates. Active cables shall support *USB PD* eMarkers and may support Alternate Modes and advertise them as defined in Section 6.1.1.

All *USB4™* active cables shall be interoperable with Thunderbolt™ 3 as defined in the *USB4* Specification (Chapter 13) and this specification (Section 6.7 and Appendices E and F).

Active cables supporting lengths up to 5 meters shall work in both directions and plug orientations and should function like passive cables from the user's perspective. Hybrid Optical active cables use copper for power and low-speed data and optical for high-speed data. They ~~active cables~~ are functionally the same as active cables and shall function like passive cables from the user's perspective.

Optically Isolated Active Cables (OIACs) are a *special case of active cables* ~~and have special~~with unique requirements and limitations that are specific to OIACs. OIACs can support longer lengths up to 50 meters and provide electrical isolation between the two ends of the cable. OIACs are targeted for Industrial, Machine Vision, Remote Sensor, Pro Video, and medical applications. OIACs do not 'just work' unlike active cables. Further details on the requirements and limitations for the OIAC are in section 6.3

6.1 Generic Specification to Active and Optical Isolated Active Cables

6.1.1 Discovering Cable Characteristics

The *USB PD* ***Discover_Identity*** Command is used to discover the characteristics of the active cable. This command shall only be sent to SOP'. All active cables shall respond to the ***Discover_Identity*** Command with Active Cable VDOs that return~~s~~ information about the cable. Note the active cable ~~shall~~ should respond ~~using either~~with *USB PD* Revision ~~2~~3 but may respond ~~or~~ with *USB PD* Revision ~~3~~ 2 following the *USB PD* Interoperability rules.

Table 6-3 summarizes the *USB4* cables regarding key identity values that will be returned to *USB PD* Revision 3 ***Discover_Identity*** commands.

Table 6-3 USB4 Cable Identity Summary

USB4™ Cable	Function				SOP' Configuration (USB PD Revision 3)					
					ID Header VDO	Passive Cable VDO	Active Cable VDO 1	Active Cable VDO 2		
	USB2	USB3	TBT3	DP	Cable Plug Passive/ Active B29…27	Cable Termination Type B12…11	Cable Termination Type B12…11	Physical connection B10	Active element B9	Optical Isolated Active Cable B2
Passive[1]	Yes	Yes	Yes	Yes	011b	00b/01b	n/a	n/a	n/a	n/a
TBT3 Linear Re-driver[1]	Yes	Yes	Yes	Opt.	011b	01b[2]	n/a	n/a	n/a	n/a
Linear Re-driver (Gen4)[1]	Yes	Yes	Yes	Opt.	100b[4]	n/a	10b/11b	0b	0b	0b
					011b[4]	01b[2]	n/a	n/a	n/a	n/a
Re-timer[1]	Yes	Yes	Yes	Opt.	100b	n/a	10b/11b	0b	1b	0b
Hybrid Optical [1, 3]	Yes	Yes	Yes	Opt.	100b	n/a	11b	1b	0b/1b	0b
Optically Isolated	No	Yes	Opt.	No	100b	n/a	11b	1b	0b/1b	1b

Notes:

1. *USB4* cables, with the exception of Optically-Isolated cables, are required to support Thunderbolt™ 3 compatibility. The TBT3-specific identity requirements are defined in Appendix F.
2. The TBT3 Linear Re-driver active cable represents as only a Passive Cable that is discovered per Figure 5-1.
3. A Hybrid Optical active cable is defined as using an intermediate optical transmission line for the high-speed signaling path (TX/RX) while retaining a copper-based solution for the rest of the defined interfaces.[RD1]
4. The *USB4* Gen4 Linear Re-driver active cable identifies as either an Active Cable or Passive Cable (for backward compatibility) depending on the version number (B14…11) given in the *USB PD* Structured VDM Discover Identity message as follows: for B14…11 = 0101b, the cable identifies as Active, and for B14…11 = 0100b, the cable identifies as Passive.

Note: As indicated in Table 6-3, *USB4* passive cables are required to support Thunderbolt™ 3 compatibility. The implication of this requirement is that *USB4* Gen3 passive cables will properly respond to TBT3 Passive Cable Discover Identity commands with the VDOs as defined in Table F-1 and Table F-3 of Section F.2.1 in order that they will be used in a TBT3 connection at Gen3 speeds. *USB4* Gen2 cables should not implement TBT3 Passive Cable Identity VDOs.

Table 6-2 ~~Summary of~~ Active Cable Features

Cable Type	Length	USB PD	VBUS	VCONN Wiring	CC	*USB 2.0*	*USB 3.2* (All required)	*USB4*	Alternate Modes	SBU
USB 3.2 Active	< 5 m	SOP' Required (SOP" Optional)	3 A or 5 A	Same as passive cable	Same as passive cable	Same as passive cable	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	N/A	Optional	Note 3 Note 4
USB4 Active	< 5 m	SOP' Required (SOP" Optional)	3 A or 5 A	Same as passive cable	Same as passive cable	Same as passive cable	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	Gen2 Gen3 Gen4	TBT3 Note 2	Note 3 Note 5
USB4 Hybrid Active[8]	< 5 m	SOP' Required (SOP" Optional)	3 A or 5 A	Same as passive cable	Same as passive cable	Same as passive cable	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	Gen2 Gen3 Gen4	TBT3 Note 2	Note 3 Note 5

Note 2: Thunderbolt™ 3 Alternate Mode support required as defined in Appendix F.

Note 3: A passive connection in *USB 3.2* mode is required.

Note 4: Support for SBU is optional normative in Alternate Modes.

Note 5: SBU support for *USB4* can be either passive or active in the case of a linear re-driver-based active cable or active in the case of a re-timer-based active cable.

All active cables, regardless of length, shall be compliant with this specification, the *USB 3.2* including Appendix E, and the *USB 3.2* Active Cable CTS.

6.1.2 Electrical Requirements

6.1.2.1 Shielding Effectiveness Requirement

All active cables shall meet the shielding effectiveness requirement defined in Section 3.7.7 and Figure 3-65.

6.1.2.2 Low Speed Signal Requirement

6.1.2.2.1 CC Channel Requirements

Active cables shall meet the Low-Speed Signal Requirements in Section 3.7.2.4.

6.1.2.2.2 SBU Requirements

~~*** Need text to the effect that SBU in USB3 == SBx in USB4 ***~~

The SBUs are a pair of end-to-end electrical connections in the cable. While USB 3.2 does not use these connections, they are used by alternate modes such as Display Port. USB4 also uses these connections, but has renamed them as SBTX and SBRX. The electrical requirements are the same for both.

Active cable~~s~~ SBU wires shall meet the requirements defined in Table 6-16 and shall meet the crosstalk requirements both near-end and far-end between the low speed signals as defined in Section 3.7.2.4.

SBUs have no guaranteed performance when Vconn is not provided to the cable. The Host or Device shall not provide any signal beyond what is defined in Table 6-16 when VCONN has not been provided.

Table 6-16 Summary of Active Cable Features

Name	Description	Min	Max	Units
zCable_SBU	Cable characteristic impedance on the SBU wires	32	53	Ω
tCableDelay_SBU	Cable propagation delay on the SBU wire		26	ns
rCable_SBU	DC resistance of SBU wires in the cable in USB		40	Ω
vCable_SBU	Cable voltage swing on SBU wires	−0.3	4.0	V
Insertion Loss[1]	Cable insertion Loss		5 @ 0.5 MHz 7 @ 1 MHz 12 @ 10 MHz 13 @ 25 MHz 15 @ 50 MHz 16 @ 100 MHz	dB
iCableSBU	Maximum end-to-end current	−25	+25	mA

Note 1: Measurement referenced to 50 Ohms.

6.1.2.3 USB 2.0

Active cables shall meet the *USB 2.0* requirements defined in Section 3.7.2.4 and 3.7.2.7.

Note: Active Cables greater than 5m report the number of hub hops consumed in the Active Cable VDOs.

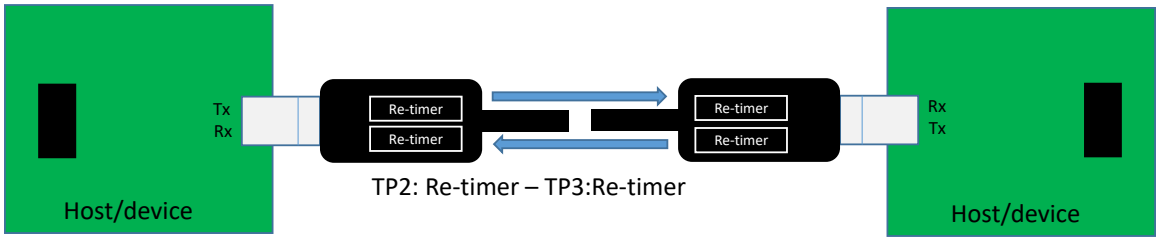
6.1.2.4 USB 3.2

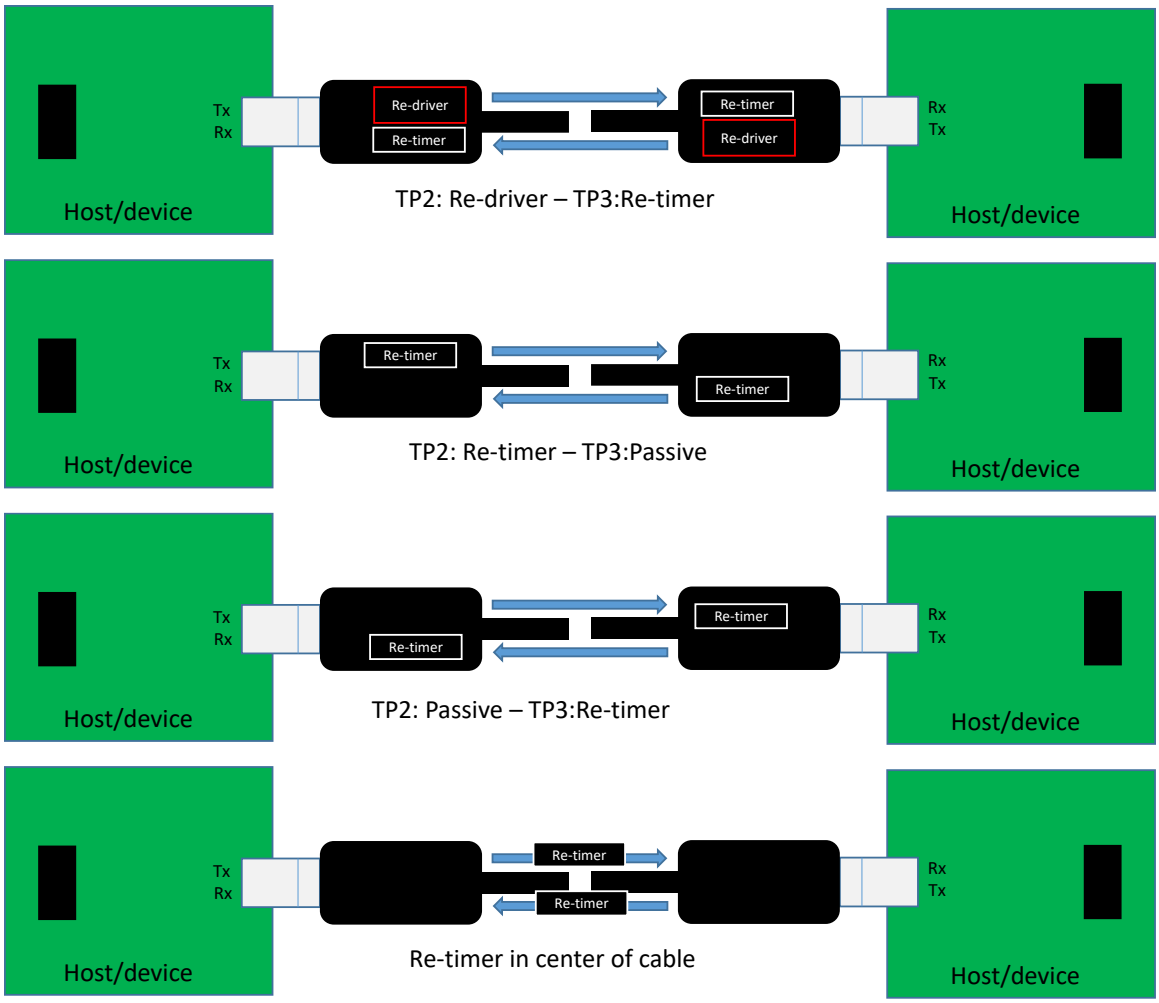
Active cables shall incorporate AC-coupling from the plug to repeater on both the *USB 3.2* TX and RX signals. Active cables shall provide a discharge path for discharging the AC-coupling capacitors in the cable on unplug per *USB 3.2*.

6.1.2.4.1 USB 3.2 Active Cable Architectures

Active cables may have the combinations of re-timers and re-drivers as illustrated in Figure 6-18. Active cables without at least one re-timer are out of scope. Active cables without re-timers connected to TP3 are out of scope. Active cables shall support the features defined in Table 6-2.

Figure 6-18 Active Cable Topologies





6.1.2.4.2 USB 3.2 Power-on and Rx.Detect

Active cables shall present a high impedance to ground of $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ when not powered. Active cables shall present a high impedance to ground of $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ at initial power-on. The active cable shall perform far-end receiver termination detection on both cable ends upon receiving V_{CONN}. Upon detecting a far-end low-impedance receiver termination ($R_{RX\text{-}DC}$), the active cable shall enable its low-impedance receiver termination ($R_{RX\text{-}DC}$) to mirror the presence of the Host/Device. The active cable shall perform far-end receiver termination detection for Repeaters per *USB 3.2* including in low power states U2/U3.

An active cable shall complete power-on and far-end receiver termination detection through the cable within $t_{FWD_RX.DETECT}$.

Table 6-17 Active Cable Power-on Requirements

Name	Minimum	Maximum	Units
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	Per *USB 3.2*	Per *USB 3.2*	
$R_{RX\text{-}DC}$	Per *USB 3.2*	Per *USB 3.2*	
$t_{FWD_RX.DETECT}$		42[1]	Ms

Note 1: 84 ms – (2 * 12 ms + 18 ms) worst case.

Active cables including OIACs shall reflect the receiver terminations across the cable to replicate the behavior of a passive cable.

6.1.2.4.3 USB 3.2 U0 Delay

All active cables shall meet the *USB 3.2* delay defined in Table 6-18.

Table 6-18 ~~OIAC~~ Maximum USB 3.2 U0 Delay

USB 3.2 Gen	Cable Maximum U0 Delay	Description
Gen1	3000 ns	Note: Active cables with *USB 3.2* Gen1 latency larger than 125 ns may not function correctly when used in conjunction with host, devices, and hubs that do not support *USB 3.2.*
Gen2	3000 ns	Note: Active cables with *USB 3.2* Gen2 latency larger than 305 ns may not function correctly when used in conjunction with host, devices, and hubs ~~which~~ that do not support *USB 3.2.*

6.1.2.4.4 USB 3.2 U-State Power Requirements

Active cables shall meet the VCONN power requirements for *USB 3.2* operation in Table 6-20. These requirements are for the entire cable not just a cable plug.

Table 6-20 USB 3.2 U-State Requirements

State	Maximum Power Consumption VCONN	Power Consumption Notes
U0	1.0 W single-lane 1.5 W dual-lane	Applies to POLLING.LFPS, TRAINING, and RECOVERY states.
U1	≤ U0 power	Forwarding LFPS is required
U2	≤ U1 power	Forwarding LFPS is required
U3	20 mW	Steady state power. eMarker in sleep.
Rx.Detect	20 mW	Rx.Detect period may be lengthened when no *USB 3.2* terminations have been detected. eMarker in sleep.
eSS.Disabled	20 mW	*USB 3.2* is disabled. eMarker in sleep.

6.1.2.4.5 USB 3.2 U-State Exit Latency

Active cables shall meet the U-state exit latency defined in *USB 3.2* Appendix E.

6.1.2.4.6 USB 3.2 Signal Swing

An active cable transmitter only has to drive 8.5 dB insertion loss at 5 GHz to the Host/Device controller receiver for *USB 3.2* Gen2, if the transmitter is located in the cable plug next to the receiving port.

A Host/Device controller transmitter must drive a total loss of 23 dB at 5 GHz to the far side for *USB 3.2* Gen2. The difference in loss budget allows the active cable transmitter swing to be reduced. An active cable receiver can assume a larger receiver swing than in the Host/Device for the same reason.

Figure 6-20 defines the SuperSpeed electrical test points and is copied from the *USB 3.2* specification. Figure 6-21 indicates the test points and test equipment connections.

Figure 6-20 SuperSpeed USB Electrical Test Points

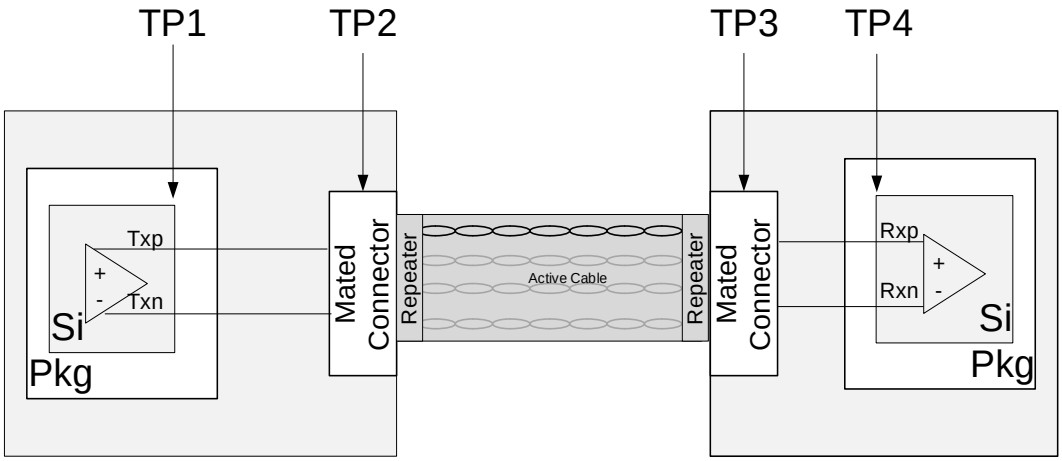
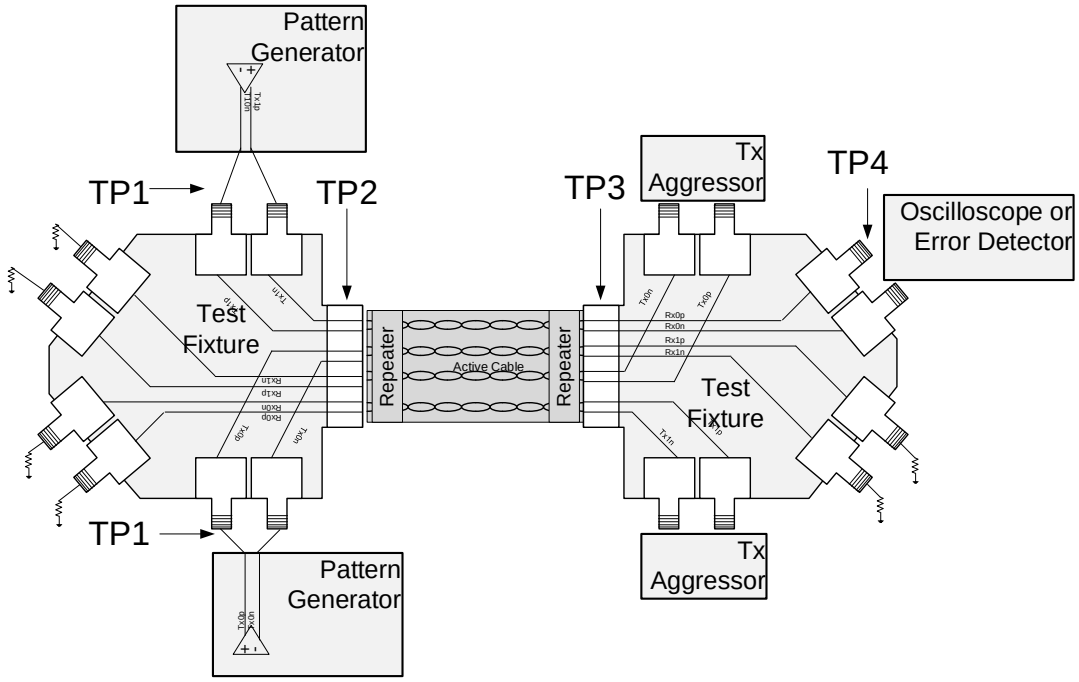


Figure 6-21 SuperSpeed USB Compliance Test Setup



6.1.2.4.6.1 TP1 – Active Cable Input Stressed Source

The active cable input stressed source is generated at TP1 per Table 6-21 for amplitude and per Table 6-22 for jitter. SSC shall be present in the stressed signal at TP1. Table 6-21 is a subset of the *USB 3.2* Table 6-18. Table 6-22 is a subset of *USB 3.2* Table 6-28. If any discrepancy exists between this specification and the *USB 3.2* specification, the *USB 3.2* specification shall take precedence.

The maximum swing with the maximum de-emphasis and pre-shoot shall be tested with the minimum loss compliance test board. The minimum swing with the minimum de-emphasis and pre-shoot shall be tested with the maximum loss compliance test board. The input jitter composition is the same for both the minimum and maximum swing stressed sources.

The active cable shall function over the range of parameter in *USB 3.2* Table 6-17 and Table 6-21.

Table 6-21 Active Cable USB 3.2 Stressed Source Swing, TP1

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p TX voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX\text{-}DE\text{-}RATIO}$	TX de-emphasis	*USB 3.2* Table 6-17	−3.1 ± 1.0	dB	Nominal is 3.5 dB for Gen1 operation. Gen2 transmitter equalization requirements are described in *USB 3.2* Section 6.7.5.2.
$V_{PRESHOOT}$	TX Preshoot	*USB 3.2* Table 6-17	2.2 ± 1.0	dB	Gen2 transmitter equalization requirements are described in *USB 3.2* Section 6.7.5.2.

Table 6-22 Active Cable USB 3.2 Stressed Source Jitter, TP1

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.0100	UI rms	1
$J_{Rj_p\text{-}p}$	Random Jitter peak-peak at 10^{-12}	0.17	0.14	UI p-p	1,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2	4.76	UI p-p	1,2,3
J_{Pj_1Mhz}	Sinusoidal Jitter	1	2.03	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	0.87	UI p-p	1,2,3
J_{Pj_4MHz}	Sinusoidal Jitter	N/A	0.37	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p	1,2,3

Notes:

1. All parameters measured at TP1. The test point is shown in Figure 6-20 and Figure 6-21.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the RX is required to tolerate Pj at all frequencies between the compliance test points.
3. During the RX tolerance test, SSC is generated by test equipment and present at all times. Each JPj source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the RX tolerance test.
5. The JTOL specs for Gen2 comprehend jitter peaking with re-timers in the system and has a 25 dB/decade slope.

6.1.2.4.6.2 TP2 – Active Cable Input (Informative)

The values in Table 6-23 indicate the informative input signal swings at TP2 for an active cable. Table 6-23 is included to provide guidance beyond the normative requirements of Table 6-21 and Table 6-22. An active cable can be fully compliant with the normative requirements of this specification and not meet all the values in Table 6-23. Similarly, an active cable that meets all the values in Table 6-23, is not guaranteed to be in fully compliance with the normative part of this specification.

Table 6-23 Active Cable USB 3.2 Input Swing at TP2 (Informative)

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p TX voltage swing	250 (min) 1000 (max)	250 (min) 850 (max)	mV	Nominal is 550 mV p-p
$V_{TX\text{-}DE\text{-}RATIO}$	TX de-emphasis	0 (min) 4.0 (max)	2.1 (min) 4.1 (max)	dB	There is no de-emphasis requirement for Gen1.
$V_{PRESHOOT}$	TX Preshoot	NA	1.2 (min) 3.2 (max)	dB	Applicable to *USB 3.2* Gen2 operation only.

6.1.2.4.6.3 TP3 – Active Cable Output (Informative)

The values in Table 6-24 indicate the informative output signal swings at TP3 for an active cable. Table 6-24 is included to provide guidance beyond the normative requirements of Table 6-21 and

Table 6-22. An active cable can be fully compliant with the normative requirements of this specification and not meet all the values in Table 6-24. Similarly, an active cable that meets all the values in Table 6-24, is not guaranteed to be in full compliance with the normative part of this specification.

Table 6-24 Active Cable USB 3.2 Output Swing at TP3 (Informative)

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential RX peak-to-peak voltage	300 (min) 850 (max)	300 (min) 850 (max)	mV	Measured after the RX EQ function Nominal is 0.5 V p-p
$V_{TX\text{-}DE\text{-}RATIO\text{-}GEN1}$	TX de-emphasis	0 (min) 4.0 (max)	NA	dB	No pre-shoot allowed
$V_{TX\text{-}DE\text{-}RATIO}$ + $V_{PRESHOOT\text{-}GEN2}$	TX de-emphasis + TX Preshoot	NA	0 (min) 3.0 (max)	dB	Sum of the de-emphasis and pre-shoot. There is no de-emphasis and pre-shoot requirement.

6.1.2.4.6.4 TP4 – Active Cable Output

The active cable transmitter output is defined at TP4 for both high and low loss channels. The requirements for TP4 are defined in the *USB 3.2* specification Table 6-20. The input signal for the test shall be applied at TP1 as defined in the *USB 3.2* specification.

The low loss test board shall be used to test the maximum output swing. The maximum loss test board shall be used to test the minimum output swing. Jitter must be met with both test boards.

The active cable bit-error-rate shall be tested at TP4 and meet or exceed a BER of 10^{-12}. The error detector used shall have the ability to remove SKP ordered sets.

6.1.2.5 USB4

This section describes the electrical requirements and compliance testing for *USB4* active cables. The compliance testing is defined to ensure interoperability in terms of data integrity and electrical specifications enabling the active cable to reliably receive an input signal and output a valid signal at its other end.

The *USB4* active cable types are:

1. Re-timer-based active cable (this section covers re-timer based cable for *USB4* only, *USB 3.2* re-timer cable is defined in Section 6.1.2.5.2)
2. Linear re-driver-based (LRD-based) active cable (*USB 3.2* and *USB4*)
3. Linear optical active cable
   (electrical spec not defined yet)

6.1.2.5.1 Electrical Requirements That Apply to All Active Cable Types

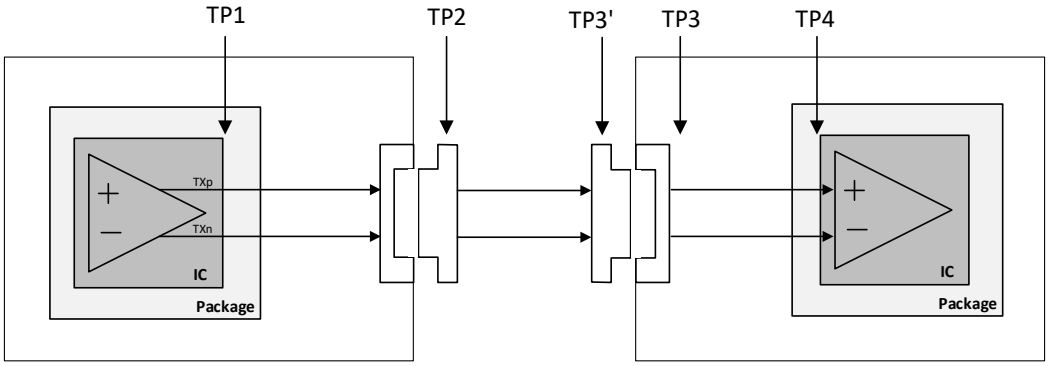
6.1.2.5.1.1 System Compliance Test Point Definition

All measurements shall be referenced to the following compliance points. Calibration shall be applied in cases where direct measurement is not feasible.

Table 6-25 Compliance Points Definition

Test Point	Description	Comments
TP1	Transmitter IC output	Not used for electrical testing
TP2	Transmitter port connector output	Measured at the plug side of the connector
TP3	Receiver port connector output	Measured at the receptacle side of the connector. All the measurements at this point shall be done while applying reference equalization function
TP3'	Receiver port connector input	Measured at the plug side of the connector
TP4	Receiver IC input	Not used for electrical testing

Figure 6-22 Compliance Points Definition



6.1.2.5.1.2 Compliance Receptacle Test Boards

The USB Type-C high speed test fixture shall be used to enable cable compliance testing. The fixture shall be comprised of a high-quality USB Type-C receptacle and a short PCB trace that may be connected to coaxial cable with SMA/SMP connector at its end. Because TP2 and TP3' reference points are located on the USB Type-C plug side of the connector, the loss and distortion of the receptacle fixture shall be calibrated such that all the measured values correspond to the standard reference points. The reference point TP3 is defined such that the insertion-loss from the connector pads to the compliance point is 0.5 dB ± 0.25 dB at 5GHz and 1 dB ± 0.25 dB at 10 GHz. Extra loss and distortion elements shall be compensated by physical and/or mathematical means.

The target impedance of the fixture shall be 85 Ω. AC coupling capacitors shall be placed on the receptacle test fixture following the Router Assembly requirements as specified in *USB4* specification and CTS.

6.1.2.5.1.3 AC Coupling Capacitors

Active cables shall include AC-coupling capacitance between 135 nF and 265 nF inside their plugs placed at the output transmit path and between 300 nF and 363 nF at the input receive path. Discharge resistors between 200 KΩ and 242 KΩ shall be placed at the input receive path. See Figure 3-3 in the *USB4* specification for a diagram of the AC-coupling capacitors and discharge resistors.

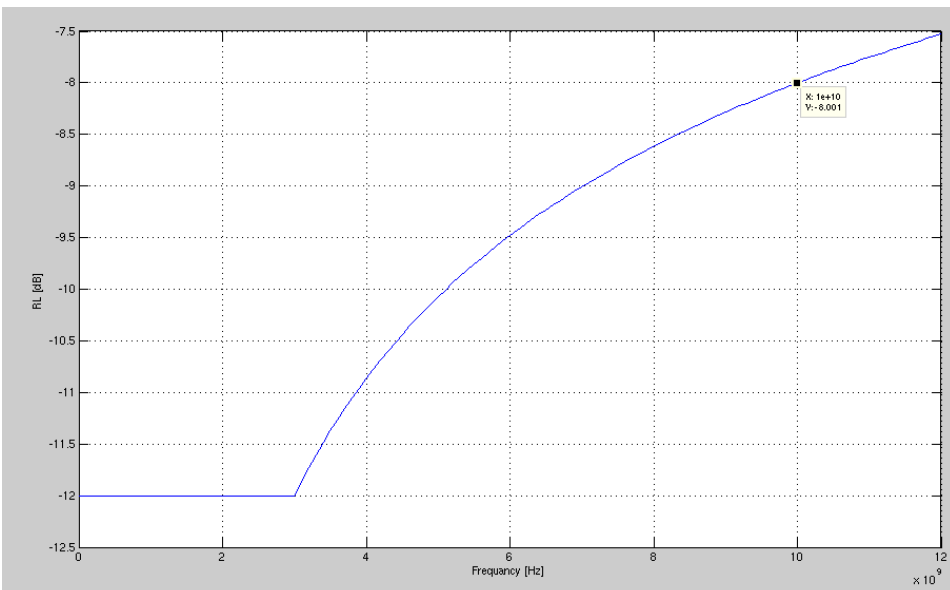
Active cable designs need to consider that a change of current consumption from V_{BUS} as allowed by *USB Power Delivery* can add a considerable amount of common mode offset that may not be handled by the AC-coupling in this spec.

6.1.2.5.1.4 Differential Return-Loss Mask (Informative)

Re-timer and re-driver cable input and output return-loss measurements shall be referenced to a differential impedance of 85 Ω. When measured at TP3' and TP1 (respectively), the differential mode return loss recommended to not exceed the limits given in the following equation:

$$SDD22(f), SDD11(f) = \begin{cases} -12 & 0.05 < f_{GHz} \leq 3 \\ -7.5 + 7.5 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$

Figure 6-23 RX Differential Return-Loss Mask



6.1.2.5.2 Re-timer-based Active Cable Electrical Specifications

This section describes the electrical requirements and compliance testing for *USB4* re-timer-based active cables.

6.1.2.5.2.1 Output Equalization

A *USB4* active cable shall implement tunable 3-tap finite-impulse-response (FIR) equalization at its output. The transmit equalization shall support 16 preset configurations with different de-emphasis and pre-shoot settings as specified in the *USB4* specification, and shall be measured at TP3'.

6.1.2.5.2.2 High-Speed Specifications

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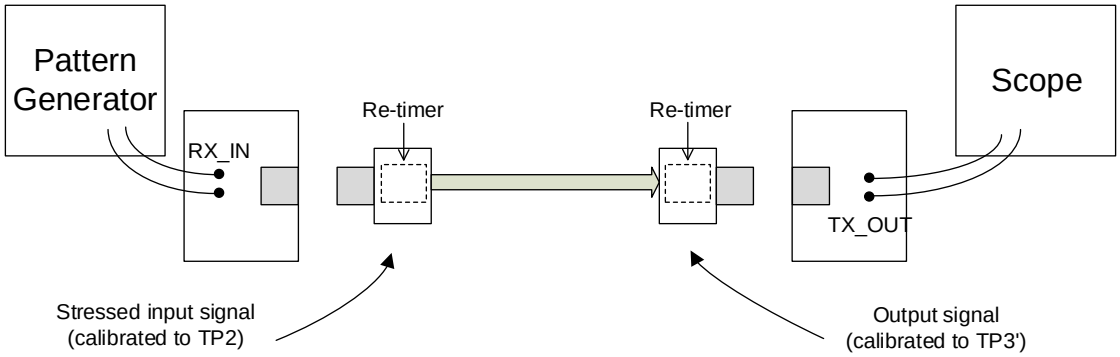
Figure 6-24 Active Cable Compliance Test Setup



6.1.2.5.2.3 Cable Compliance Testing

Table 6-26 defines the *USB4* Active Cable specifications for Gen2 and Gen3 systems at TP3'. These parameters shall be measured at the Active Cable's output while applying a stressed signal at the input as specified in Table 6-27.

A *USB4* active cable shall be tested by injecting several different periodic jitter components, one at a time. The test shall include sinusoidal jitter frequencies of 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz. In all cases, the incoming signal shall include SSC modulation on top of the sinusoidal jitter component at the range of 300ppm to −5300ppm. PRBS31 pattern shall be used for *USB4* active cable compliance testing. However, calibration of the stressed signal source may be performed with a periodic pattern shorter than PRBS31. AC common-mode noise shall be added at the pattern generator output to ensure worst-case transmitter characteristics. The total common-mode noise shall be 100 mV peak-to-peak at TP2, where the added noise profile shall be sinewave at frequency not smaller than 400 MHz. All the specified jitter values shall be calibrated while applying the reference CDR defined in the *USB4* specification.

A *USB4* active cable receiver may configure its Link Partner's TX equalizer during the Link establishment. The pattern generator shall support tunable 3-tap FIR at its output, which may be adjusted during the test by the receiver under test through out-of-band software channel.

Table 6-26 Re-timer-based USB4 Active Cable Output Specifications Applied for All Speeds (at TP3')

Name	Description	Min	Max	Units	Comments
CABLE_BER	End to End bit error rate		1E−12		See Note 1
AC_CM	Output AC Common Mode Voltage		100	mV pp	
LANE_TO_LANE_SKEW	Cable's Input-to-Output Skew between lanes		18	ns	
NRL	Noise Contributed by Integrated Return Loss				See 6.1.2.5.2.5
JTF_BW	Jitter tracking (forwarding) 3dB bandwidth from cable input to output		0.5	MHz	See Note 2
JTF_PEAKING	Jitter amplification from cable input to output		0.3	dB	Measured from 0 to 0.5 MHz. See Note 2

Name	Description	Min	Max	Units	Comments
SSC_VARIATION	SSC output to input down-spread variation	−0.3	+0.3	dB	See Note 2
SSC_SLEW_RATE	SSC frequency slew rate (df/dt) during steady-state		1250	ppm/µs	See Note 3
INIT_FREQ_VARIATION	Non-modulated transmit frequency accuracy during the initial stages of the training period	−300	+300	ppm	See Notes 4 and 5
DELTA_FREQ_200ns	Transmit frequency variation over 200 ns measurement windows following the switching from local to recovered clock		1400	ppm	See Notes 4 and 5
DELTA_FREQ_1000ns	Transmit frequency variation over 1 µs measurement windows following the switching from local to recovered clock		2200	ppm	See Notes 4 and 5
V_OUTPUT_DC_AC_CON N	Instantaneous DC+AC voltages at the cable output side of the AC coupling capacitors	−0.5 (min1) −0.3 (min2)	+1.0	V	See Note 6
TJ	Total Jitter		0.32	UI pp	See Notes 7 and 9
UDJ	Deterministic jitter that is uncorrelated to the transmitted data		0.13	UI pp	
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter		0.06	UI pp	See Note 10
DCD	Deterministic Jitter Associated by Duty-Cycle-Distortion		0.03	UI pp	
Y1	Eye inner height at TP3' (one-sided voltage opening of the differential signal)	200		mV	Measured for 1E6 UI. See Notes 8 and 9, and *USB4* specification.
Y2	Eye outer height at TP3' (one-sided voltage opening of the differential signal)		650	mV	Measured for 1E6 UI. See Notes 8 and 9, and *USB4* specification.

Name	Description	Min	Max	Units	Comments

Notes:

1. The cable BER requirement is referred to the raw data, without applying forward error correction nor pre -coding.
2. JTF_BW and JTF_PEAKING characterizes the corresponding input-to-output low-pass Jitter Transfer Function bandwidth and peaking. In addition, it is required that the cable will not change the SSC modulation depth by more than specified. For verifying that, the SSC down-spreading depth of the cable input and output shall be compared.
3. The SSC slew rate shall be extracted from the transmitted signal over measurement intervals of 0.5 µs. The SSC slew-rate shall be extracted from the transmitter phase after applying a 2nd order low-pass filter with 3 dB point at 5 MHz. Steady-state clocking shall be applied from the point that SLOS training pattern is forwarded by the transmitter.
4. As shown in Figure 6-25, the initial transmit frequency is not modulated. The transmit frequency variation following the switching from local to recovered clock shall be measured over time intervals of 200 ns and 1 µs.
5. Measurement shall be performed over the transmitted signal. The signal phase shall be extracted while applying 2nd order low-pass filter with 3 dB point at 5 MHz.
6. The absolute single-ended voltage seen by the receiver. This requirement applies to all link states and during power-on, and power-off. (min1, max) is measured with a 200 KΩ receiver load, and (min2, max) is measured with a 50 Ω receiver load. The ground offset between the cable output and UFP is not included in V_OUTPUT_DC_AC_CONN.
7. TJ is defined as the sum of all "deterministic" components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).
8. The output voltage is differential.
9. Transmit jitter shall be measured while applying the reference CDR described in the *USB4* Specification. Note that the measured jitter includes residual SSC jitter passing the reference CDR.
10. UDJ_LF is the uncorrelated deterministic jitter measured after applying 2nd order Low-Pass-Filter with 3 dB cut-off at 0.5 MHz on the measured jitter. This filter needs to be applied on top of the reference CDR rejection function. The measurement shall be performed while applying input stress signal with periodic jitter component of 100 MHz.

Figure 6-25 Example for Transmitter Frequency Variation During Clock Switching

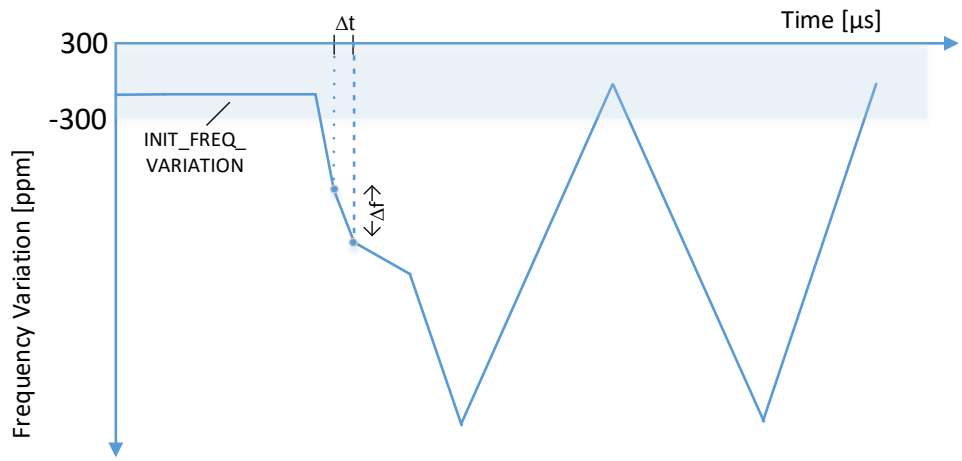
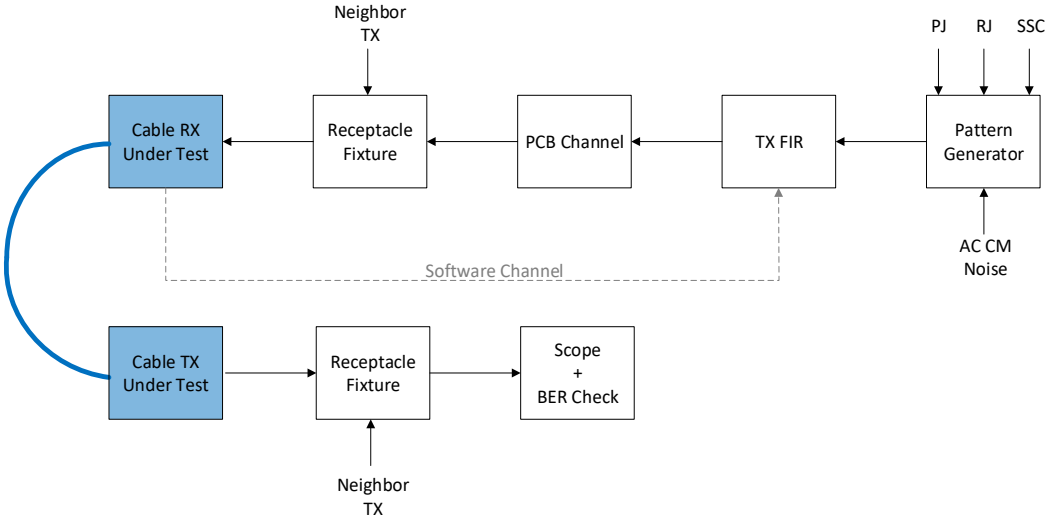


Table 6-27 Stressed Received Conditions for USB4 Gen2 and Gen3 Cable Compliance Testing (at TP2)

USB4 Gen	Inner eye Voltage [mV peak]	Data Dependent Jitter (DDJ) [UI peak-to-peak]	Random Jitter [UI peak-to-peak]	Periodic Jitter [UI peak-to-peak]	Total Jitter [UI peak-to-peak]
Gen2	140	0.12	0.14	0.17	0.43
Gen3	120	0.15	0.14	0.17	0.46

Figure 6-26 Active Cable Functional Test Setup



6.1.2.5.2.4 Cable Error-Bursts Testing

In order to facilitate proper FEC operation, an active cable receiver shall take steps to limit the probability that a burst of errors is restarted immediately after receiving one or more correct bits (see *USB4* specification). The cable receiver under test shall trigger on bit-errors and shall capture error events that follow.

The test setup shall be initialized with the same configuration used for testing the uncoded BER with periodic jitter component of 100 MHz. As part of this setup, PRBS31 pattern is assumed and neither forward-error-correction nor pre-coding are applied. After initialization, the periodic jitter magnitude shall be increased to the point where uncoded BER of 1E−8 is observed. The receiver under test shall trigger on bit-error and shall capture error events that follow. An error event is defined as a mismatch between the received data and the reference PRBS31 pattern. At least 32 consecutive bits shall be examined for errors starting from the initial trigger. The probability for burst renewal shall be 5E−7 or less (i.e. one error burst restart per 2 million error captures).

The following is an example analysis:

No burst restart: captured_data[31:0]=00000000000000000000001111111111

Burst restart: captured_data[31:0]=00000000000000000000111001111111

where '1' represents a bit error and '0' represents a correct bit, as expected from "exclusive or" (XOR) operation between the received bits and the synchronized reference PRBS31 pattern. Captured_data[0] corresponds to the error event trigger.

Note: A burst of errors contains 1 or more consecutive bit errors.

6.1.2.5.2.5 Noise Contributed by Integrated Return Loss (NRL)

This section will be added in a future ECN.

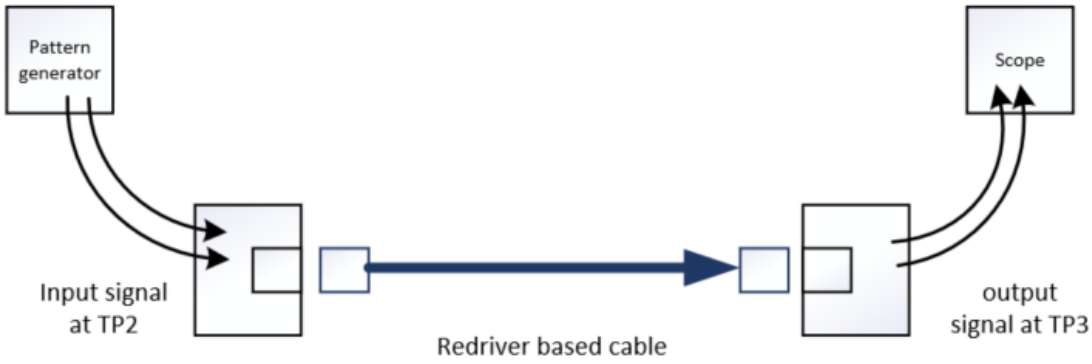
6.1.2.5.3 LRD-based Active Cable Electrical Requirements

LRD-based (LRD-based) active cables shall be tested as a complete component for compliance.

An LRD-based active cable is expected to receive a reference signal (referenced to TP2) defined in this specification and output a signal at the other end with electrical characterization that meets the requirements (referenced to TP3).

As shown in Figure 6-27, a compliant USB Type-C receptacle shall be connected to both ends of the active cable for injecting and measuring the signal to the corresponding TP2 and TP3 reference points. Details of the Compliance Receptacle and boards can be found in Section 3.3.6 of *USB4* Specification.

Figure 6-27 LRD-based Active Cable Compliance Setup



Note: The internal placement of the LRD ICs is purposely not specified to allow full flexibility to the manufacture to develop various LRD-based solutions.

6.1.2.5.3.1 General Implementation Notes

This specification was developed considering electrical interoperability with legacy systems, as the LRD-based Active Cables were added to the USB ecosystem in a late phase when a lot of devices were already in the field.

The USB Type-C interconnect ecosystem assumes the worst case 1 m/2 m/0.8 m passive cable is the worst-case connection (for *USB 3.2*, *USB4* Gen2 and *USB4* Gen3 respectively).

The intent is to align the LRD-based Active-Cable specifications to the existing passive cable specifications defined in Chapter 3 of this specification, such that the LRD-based active cable characteristics will be equal or better than those of the worst-case passive cable. The worst-case passive cable is defined in the *USB 3.2* and *USB4* Compliance Test Specification (CTS). This specification will define the electrical characteristics of the LRD-based cable that shall meet this requirement.

The LRD-based active cable specification assumes no change is needed to the existing TX/RX specification of the endpoint PHYs so that compatibility to existing certified *USB 3.2* and *USB4* devices is maintained.

For the Gen4 update to the *USB4* specification, LRD-based cable technology was considered, and all TX/RX implications are implicitly comprehended in the base specification.

Given this background, the following are assumptions regarding the LRD-based active cable implementation:

1. LRD-based active cable is assumed to have no clock mechanism in its datapath (such as CDR).
2. For *USB 3.2* Gen2 and *USB4* Gen2/3, LRD-based active cable is assumed to not have a dynamic amplitude control (such as AGC) to avoid masking the txffe training from the receiver.
3. For *USB4* Gen4, it is a valid implementation choice to include AGC in the cable, however the time which this AGC can be enabled is limited to tLRDSelfTune which defined in this spec at 6.1.2.5.3.13
4. LRD-based active cable is assumed to not use the training patterns to train itself, especially it is assumed to not block the output data during any phase of the training period.
5. Receiver systems rely on the low-pass-filter nature of the cable and having an over-equalized cable (i.e. weak LPF characteristic) can lead to interoperability issues. Therefore, it is recommended that when developing an LRD-based active cable, the cable should be built and tuned in a way that will make it the most passive-cable-like as opposed to most equalized cable.
6. During the development of the USB4-Gen4 LRD cable we used a set of design assumptions that can be found in Appendix J of this document

6.1.2.5.3.2 USB4 LRD-based Active Cable Compliance Testing

Table 6-28 defines the *USB4* LRD-based active cable specifications for *USB 3.2* and for *USB4* Gen2, Gen3 and Gen4 systems at TP3.

These parameters shall be measured at the LRD-based active cable's output while applying a reference signal at the input as specified in Table 6-29.

An LRD-based active cable shall be tested by injecting several patterns, calibrated to TP2.

Table 6-28 LRD-based Active Cable Output Parameters

Symbol	Description	Min	Max	Units	Conditions
$ILfitatDC$	Defining the ILfit mask for the cable response. Note: The main intention is to keep the cable with LPF characteristic similar to the passive cable. Note: Not applicable to USB4 Gen4, see 6.1.2.5.3.11.	ILfitatNq+1.5 USB4 Gen2: -5dB	0	dB	See 6.1.2.5.3.4
$ILfitatf1$		$ILfitatNq$	$ILfitatDC$	dB	See 6.1.2.5.3.4
$ILfitatNq$		USB 3.2: −6 USB4 Gen2: −12 USB4 Gen3: −7.5	ILfitatDC − 1.5	dB	See 6.1.2.5.3.4
$ILfitatf2$		$ILfitatNq - 3$	$ILfitatNq$	dB	See 6.1.2.5.3.4
$ILfitatf3$		$ILfitatf2 - 4$	$ILfitatf2$	dB	See 6.1.2.5.3.4
$ILfitatWB$	Max gain of the cable in the range of DC to f_N		0	dB	See 6.1.2.5.3.4
OUTPUT_NOISE	Standard deviation of the cable output noise. Combination of all noises beside the non-linearity noise.	See 6.1.2.5.3.2	mV		See 6.1.2.5.3.5
SIGMA_E	Standard deviation of the Non-linearity noise measured in the cable output	USB 3.2, USB4 Gen2/3: 15	mV		See 6.1.2.5.3.6
CABLE_SNDR	Signal to non-linearity noise ratio in the cable output	USB4 Gen4: TBD	dB		See 6.1.2.5.3.6
Operating margin	Receiver margin evaluation	USB4 Gen3: 3 USB4 Gen4: 0		dB	See 6.1.2.5.3.10 normative only for USB4 Gen3 and Gen4
Eye mask	Eye mask in the cable output				See 6.1.2.5.3.10
CM_NOISE	Common mode noise		100	mV pp	See 6.1.2.5.3.12
IRL	Integrated Return Loss				See 6.1.2.5.3.7
IMR	Integrated multi-reflection (integration of ILD (Insertion loss deviation))				See 6.1.2.5.3.8

Table 6-29 Input Signal at TP2 for Compliance Testing

Pattern (defined in USB4 Specification 8.3.2.1.1)	Swing (reference to TP2)	Added Jitter	TX Equalization	SSC	Minimum Measurement Time	Usage
PRBS15	800 mV p-p	No	No EQ	No	20 µs	Cable gain, non-linearity noise
PRBS15	USB4: 1300 mV p-p USB 3.2: 1200 mV p-p	No	No EQ	No	20 µs	Non-linearity noise
PRTS7	800 mV p-p	No	No EQ	No	20 µs	Cable gain, non-linearity noise (Gen4)
PRTS7	1000 mV p-p	No	No EQ	No	20 µs	Non-linearity noise (Gen4)
SQ512	300 mV p-p	No	NoEQ	No	20 µs	Output noise
PRBS31	As defined in USB4 Specification and CTS					Eye mask at TP3

6.1.2.5.3.3 Measurement Methods

The compliance testing of an LRD-based active cable to this specification will be done based on measurements from both time and frequency domains.

For all time domain specification items, the measured LRD-based active cable parameters will be compared to the worst-case passive cable supported in each technology (with nominal cable length of 1 m for USB 3.2, 2 m for USB4 Gen2 and 0.8 m for USB4 Gen3) measured in the exact same setup to reduce testing complexity. The worst-case passive cable is defined in the active cable CTS.

For USB4 Gen4, the measurements will be against absolute values and not referenced to the worst-case passive cable.

More details on the measurement methods can be found in the active cable CTS.

6.1.2.5.3.4 Cable ILfit Mask (DC/f1/Nq/f2/f3/WB) for USB 3.2 and USB4 Gen2/3

Based on the pulse response extraction from the time domain measurements, $(h(n))$ Fourier Transform is used to extract the impulse frequency response $H_{impulse}(f)$. For the specification parameters calculation, a fitted version of $H_{impulse}(f)$ shall be used. The pulse extraction and fitting methods are detailed in the active cable CTS and in Appendix G of this document.

$$ILfitatDC = 20 * \log_{10}(ILfit(DC))$$
$$ILfitatf_1 = 20 * \log_{10}(ILfit(f_1))$$
$$ILfitatf_N = 20 * \log_{10}(ILfit(f_N))$$
$$ILfitatf_2 = 20 * \log_{10}(ILfit(f_2))$$
$$ILfitatf_3 = 20 * \log_{10}(ILfit(f_3))$$
$$ILfitat\mathrm{WB} = \max\left(20 \cdot \log_{10}\left(ILfit(f_0)\right)\right), where\ f_0\ is\ in\ the\ range\ of\ DC\ to\ f_N$$

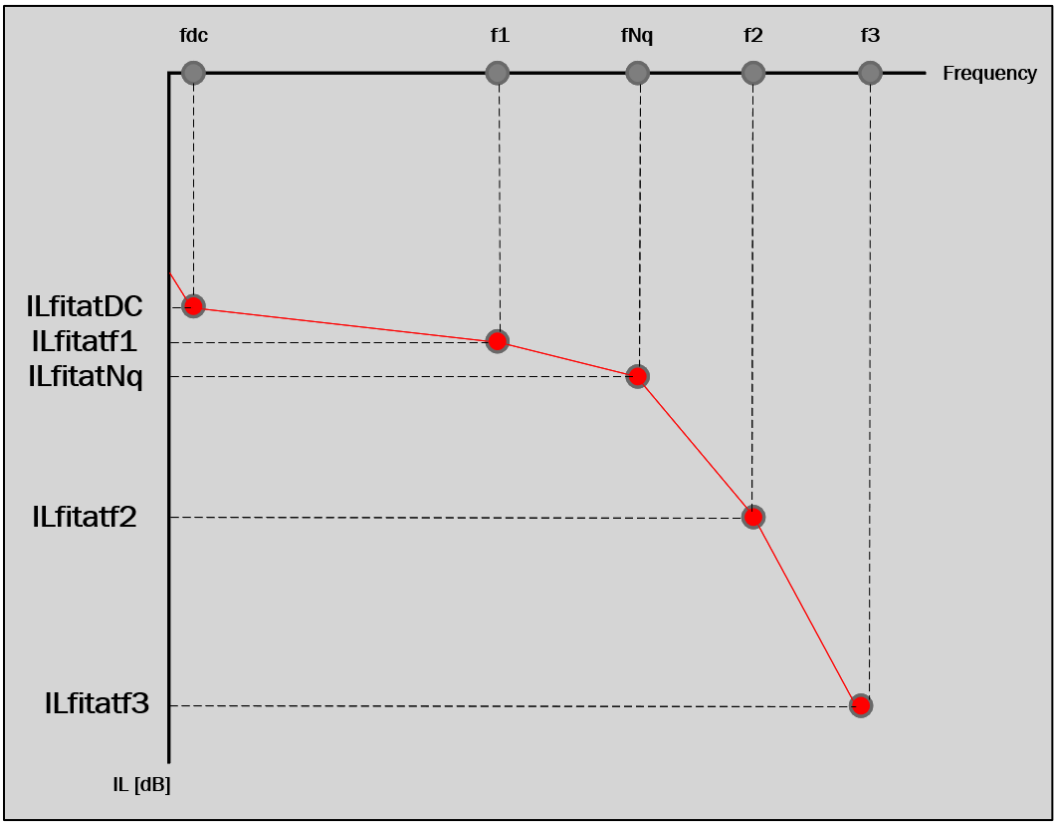
$$DC = 100\ MHz$$

$$f_1 = f_N * 0.7$$
$$f_2 = f_N * 1.25$$

$$f_3 = f_N * 1.5$$

$$f_N\ for\ USB3.2: 5\ GHz$$
$$f_N\ for\ USB4\ Gen2: 5\ GHz$$
$$f_N\ for\ USB4\ Gen3: 10\ GHz$$

Figure 6-28 Gain Parameters for USB 3.2 and USB4 Gen2/3 LRD Active Cables



6.1.2.5.3.5 OUTPUT_NOISE (σ_n)

σ_n is the standard deviation of the uncorrelated additive noise added to the output signal of the LRD-based active cable.

To achieve an accurate measurement, the calculation will be done based on a low frequency signal (SQ512 pattern) applied to the cable input, with 0.3 Vpp amplitude.

Since the noise calculation is referred to the receiver input, a 2nd order Butterworth LPF filter with −2 dB @ Nq shall be applied on the captured wave to account for the receiver BW and device side platform.

For *USB 3.2* and *USB4* Gen2/3, the limit of OUTPUT_NOISE is defined as function of the IL at Nyquist frequency. This allows a degree of freedom to the cable developer to trade between the cable's gain and noise.

The limit is defined as:

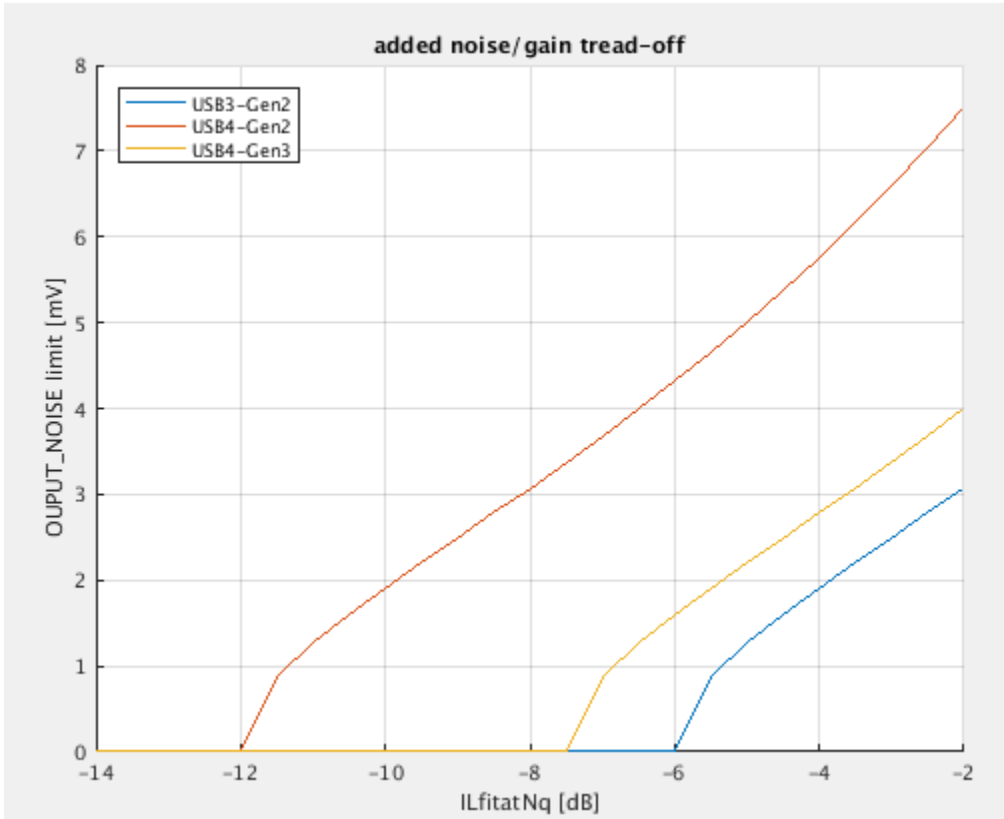
$$\sigma_{cable} \leq \sqrt{\frac{\sigma_1^2}{10^{\frac{H(f_N)_{PC}-H(f_N)_{RC}}{10}}} - \sigma_1^2} \cdot \frac{1}{\alpha}$$

Using the following parameters:

σ_1	2 mV
α	0.9
$H_{PC}(f_N)$	*USB 3.2*: −6 dB *USB4* Gen2: −12 dB *USB4* Gen3: −7.5 dB

Figure 6-29 shows a graph of this function for the given parameters.

Figure 6-29 OUTPUT_NOISE Limit Versus *ILfitatNq*



~~For USB4 Gen4, the limit of OUTPUT_NOISE is fixed and set to 1.2 mV RMS.~~[CK2]

6.1.2.5.3.6 SIGMA_E (σ_e)

σ_e is the standard deviation of the non-linearity related noise added by the LRD-based active cable.

This measurement shall be performed twice: once with minimum input swing and once with maximum input swing.

Then, $\sigma_e = \max(\sigma_{e\,\max swing}, \sigma_{e\,\min swing})$.

where:

maximum input $swing = 1300mVpp\ (USB4\ Gen2/3), 1200mVpp\ (USB3.2)\ or\ 1000mVpp\ (USB4\ Gen4)$
Minimum $input\ swing = 800mVpp$
$(compatible\ with\ USB\ 3.2/USB4\ specification\ \max swing\ definition)$

For USB4-Gen4, CABLE_SNDR results should be further calculated as:

$$CableSNDR = db\left(\frac{PulseResponsePeack}{sqrt(C_e \cdot \sigma_e^2 + C_n \cdot \sigma_N^2)}\right)$$

The value of $C_e and\ C_n$ is still TBD and will be added in another ECR soon.

More details on the calculation of the non-linearity noise can be found in the Active Cable CTS and in Appendix G of this document.

6.1.2.5.3.7 Integrated Return-Loss (IRL)

The IRL term for an LRD-based active cable is calculated similarly to the passive cable, see 3.7.2.3.1.

The IRL limit is different for LRD-based active cables and is given by the following functions:

Mode:	IRL Limit:
USB 3.2 Gen2	$IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 8.784$
USB4 Gen2	$IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 8.784$
USB4 Gen3	$if(-4dB \leq ILfit@Nq)$: $IRL \leq -13dB$ $if(ILfit@Nq < -4dB)$: $IRL \leq ILfit@Nq - 9$
USB4 Gen4	still TBD and will be added in another ECR soon

6.1.2.5.3.8 Integrated Multi-Reflection (IMR)

The IMR term for an LRD-based active cable is calculated similarly to the passive cable, see 3.7.2.3.2.

The IMR limit is different for LRD-based active cables and is given by the following functions:

Mode:	IRL Limit:
USB 3.2 Gen2	$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 20.392$
USB4 Gen2	$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 20.392$
USB4 Gen3	$if(-4dB \leq ILfit@Nq)$: $IMR \leq -29dB$ $if(ILfit@Nq < -4dB)$: $IMR \leq 1.741 \cdot ILfit@Nq - 22.143$
USB4 Gen4	still TBD and will be added in another ECR soon

6.1.2.5.3.9 Evaluating Channel Operation Margin (COM)

For USB4 Gen3, Channel Operating Margin (COM) shall be calculated for LRD-based active cables supporting USB4 Gen3, for evaluating a reference receiver margin based on the cable's measured S parameters.

The measurements of the cable and the setting of the associated COM tool is defined in the Active Cable CTS.

For USB4 Gen4, the Channel Operating Margin shall be calculated with the eCOM tool instead of the standard COM tool.

6.1.2.5.3.10 Cable Output Eye Mask

An LRD-based active cable shall meet the eye mask limits at its output.

The test setup shall be identical to the USB 3.2 and USB4 calibrated receiver test which includes worst case passive cable.

During the test, a reference CTLE, DFE and TXFFE settings shall be tuned according to the *USB 3.2* /*USB4* spec for obtaining the optimal eye.

1. *USB 3.2* have fixed TXFFE setting according to the *USB 3.2* Gen2 TX specification.
2. *USB4* can tune the TXFFE according to the TXFFE preset table in *USB4* Specification Table 3-5.

After obtaining the optimal eye with the passive cable, repeat the same measurement with the LRD cable under test, and compare the extracted eyes.

For *USB 3.2* and *USB4* Gen2/3, the optimal LRD cable eye shall meet these criteria:

$$LRD\ cable\ eye\ area \geq Passive\ cable\ eye\ area$$
$$\text{AND}$$
$$LRD\ cable\ eye\ width > 0.9 * \ Passive\ cable\ eye\ width$$

For *USB4* Gen4, the optimal LRD cable eye shall meet the limits as defined in the CTS.

Note that the maximum eye height is constrained by the spec item $ILfitatWB$ that prevent active amplification over the entire frequency range.

6.1.2.5.3.11 USB4 Gen4 ILfitMask Limits

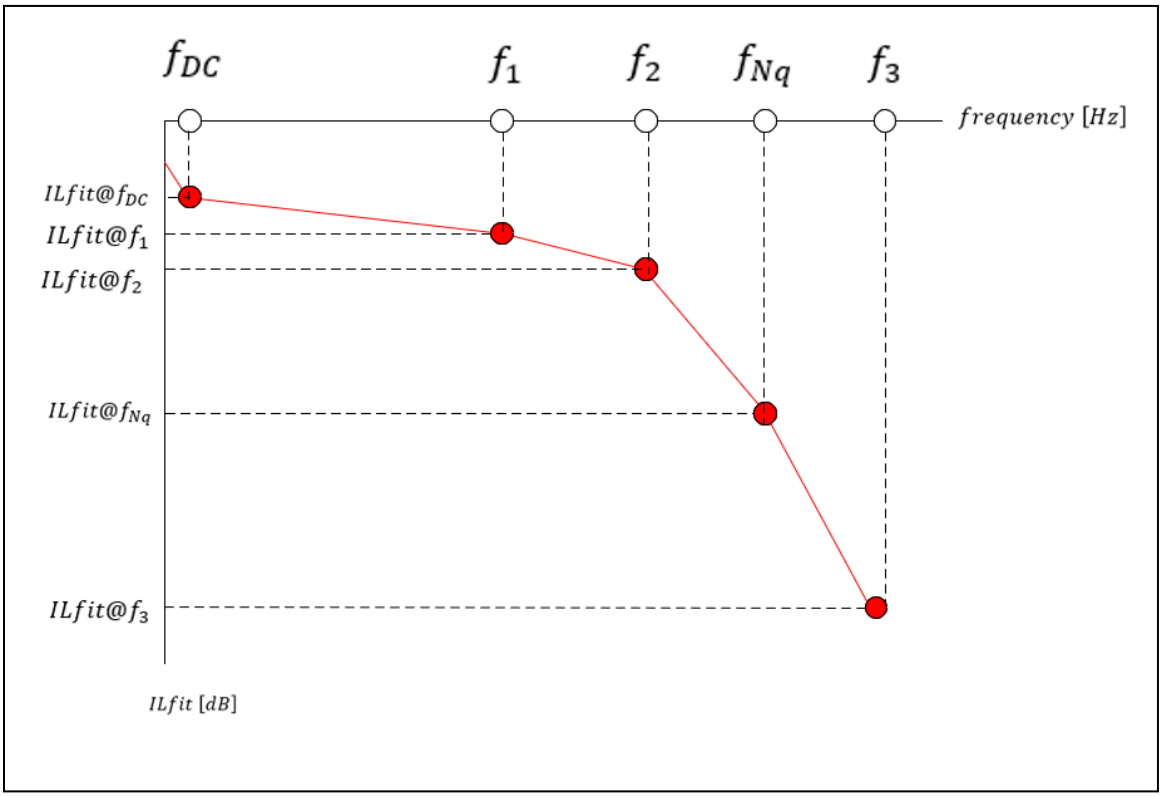
The ILfitMask for an LRD-based active cable supporting USB4 Gen4 is defined in Table 6-xx.

Table 6-xx USB4 Gen4 LRD-based Active Cable ILfitMask Limits

Symbol	Frequency	Min	Max	Units
$ILfitatDC$	100 MHz	$-3\ [TBD]$	0	dB
$ILfitatf1$	$0.7 * fNq$	$ILfitatf2$	$ILfitatDC$	dB
$ILfitatf2$	$0.85 * fNq$	$ILfitatNq$	$ILfitatf1$	dB
$ILfitatNq$	12.8 GHz	$ILfitatDC - 7.5$	$ILfitatDC - 3$	dB
$ILfitatf3$	$1.2 * fNq$	$ILfitatNq - 4\ [TBD]$	$ILfitatNq$	dB

This mask shall be met for any TXFFE setting in the cable input, and for minimum and maximum swing level in the TX.

Figure 6-28 Gain Parameters for USB4 Gen4 LRD Active Cables



6.1.2.5.3.12 Cable CM_NOISE

CM_NOISE is defined as the maximum peak value of the signal captured in the cable output with common mode setting on the scope (p+n) and prbs15 data pattern.

The CM_NOISE shall not exceed 100mV.

6.1.2.5.3.13 Self Gain Tuning Capabilities in USB4 Gen4 LRD Cables

For the *USB4* Gen4 rate, the cable can tune its own gain to the optimal settings depend on the incoming signal. Refer to 6.1.2.5.3.17.2 Phase 4 and Phase 5 for details on when the cable may tune its gain.

tLRDSelfTune is defined to be 250 µs.

After that period the LRD response shall be fixed.

Note: this self-tune ability is for gain only, the EQ response shall be fixed for all input (see more on the ILfitMask for *USB4* Gen4 in 6.1.2.5.3.4).

Section 6.1.2.5.3.16 defines how the cable snoops and adjusts its gain.

6.1.2.5.3.14 USB4 Gen4 Lane Direction Change

LRD-based active cables that support *USB4* Gen4 shall support the asymmetric mode as defined in *USB4* specification (Section 4.2.2.5) and the LRD_Tuning.Force_Lane_Reversal for cable compliance . That mean that each high-speed pair of the cable (TX0/TX1/RX0/RX1) shall be able to operate in both directions.

The cable shall follow 6.1.2.5.3.17.7 and 6.1.2.5.3.17.8 when switching into and out of asymmetric mode.

6.1.2.5.3.15 LRD Active Cable Logical Layer Wiring Diagram

The LRD active cable shall follow the wiring diagram as indicated in Table 6-xx. The assumption in this table is that there is an LRD in each cable plug.

Table 6-xx USB4 Gen4 LRD Active Cable Wiring Diagram for Compliance

USB Type-C Plug #1		Cable Connection			USB Type-C Plug #2	
Pin	Signal Name				Pin	Signal Name
A1, B1 A12, B12	GND	Fixed connection			A1, B1 A12, B12	GND
A4, B4, A9, B9	Vbus	Fixed connection			A4, B4, A9, B9	Vbus
A5	CC	Fixed connection			A5	CC
B5	Vconn	Ra to GND, Diode connection			B5	Vconn
A6	Dp1	←----------→			A6	Dp1
A7	Dn1	←----------→			A7	Dn1
A8	SBU1	Fixed connection			B8	SBU2
B8	SBU2	Fixed connection			A8	SBU1
Shell	Shield	Fixed connection, outer shield			Shell	Shield
Normal Operation or Compliance Force Lane Reversal = 0b						
		Symmetric Connection	**Enable3Tx Plug#1 Enable3Rx Plug#2**	**Enable3Rx Plug #1 Enable3Tx Plug #2**		
A2	TXp1_IN	----------LRD-----→	----------LRD-----→	----------LRD-----→	B11	RXp1_OUT
A3	TXn1_IN	----------LRD-----→	----------LRD-----→	----------LRD-----→	B10	RXn1_OUT
B11	RXp1_OUT	←--------LRD-------	←--------LRD-------	←--------LRD-------	A2	TXp1_IN
B10	RXp1_OUT	←--------LRD-------	←--------LRD-------	←--------LRD-------	A3	TXn1_IN
B2	TXp2_IN	----------LRD-----→	----------LRD-----→	←--------LRD-------	A11	RXp2_OUT

B3	TXn2_IN	----------LRD-----→	----------LRD-----→	←--------LRD-------	A10	RXn2_OUT
A11	RXp2_OUT	←--------LRD-------	----------LRD-----→	←--------LRD-------	B2	TXp2_IN
A10	RXn2_OUT	←--------LRD-------	----------LRD-----→	←--------LRD-------	B3	TXn2_IN
Compliance Force Lane Reversal =1b						
		Symmetric Connection	**Enable3Tx Plug#1 Enable3Rx Plug#2**	**Enable3Rx Plug #1 Enable3Tx Plug #2**		
A2	TXp1_IN	----------LRD-----→	----------LRD-----→	←---------LRD-----	B11	RXp1_OUT
A3	TXn1_IN	----------LRD-----→	----------LRD-----→	←---------LRD-----	B10	RXn1_OUT
B11	RXp1_OUT	←--------LRD-------	--------LRD-------→	←--------LRD-------	A2	TXp1_IN
B10	RXp1_OUT	←--------LRD-------	--------LRD-------→	←--------LRD-------	A3	TXn1_IN
B2	TXp2_IN	----------LRD-----→	----------LRD-----→	--------LRD------→	A11	RXp2_OUT
B3	TXn2_IN	----------LRD-----→	----------LRD-----→	--------LRD------→	A10	RXn2_OUT
A11	RXp2_OUT	←--------LRD-------	←---------LRD-----→	←--------LRD-------	B2	TXp2_IN
A10	RXn2_OUT	←--------LRD-------	←---------LRD-----→	←--------LRD-------	B3	TXn2_IN

Error! Reference source not found. defines the SBx transactions the LRD active cable is required to snoop and common optional SBx transactions which may be snooped. The LRD active cable may snoop more SBx transactions if desired. SBx transactions snooped on SBU1 have been transmitted from SBTX of the attached Router or Re-timer and may have an assumption of direction depending on the transaction.

Table 6-xx USB4 Active Cable SBx Transaction Snooping

Transaction Type	Symbol or Transaction Contents	Optional or Required?	Action
LT	LT_Fall	Required	Transition to CLd
	LT_Resume	Optional if LOS (loss of signal) is used	Transition to Forwarding
	LT_LROff	Required	Transition to CLd. Issued on Lane 0 but affects all both lanes.
	LT_SwitchRx2Tx	Required	Transition to/from Asymmetrical when snooped on SBU1
	LT_SwitchAck	Required	Transition to/from Asymmetrical when snooped on SBU1

	LT_Gen2	Optional if LOS is used	Transition to Forwarding. Optional to use specific gen2 fixed gain and equalization
	LT_Gen3	Optional if LOS is used	Transition to Forwarding. Optional to use specific gen3 fixed gain and equalization
RT broadcast	TBT3-CompatibleSpeed	Optional	Modify gain and equalization for TBT rates
	USB4	Required	0b – Use LT transactions for link training 1b – Use RT transactions for link training
	SelectedGen	Optional	Modify gain and equalization per data rate gen2, gen3, gen4
	Enable3Tx	Required	Asymmetrical Initial link training
	Enable3Rx	Required	Asymmetrical Initial link training
	Lane1Enabled	Optional if LOS is used	0b – CLd lane1 1b - Enable forwarding lane1
	Lane0Enabled	Optional if LOS is used	0b – CLd lane0 1b - Enable forwarding lane0
RT Addressed Index 0 to Gen4TxFFE	Partner_Tx_Status_Byte .TxFFE_Start	Optional	Adjustment of AGC is allowed
	Partner_Tx_Status_Byte .Request_Done		0b – Do not start AGC 1b – start AGC for tLRDSelfTune
RT Addressed Index 0 to LRD Tuning	Force Lane Reversal (bit 1)	Required	Required for Compliance Force Lane Reversal Optional to adjust gain and equalization in a TBD way
ELT	ELT_OpDone	Optional	No action
	ELT_Recovery	Required	Transition to Forwarding

6.1.2.5.3.16 USB4 and TBT Logical Layer

The LRD active cable shall determine its USB4 behavior based on snooping the RT broadcast (RTb) and RT addressed (RTa) transactions, the LT, and the ELT transactions.

6.1.2.5.3.17 USB4 and TBT Timing Parameters

The LRD active cable shall meet the timing requirements in Table 6-XX.

Table 6-xx USB4 LRD Active Cable Logical Timing Parameters

Parameters	Description	Min	Max	Units
tLRDForward	The amount of time the LRD takes to transition to Forwarding upon snooping Lane Enable.		1	ms
tLRDSwitch	The amount of time the LRD takes to switch direction after snooping LT_SwitchRX2TX or LT_SwitchAck and receiving no high speed data.		1	ms

6.1.2.5.3.17.1 USB4 and TBT USB-PD Mode Entry

This section defines the behavior of the LRD cable during the phases of link training.
The USB-PD controller shall use the information from the SOP' and SOP" (if present) Enter Mode to configure to the LRD to USB4/TBT.

6.1.2.5.3.17.2 USB4 and TBT Link Training

Phase 1: Receiver and Transmitter terminations are enabled. The common-mode voltage is unchanged. The LRD shall assume the Router far side termination is not present in this state. The Router may change its common-mode voltage with or without terminations present when transitioning to this state.
The USB-PD Controller informs the LRD in the active cable of the connection and mode.
Phase 2: No action
Phase 3: No action
Phase 4: Requirements
Snooping of any SBU transaction other than LT_Fall or LT_LRoff starts this phase. The LRD may change its common-mode voltage after snooping a LT or RT transaction. The LRD shall meet Vdc+ac-conn if changing its common-mode voltage when measured into a 50 Ohm load. The common-mode voltage ramp shall complete in tLaneParams minimum (USB4v2 Specification).
Note: Routers and Re-timers present terminations before transmitting LT or RT transactions.

1. TBT Legacy Requirements
    a. Snooped LT transactions on SBU1:
        i. LT_Gen2 and LT_Gen3: Set fixed gain and equalization. It is optional for the gain and equalization to change based on the speed indication. Enable forwarding if not already enabled.
        ii. LT_Resume: Enable forwarding if not already enabled.
    b. Snooped Broadcast RT transactions on SBU1:
        i. USB4: If the USB4 bit is set to 1b, addressed RT transactions are used for link training.
        ii. SelectedGen: Set fixed gain and equalization. It is optional for the gain and equalization to change based on the speed indication.

iii. Lane0Enabled, Lane1Enabled: Enable forwarding if not already enabled. Optional to use LOS to enable forwarding.

2. USB4
   a. Snooped Broadcast RT transactions on SBU1:
      i. USB4: If the USB4 bit is set to 1b, addressed RT transactions are used for link training.
      ii. SelectedGen: Set fixed gain and equalization. It is optional for the gain and equalization to be change based on the speed indication.
      iii. Lane0Enabled, Lane1Enabled: Enable forwarding if Enable3Tx or Enable3Rx are not enabled. The LRD shall enable forwarding in tLRDForward after snooping the Lane Enable. Optional to use LOS to enable forwarding.
      iv. Enable3Tx: Enable three transmitter and one receiver as defined in **Error! Reference source not found.**. Enable forwarding after the LRD has switched direction within tLRDSwitch.
      v. Enable3Rx: Enable three receivers and one transmitter as defined in Table 1. Enable forwarding after the LRD has switched direction within tLRDSwitch.
   b. Snooped Addressed RT transaction to SB Register Gen_4_TxFFE with Gen4TxFFE.Tx_Status_Byte.Start_TXFFE:
      i. If Gen4TxFFE.Tx_Status_Byte. Start_TXFFE (bit 7) =1b, the LRD may adjust its AGC in phase 5.
      ii. If Gen4TxFFE.Tx_Status_Byte.Start_TXFFE (bit 7) =0b, the LRD may not adjust its AGC in phase 5.
      iii. Note that the bytes in Gen4TxFFE.Tx_Status_Byte change if the link is initialized as an asymmetrical link. Refer to the USB4v2 Specification for details.
   c. Snooped addressed RT transaction to SB Register LRD_Tuning on SBU1:
      i. If LRD_Tuning.Force_Lane_Reversal=0b, use normal Lane1 and Lane2 operation relative to CC without changing the SBU1/2.
      ii. If LRD_Tuning.Force_Lane_Reversal=1b, swap Lane1 and Lane2 without changing the SBU1/2. The lane reversal shall complete within tLRDSelfTune.

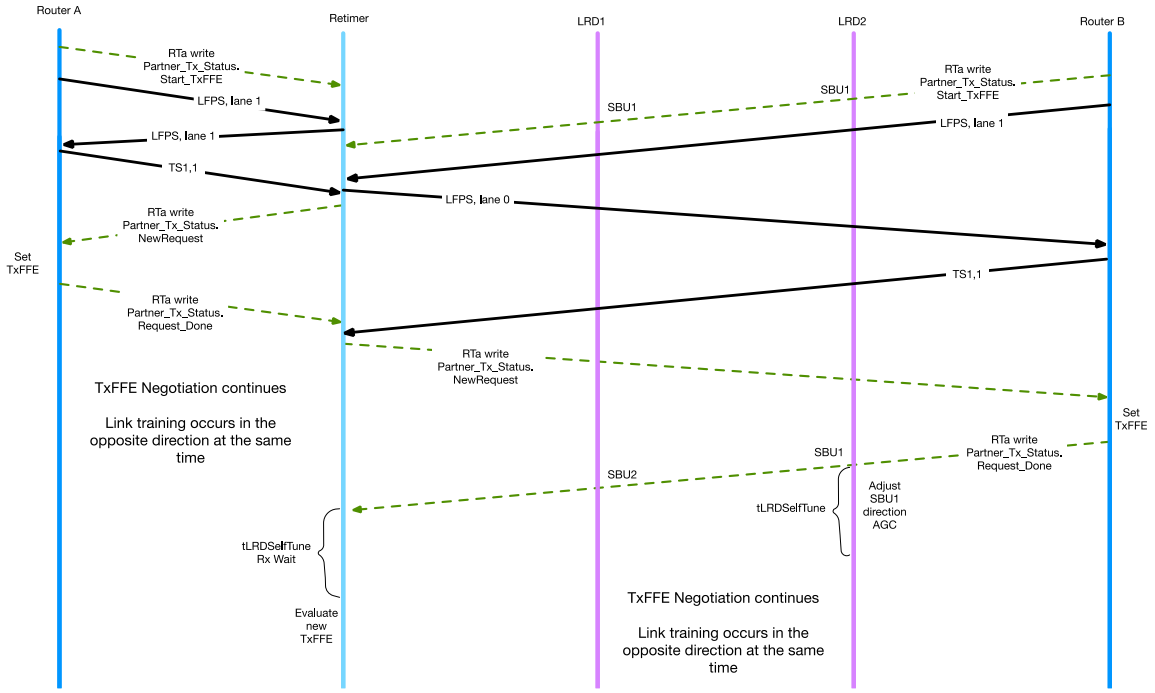
Phase 5: Requirements (only applies to USB4 Gen 4)

1. Snooped addressed RT transaction to SB Register Gen_4_TxFFE:
   a. Partner_Tx_Status_Byte.Request_Done (bit 6)=1b is the indication to the LRD to start the AGC training in the SBU1 to SBU2 direction.
   b. The LRD active cable AGC shall complete it adjustments within tLRDSelfTune. If there are two LRDs in the cable, each may be adjusted independently but tLRDSelfTune shall be met for the cable assembly.
2. Snooped addressed RT transaction to SB Register LRD_Tuning on SBU1:
   a. Optionally save the entire LRD_Tuning register. The LRD may optionally adjust its gain and equalization in a TBD way based on the contents of the register. The LRD shall complete its gain and equalization adjustment in tLRDSelfTune minimum time (USB4v2 Specification) when it snoops a write to LRD_Tuning.

An example of link training with LRD AGC adjustment is indicated in Figure 13.

Note: The LRD has no sideband indication of the switch from PAM2 to PAM3 and AGC and equalization training must function on both PAM2 and PAM3 incoming data.

Figure 13. USB4 LRD Active Cable Snooping of TxFFE Negotiation

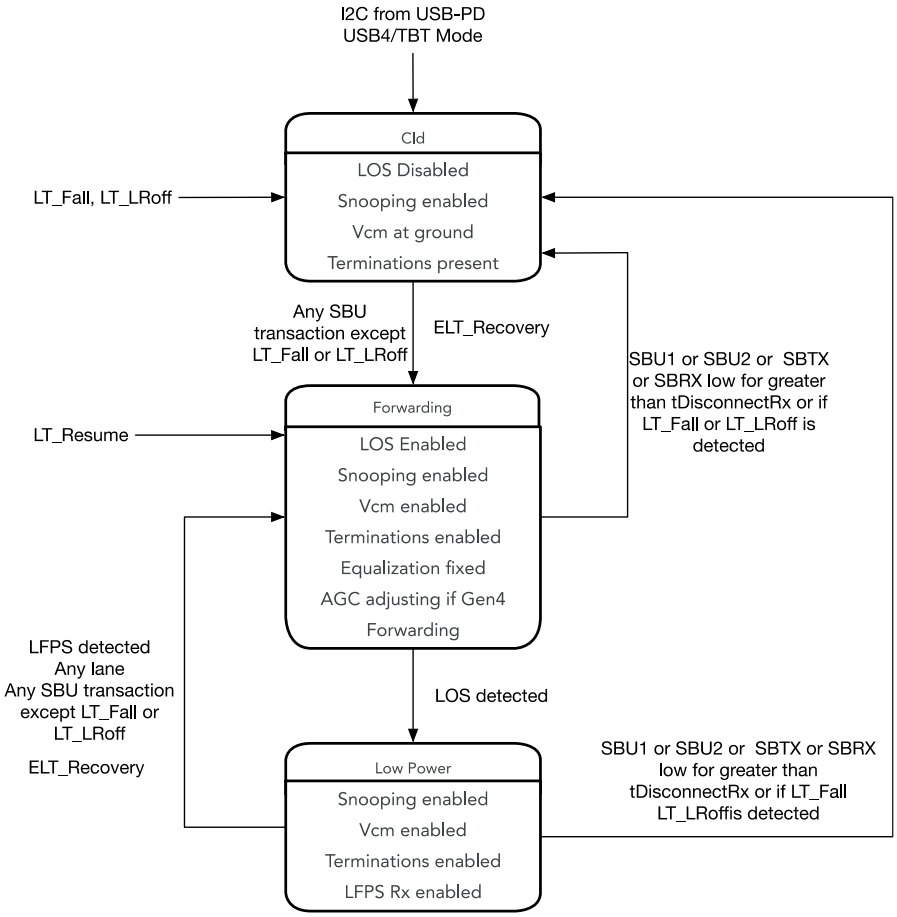


6.1.2.5.3.17.3 USB4 and TBT3 Logical Layer State Machine (Informative)

The state machine in Figure 14 describes the behavior of the Logical Layer of the LRD(s) in the active cable. The state machine is per channel (i.e., per direction per lane)

- CLd State – the LRD is disabled but snooping for any traffic on SBU1 (and optionally SBU2)
- Forwarding State – the LRD is forwarding. The LRD snoops the link characteristics on the RT broadcast transactions and adjusts its AGC if Gen4 and enabled.
- Low Power State – reduced power state

Figure 14. USB4 State Machine per Channel (Informative)



6.1.2.5.3.17.4 CLd State

Entry to State

The LRD shall enter this state on the following events:

- Entry to USB4/TBT3 Alt mode being set from the USB-PD Controller
- Snooping of LT_Fall or LT_LRoff transaction
- SBU1 or SBU2 low for greater than tDisconnectRx

Behavior in State

- LOS detector disabled
- SBU1 (and optionally SBU2) shall be snooped for activity
- The common mode voltage remains constant

- The 50 Ohm terminations are present on all Tx and Rx

Exit from State

- Transition to Forwarding State upon detection of SBU1 (and optionally SBU2) transaction which is not LT_Fall (per lane) or LT_LRoff (lane independent).
- Transition to Forwarding State upon detection of SBU1 (and optionally SBU2) ELT_Recovery.

6.1.2.5.3.17.5 Forwarding

Entry to State
The LRD shall enter this state on the following events:

- Any SBU1 (or optionally SBU2) transaction which is not LT_Fall or LT_LRoff
- After exiting Low Power state
- Snooping ELT_Recovery

Behavior in this state

- Enable the LOS receiver
- Snoop SBU1 (and optionally SBU2)
- Determine the direction of the lanes if USB4 gen4
- Ramp the common mode voltage if needed as defined in the link training
- Forward the high-speed data. Use last known AGC setting if the transition was from Low Power or ELT_Recovery
- Forward the high-speed data and adjust the AGC per Phase 4 and 5 Link training if gen4
- Forward the high-speed data and use the fixed stored AGC and EQ if gen2 or gen3

Exit from State

- Transition to CLd on detection of low on SBU1 (or optionally SBU2) for greater than tDisconnectRx or upon snooping LT_Fall or LT_LRoff.
- Transition to Low Power if LOS is detected

6.1.2.5.3.17.6 Low Power State

The Low Power state is used to conserve power in electrical idle.

Entry to State

- Transition to Low Power when detecting no high-speed signal on the Rx input

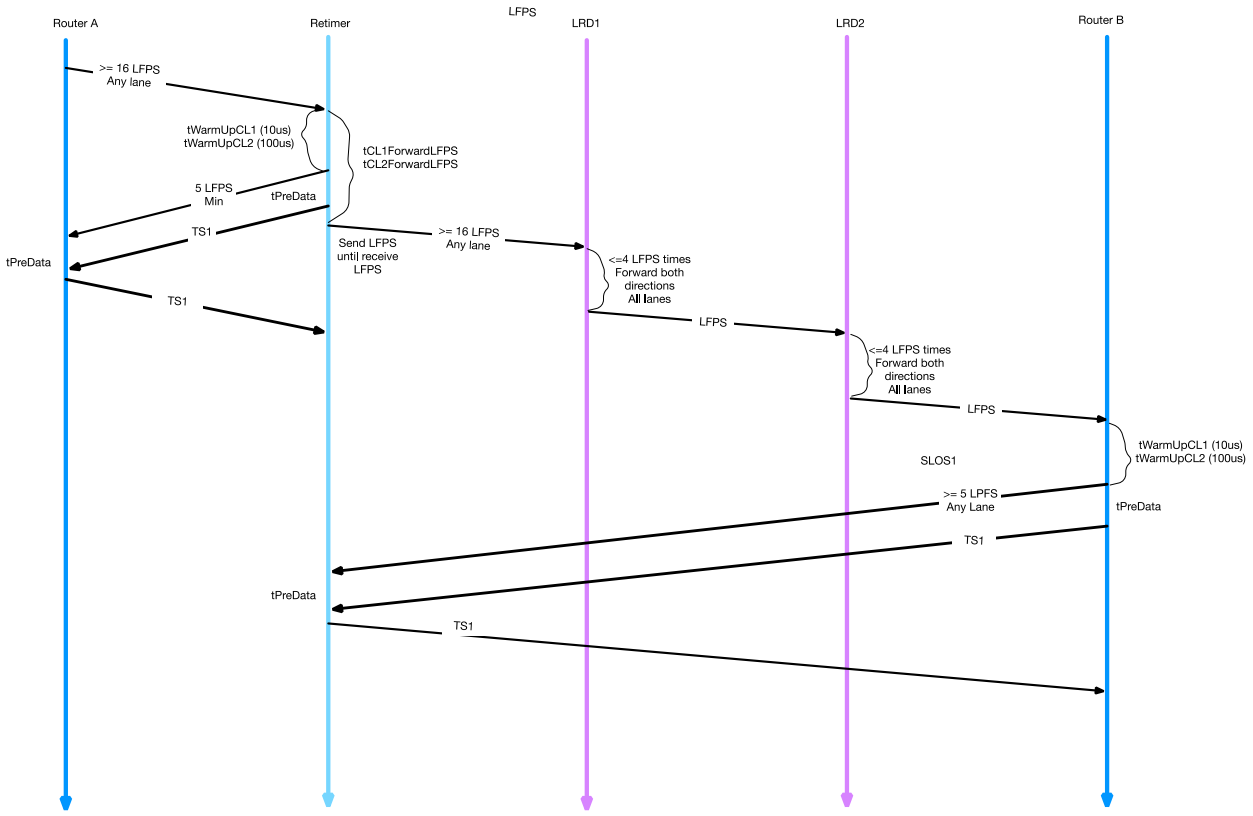
Behavior in this state

- Snoop SBU1 (and optionally SBU2)
- Common mode voltage shall be maintained
- Terminations shall be maintained
- Consume less power than in Forwarding

Exit from State

- Transition to Forwarding
  - Detection of LFPS on any channel shall transition the LRD to Forwarding on the channel receiving the LFPS and the channel in the same lane in the opposite direction. Note that LFPS may be on only one channel (one lane in one direction) if the link is in CL0s.
  - The LRD active cable shall consume a maximum of eight LFPS when transitioning to Forwarding.
  - The LRD shall not forward LFPS until it has enabled forwarding in both directions. Refer to Figure 15
  - Meet the electrical requirements when forwarding LFPS
  - Snoop of ELT_Recovery
- Transition to CLd
  - If SBU1 (or optionally SBU2) is low for greater than tDisconnectRx or if LT_Fall, or LT_LR_Off is detected
  - The transmitter and receiver shall maintain the common-mode voltage and terminations.

Figure 15. USB4 gen4 CL1/2 Exit Flow with LRD Active Cable

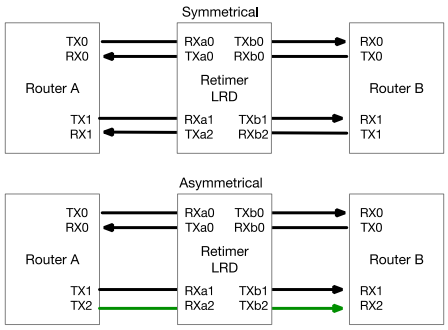


6.1.2.5.3.17.7 USB4 Gen4 Symmetrical to Asymmetrical Transitions

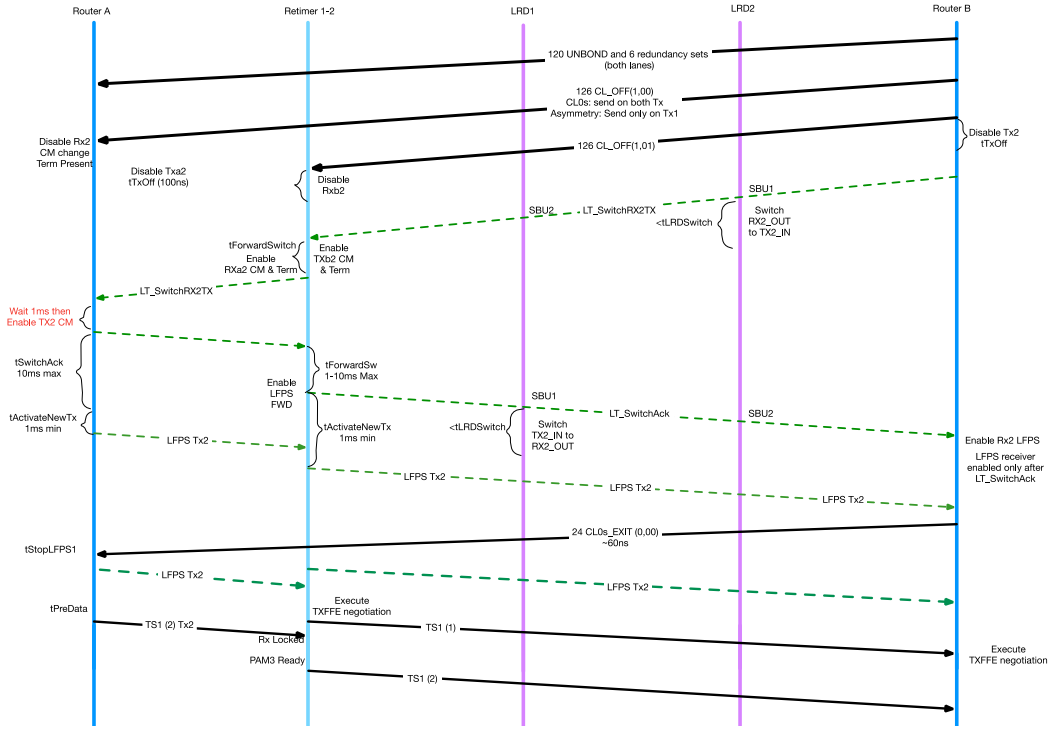
- **Error! Reference source not found.** provides an example of the Symmetric to Asymmetric flow for an LRD active cable.
- The LRD transitions from symmetrical to asymmetrical when it snoops the LT_SwitchRX2TX or LT_SwitchACK on SBU1.
- The LRD switches its RX2_OUT to a TX2_IN on receipt of the LT_SwitchRX2TX on SBU1.
- The LRD shall check for high-speed signal when receiving the LT_SwitchRX2TX. If high speed signal is detected by the LRD on the lane which will switch direction, the LRD shall wait for no high-speed signal and then perform the direction switch within tLRDSwitch. The LRD shall assume this is a transition to Asymmetrical because the previous state was Symmetrical.
- The LRD switches its TX2_Out to RX2_IN on receipt of the LT_SwitchACK on SBU1 within tLRDSwitch. The LRD transmitter and receiver shall modify their common-mode voltage after receipt of the LT_SwitchRX2TX or LT_SwitchACK if needed. The transmitter and receiver shall not exceed the V_DC_AC_CONN during the transition assuming the far side termination present. The transmitter and receiver shall apply terminations after the common-mode voltage ramp if the termination was removed during the common-mode ramp.
- The LRD shall not forward LFPS until it has completed direction switching.

  Note that if no LT_SwitchACK is received within 1s, the Link will disconnect by pulling SBTX low tDisconnectTx.

Figure 16. Symmetrical to Asymmetrical Transition



Switching from Symmetrical to Asymmetrical



6.1.2.5.3.17.8 USB4 Gen4 Asymmetrical to Symmetrical

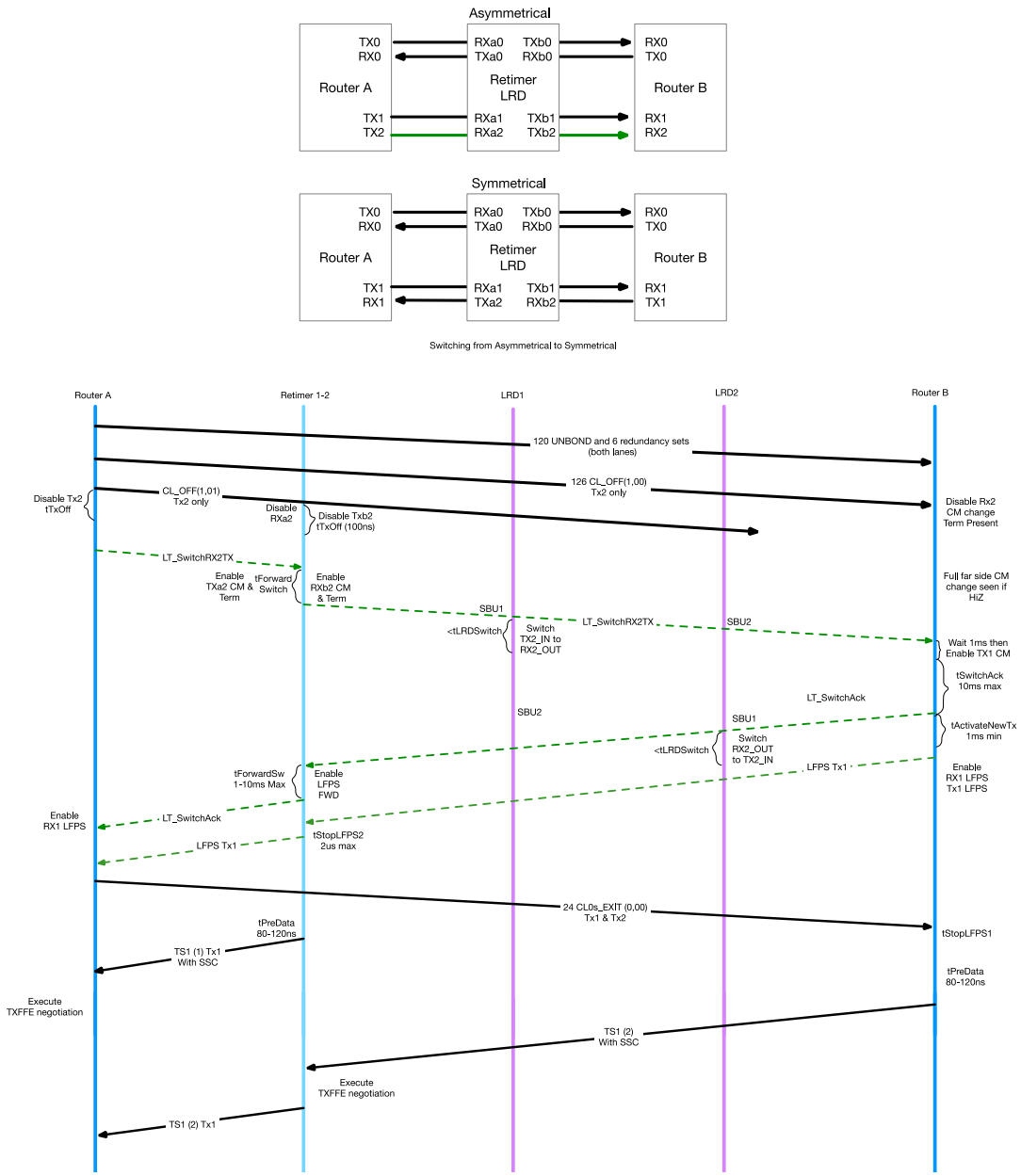
- Figure 17 provides an example of the Asymmetric to Symmetric flow for an LRD active cable.
- The LRD transitions from asymmetrical to symmetrical when it snoops LT_SwitchRX2TX or LT_SwitchACK on SBU1.
- The LRD switches its TX2_OUT to a RX_IN on receipt of the LT_SwitchRX2TX on SBU1.
- The LRD shall check for high-speed signal when receiving the LT_SwitchRX2TX. If high speed signal is detected by the LRD on the lane which will switch direction, the LRD shall wait for no high-speed signal and then perform the direction switch within tLRDSwitch. The LRD shall assume this is a transition to Symmetrical because the previous state was Asymmetrical.
- The LRD switches its RX2_Out to TX2_IN on receipt of the LT_SwitchACK on SBU1 within tLRDSwitch. The LRD transmitter and receiver may ramp their common-mode voltage after receipt of the LT_SwitchRX2TX or LT_SwitchACK if needed. The transmitter and receiver shall not exceed the V_DC_AC_CONN during the transition assuming the far side termination present. The transmitter and

receiver shall apply terminations after the common-mode voltage ramp if the termination was removed during the common-mode ramp.

- The LRD shall not forward LFPS until it has completed direction switching.

  Note that if no LT_SwitchACK is received within 1s, the Link will disconnect by pulling SBTX low tDisconnectTx.

Figure 17. Asymmetrical to Symmetrical Transition



6.1.2.5.3.18 Cable Compliance

The LRD in the active cable shall support snooping the LRD Tuning register as defined in Table 16. The Compliance Software only writes to the LRD Tuning Register if it needs to swap Lane1 and Lane2 in the active cable. The Compliance Software first writes to the Router LRD Tuning Register to

set Force Lane Reversal=1b with Response Request=1b. The connected Router will then write to the LRD Turning register in the test equipment with the same Force Lane Reversal=1b with Response Request=0. This allows LRD active cables which only snoop SBU1 to snoop the LRD Tuning Register write on the cable plug farthest from the Compliance Software and test equipment.

The Compliance Software then writes to the LRD Tuning register to set Force Lane Reversal=1b with Response Request=0b to inform the local cable plug.

The active cable shall switch back to normal Lane1 and Lane2 operation on disconnect.

Table 16. LRD Tuning Register Snooping

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
7	LRD Tuning	0	0	**Response Request** – When this bit is set to 1b, the USB4 Port shall send a write Command to the LRD Tuning register in the adjacent Router/Re-timer. The write shall contain the values of the local LRD Tuning register and shall have the Response Request bit set to 0b. The USB4 Port shall then set this bit to 0b.	R	0
			1	**Force Lane Reversal** – Identifies whether to override the functional Lane Reversal. 0b: Cable shall use normal Lane1 and Lane2 operation relative to CC 1b: Cable shall swap Lane1 and Lane2 *Note: Sideband SBU1 and SBU2 shall remain in normal orientation regardless of the Force Lane Reversal setting.*	R	0

6.1.2.6 Return Loss

Return loss is defined in the *USB 3.2* specification.

6.1.3 Mechanical

All active cables shall meet the mechanical requirements defined in the Section 3.8.

6.1.3.1 Thermal

6.1.3.1.1 Thermal Shutdown

All active cables shall implement a temperature sensor and place the *USB 3.2* signals in the eSS.Disabled state when the plug skin temperature reaches the maximum defined in Table 6-15. Active cables shall indicate they are in thermal shutdown if queried via the *USB PD* ***Get_Status*** command.

The Thermal Shutdown is cleared by the following events:

- Disconnect
- *USB PD* Hard Reset

6.1.3.1.2 Maximum Skin Temperature

Active cable plug's skin temperature shall not exceed a maximum operating temperature of 30 °C above the ambient temperature for a plastic/rubber housing and 15 °C for a metal housing in any operating mode.

6.1.3.1.3 Thermal Reporting

Active cables shall implement reporting their maximum internal operating temperature in the *USB PD* ***Discover_ID*** Command. Active cables shall implement reporting their current internal operating temperature in the *USB PD* ***Get_Status*** Command on SOP' and SOP" when supported. Active cables shall update their reported Internal Temperature at least every 500 ms.

The plug's Internal Temperature is reported in °C and shall be monotonic. It is not the plug's skin temperature, but cable manufacturers shall correlate the maximum internal operating temperature with the maximum plug skin temperature to ensure shutdown when the maximum plug skin temperature is reached.

Sources and/or Sinks may take action to reduce VBUS current to reduce the cable plug internal operating temperature to below the reported maximum operating temperature. It is recommended Sources and/or Sinks poll the plug's Internal Temperature every 2 seconds.

Table 6-15 Cable Temperature Requirements

Temperature Requirements	
Maximum Internal to Skin Temperature Offset	Design Specific
Maximum Internal Operating Temperature	Design Specific
Maximum Skin Temperature Plastic/Rubber[1]	80 °C
Maximum Skin Temperature Metal[1]	55 °C

Note 1: IEC 60950-1 reduced by 5 °C

6.1.3.2 Plug Spacing

Active cables will support the USB Type-C vertical and horizontal spacing defined Section 3.10.2 when functioning in *USB 3.2* x1 operation. However, this spacing may impose thermal constraints. Appendix D provides system design guidance to minimize the thermal impact due to connector spacing. It is recommended that products designed for *USB 3.2* x2 operation with multiple adjacent USB Type-C connectors follow the design guidance in Appendix D to minimize the likelihood the active cable will go into thermal shutdown.

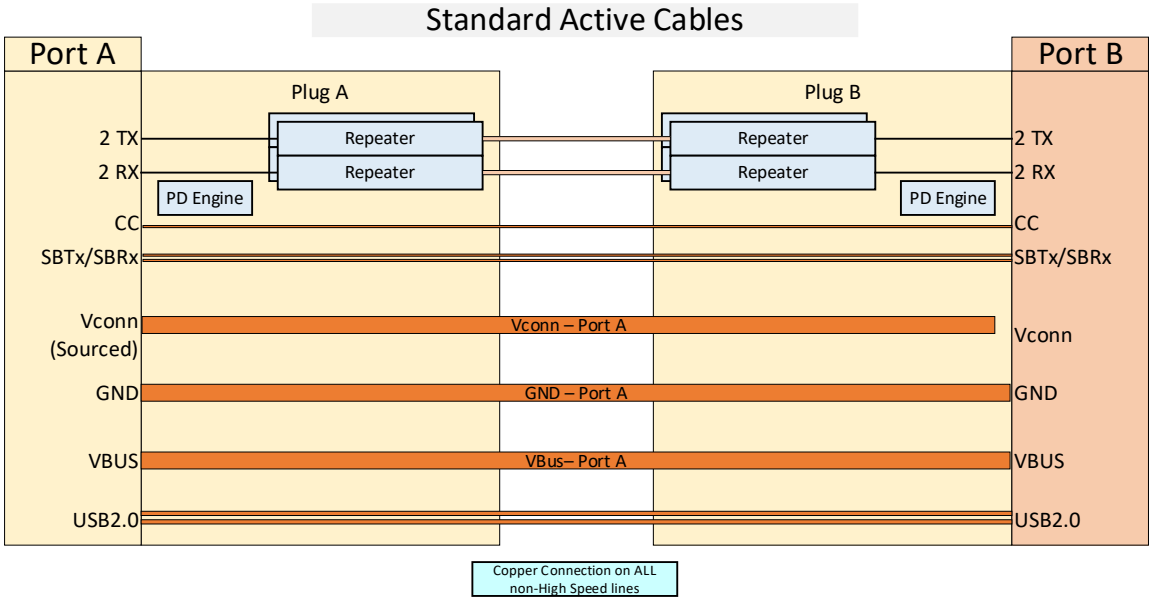
6.2 Active Cables

Active cables defines all active element cables including retimer, redriver and hybrid optical based cables. Hybrid Optical active cables use copper for power and low-speed data and optical for high-speed data.

Active cables minimally support *USB 3.2* Gen 2x2. *USB4* active cables support ~~all *USB 3.2* rates and *USB4*~~ as well as all *USB 3.2* rates.

All *USB4™* active cables shall be interoperable with Thunderbolt™ 3 as defined in the *USB4* Specification.

6.2.1 Active Cable Block Diagrams



6.2.2 Asymmetric Mode (3x1) in USB4v2

All Active Cables ***SHALL*** support Asymmetric Mode (3x1) in USB4v2. The ONLY exception is the OIAC defined in Section 6.3. This is reported in the Active Cable VDO2.

6.2.3 Active Cable USB PD Requirements

Active cables shall support *USB PD* Revision 3, Version 1.2 or later. Active cables shall support *USB PD* Structured VDMs.

6.2.3.1 SOP' and SOP" Requirements

SOP' and SOP" are fixed in the active cable at the time of manufacture. [LE3]

Active cables shall respond to ***Discover_Identity*** and ***Get_Status*** on SOP'. When the SOP'' Controller Present bit is set in the Active Cable VDO, they shall respond ***Get_Status*** on SOP'' as well.

6.2.3.2 Cable Status

The *USB PD* ***Get_Status*** Command is used to discover the current state of the active cable. Cable status shall be reported on SOP' and shall also be reported on SOP" when the SOP'' Controller Presence bit is set in the Active Cable VDO.

6.2.4 Active Cable Behaviors in Response to Power Delivery Events

Each cable plug of the short active cable shall be capable of communicating on SOP' and SOP" if reported in the Discover_Identity Command.

6.2.4.1 Data Role Swap

Active cables are transparent to the *USB PD* Data Role swap.

6.2.4.2 Power Role Swap

Active cables shall maintain *USB 3.2* signaling during a *USB PD* Power Role swap. The source of VCONN is not affected by a Power Role Swap.

6.2.4.3 VCONN Swap

Active cables shall maintain *USB 3.2* signaling during a *USB PD* VCONN swap. During a VCONN Swap, the original VCONN Source continues to supply VCONN for some time after the new VCONN Source begins to supply VCONN. This ensures that VCONN is never dropped.

6.2.4.4 Fast Role Swap

Active cables will drop *USB 3.2* signaling as a side-effect of a Fast Role Swap if VCONN is not maintained during the Fast Role Swap.

6.2.5 Active Cable Power Requirements

6.2.5.1 VBUS Requirements

Active cables shall meet the limits of the IR Drop on VBUS and ground defined in Section 4.4.1.

Active cables shall provide VBUS and support at least 3 A and optionally 5 A current.

6.2.5.2 VCONN Requirements

Active Cables shall:

- Meet the VCONN sink requirement defined in Table 4-6, Table 6.3.x.x.x (U-Requirements) and Table 6.3.x.x.x (CLx)
- Connect VCONN as shown in Figures xxx in Section 6.3.2

Active cables shall meet the VCONN requirements specified in Section 4.9.

6.3 Optical Isolated Active Cable

6.3.1 Overview[LE4]

Optically Isolated Active Cables (OIACs) key features are that they support longer lengths up to 50 meters and provide electrical isolation between the two ends of the cable.

This specification defines support for the following OIACs:

- USB3.2 Gen2
- USB4 Gen3 (USB3.2 Gen2, USB4 Gen2, TBT3, and USB4 Gen3)
- USB4 Gen4 (USB3.2 Gen2, USB4 Gen2, TBT3, USB4 Gen3, USB4 Gen4)

They are targeted for Industrial, Machine Vision, Remote Sensor, Pro Video, and Medical applications.

Since no power runs through an OIAC, Vconn must be provided from both ends and USB-PD is required to correctly setup DFP-UFP link. Therefore an OIAC can only be used to connect a Source DRD to a Source DRD or a Source DRD to a DFP, and at least one of the Sourcing DRDs must start out as a Sourcing DFP and ACCEPT a DR_Swap request to a UFP. *USB PD* Revision 3 must be supported on both port partners for an OIAC to function. These requirements are detailed in section 6.2.4.1

OIACs have additional limitations on the systems as a whole, even when a viable High Speed link has been established, including but not limited to some power saving modes, and features that require Alt-Modes or USB2.0, which are not supported by the OIAC. Additional system limitations are defined in section 6.3.3.4

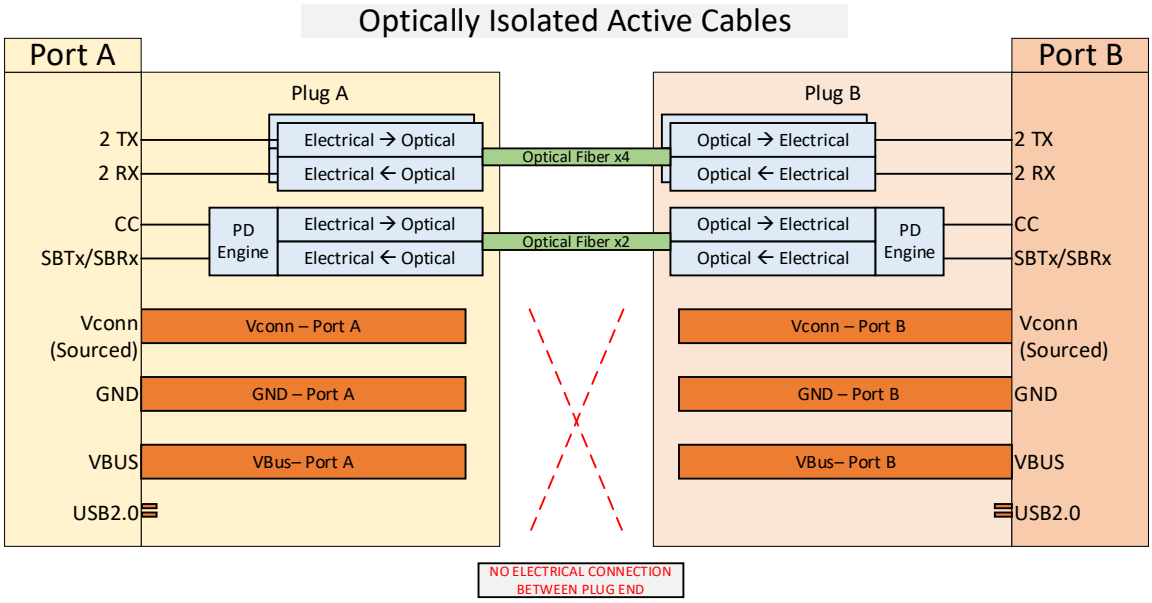
If a connection to a *USB 2.0* Device is required at the end of an OIAC, an adapter with a *USB 3.2* to *USB 2.0* transaction translator and VBUS/VCONN Source may be connected at the Device side of the cable to convert the *USB 3.2* signals to *USB 2.0* and provide power to the *USB 2.0* Device and the OIAC.

OIACs may optionally support other Alternate Modes. If an OIAC supports Alternate Modes that require the use of SBUs, the SBUs shall be optically isolated.

6.3.2 OIAC Block Diagrams

OIACs can be implemented in different ways: this document will only describe one possible implementation for the USB3.2 and the corresponding USB4 version. Other implementations can be used, as long as the all the electrical plug specification and characteristics are the same.

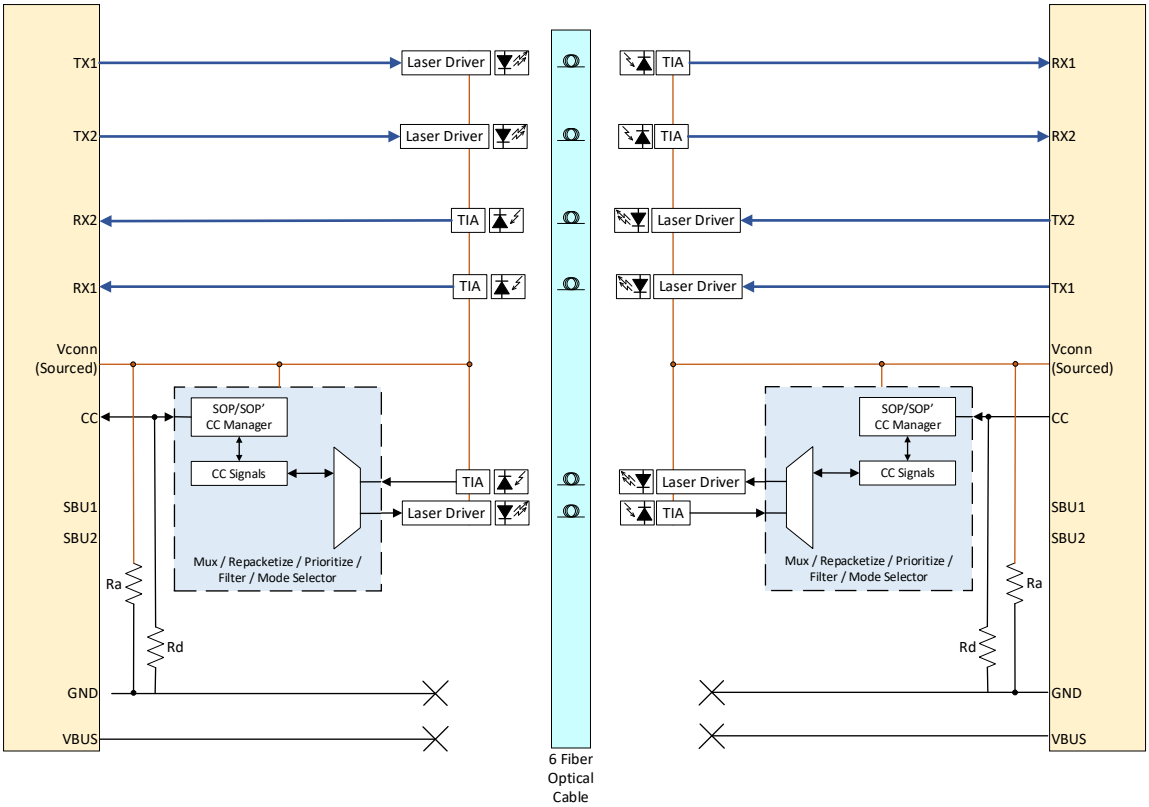
6.3.2.1 Simplified Optically Isolated Active Cable (OIAC) Block Diagram



6.3.2.2 Example - Detailed OIAC Block Diagram - USB3.2 Gen 2

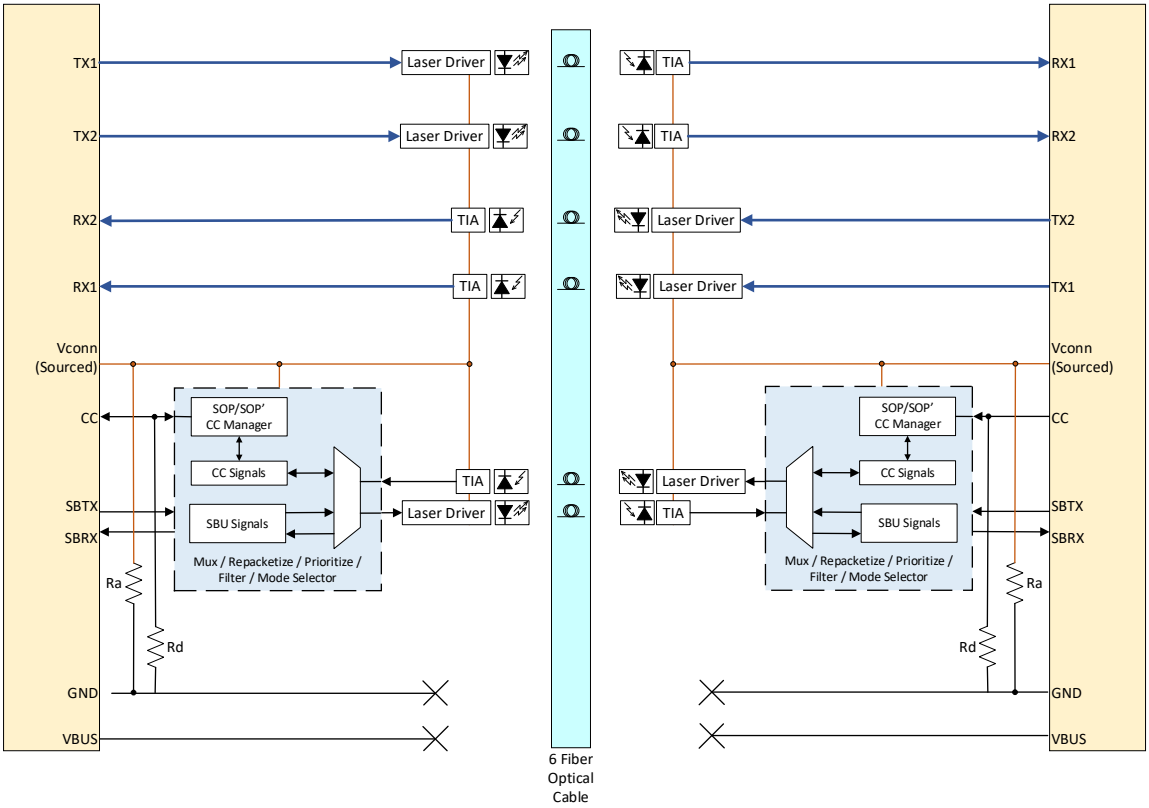
Example of an OIAC implementation.

SBU lines are unused unless directed to enter an Alt-Mode.



6.3.2.3 Example - Detailed OIAC Block Diagram - USB4 Gen3/4 Block Diagram

Example of an OIAC implementation.



6.3.3 Limitations and Requirements

6.3.3.1 Limitations of Optical Isolated Active Cable vs. Active Cable

The Optically Isolated Active Cable (OIAC) ***shall*** not have any electrical wires running between the two plug ends. There are NO electrical wires for VBUS, VCONN, GND, SBx, or USB2.0.

VBUS, VCONN, and GND are completely isolated on each end of the cable, which means that the host/device must be both self-powered and supply Vconn to the OIAC.

The following features are optional:

- DP-Alt Mode
- USB2.0
- USB-PD Unchunked Messages
- Asymmetric Mode (3x1) in USB4v2 (Section6.x.x.)

Cable Vconn CLd/U3 Power Requirement

The OIAC does not reduce the power requirement on Vconn during the CLd/U3 power state. The power consumption for Vconn power @ CL3/U3 <= power at CL0/U0. Additional details are in Section 6.3.7.4.3 and Section 6.3.7.7

The above limitations of the OIAC force additional requirements on the Host / Device connected to the OIAC, including be not limited to both Vconn and USB-PD being required on each end of the cable. Additional requirements for the Host and Device and listed in the section 6.3.3.2 and section 6.3.3.3

6.3.3.2 Host Requirements

All USB certified hosts should meet all the requirements to support an OIAC.

However, the minimum requirements are listed here:

1) Source VCONN
2) Support USB-PD
3) Initialize as a Sourcing DFP
4) Dual Role Data (*)

(*) Conditional Requirement:

In the scenario where the Host and OIAC is connected to Dual Role Data (DRD) Host/Device, at least one of the two (the Host on the near end or Host/Device on the far end) must be able to accept a DR_Swap when requested. If both ends "Reject" (or continuously respond with "Wait") then the DFP-UFP link can not be created and a USB link will not be established.

6.3.3.3 Device Requirements

There are more device requirements to use an OIAC and a standard USB device. This is because the OIAC does not have a VBUS wire connecting the DFP and the UFP.

The device will need the meet all the following requirements:

1) Source VCONN
2) Support USB-PD
3) Initialize as a Sourcing DFP
4) Dual Role Data (*)

(*) Conditional Requirement:

In the scenario where the Device and OIAC is connected to Dual Role Data (DRD) Host/Device, at least one of the two (the Device on the near end or Host/Device on the far end) must be able to accept a DR_Swap when requested. If both ends "Reject" (or continuously respond with "Wait") then the DFP-UFP link can not be created and a USB link will not be established.

Note: It is expected that the Device is a DRD Device that is able to support a DR_Swap request to a UFP.

6.3.3.4 Additional limitations with using an OIAC with a downstream device (Dock/Hub/Devices)

Assuming a USB4 (or USB3) link is established using an OIAC, some features that are normally available with a Full Featured Copper Cable, may not be fully supported in the link including the following:

Downstream USB2.0 ports

Downstream USB2.0 ports may not work on the Dock/Hub/Device. This is device dependent, as the device could and most likely will connected directly to the upsteam USB2.0 link.

Downstream USB2.0 ports maybe not work properly.

Downstream Alt-Modes ports

Some devices may assume that all Alt-Modes are supported by the cable. However, the ONLY required supported Alt-Mode for the OIAC is Thunderbolt3. All other Alt-Mode (ie. DP) are only supported, if the OIAC specifically specifies that that mode is supported.

Downstream Alt-Mode (ie. DP or HDMI) ports may not work.

6.3.3.5 Typical Link Examples [LE5]

6.3.3.5.1 NonDRD Host to DRD Device

6.3.3.5.2 DRD Host to DRD Device

6.3.3.5.3 Non-Typical Host to Host Link Examples

6.3.3.5.4 NonDRD Host to DRD Host

6.3.3.5.5 NonDRD Host to NonDRD Host

6.3.3.5.6 DRD Host to DRD Host

6.3.4 OIAC Cable Power Requirements

6.3.4.1 VBUS Requirements

There are NO VBUS wires across the OIACs.

6.3.4.2 VCONN Requirements

There is no VCONN wire between the two ends of the OIAC, therefore, it is possible for the each OIAC plug to consume the entire 1.5W allocated to VCONN from each port. However, the ***OIAC MUST meet all thermal and mechanical requirements*** of the USB Type-C Active Cable.

OIAC Cables shall:

- Meet the VCONN sink requirement defined in Table 4-6, Table 6-20 and Table 6-30.
- Connect VCONN as shown in Figures 6.x.x. in section 6.3.2

Active cables shall meet the VCONN requirements specified in Section 4.9.

6.3.4.3 OIAC Power Contract

The OIAC does NOT have VBUS going through the cable, however each OIAC cable plug will have a power contract with their respective ports. This is required for any USB-PD communication, which is needed for the OIAC to properly initialize.

The recommended power contract response for the OIAC is detailed in Section 6.3.x.x. (OIAC's specific response to Source_Capabilities).

6.3.5 Optical Isolated Active Cable USB PD Requirements

OIACs shall support *USB PD* Revision 3, Version 1.5 or later[LE6]. OIACs shall support *USB PD* Structured VDMs.

6.3.5.1 SOP' and SOP" Requirements

OIAC shall respond to ***Discover_Identity*** and ***Get_Status*** on SOP'.

SOP'' Controller is not required in the OIAC, however, a ***Get_Status*** on SOP' will respond with Thermal Shutdown and temperature information of the worse case of BOTH cable ends. The OIAC will need to internally communicate thermal information between the plug ends and provide that information on the SOP' response.

OIACs will always have SOP' are the near end and SOP" is the far end with respect to each port.

6.3.5.2 USB4v2 Asymmetric Mode Support

The OIAC may optionally support USB4v2 asymmetric mode. This support shall be reported in the Active Cable VDO2 (bit x).

6.3.5.3 USB-PD Message Handling

Table 6-x OIAC PD Message Handling

Received Message	Local OIAC Plug Response (sink)
Resets	
Cable Reset	Specified in Section 6.3.5.2.1
Hard Reset	Specified in Section 6.3.5.2.1
Soft Reset	Specified in Section 6.3.5.2.1
Data Reset	Specified in Section 6.3.5.2.1
Locally Handled Messages	
Get_Sink_Capabilities	Specified in Section 6.3.5.2.2.1.1

Source_Capabilites	Specified in Section 6.3.5.2.2.1.2
PR_Swap	Reject (Section 6.3.5.2.2.1)
FR_Swap	Reject (Section 6.3.5.2.2.1)
Vconn_Swap	Reject (Section 6.3.5.2.2.1)
Get_Source_Capabilities	Not Supported (Section 6.3.5.2.2.2)
Get_Source_Capabilites_Extended	Not Supported (Section 6.3.5.2.2.2)
EPR_Get_Source_Capabilities	Not Supported (Section 6.3.5.2.2.2)
EPR_Get_Sink_Capabilites	Not Supported (Section 6.3.5.2.2.2)
BIST	Specified in Section 6.3.5.2.2.4.1
GoodCRC	Specified in Section 6.3.5.2.2.4.2
PS_RDY	Specified in Section 6.3.5.2.2.4.2
GotoMin	Ignore (Section 6.3.5.2.2.4.3)
Conditionally Handled Messages	
Accept	Specified in Section 6.4.3.1
Reject	Specified in Section 6.4.3.2
Wait	Specified in Section 6.4.3.3
All other USB-PD Messages shall be allowed to traverse the OIAC	

6.3.5.3.1 USB-PD Reset (Hard, Cable, Soft, Data)

All Resets (Cable, Hard, Data, Soft) will be handled the same by the OIAC. They will be all be treated as Hard Reset, which resets VCONN.

For Hard (or Cable) Reset, an OIAC plug shall:

1. Detect the Hard (or Cable) Reset ordered set
2. Forward "disconnect event" to the remote plug
3. Remove Rd

For Data (or Soft) Reset, an OIAC plug shall:

1. Detect the Data (or Soft) Reset Message
2. Forward "disconnect event" to the remote plug
3. Remove Rd

(Far End Plug)

1) Receive "disconnect event"
2) Remove Rd

(Forwarding a "disconnect event," can be accomplished with a simple internal message or any other means the implemented decides.)

A Hard Reset signal can occur at any time during normal operation of the cable and also during the cable initialization. This signal will take precedent over the initialization state machine and immediately forward the Hard Reset Message to the remote plug, using an internal cable message.

6.3.5.3.2 Locally handled SOP USB-PD messages received by the OIAC Plug

6.3.5.3.2.1 Specific Responses from the local OIAC plug

6.3.5.3.2.1.1 Get_Sink_Capabilites

The OIAC plug ***shall*** respond to this message directly and the suggested response is defined in Table x.x and Table x.x. depending on which phase of the link bring up the OIAC is currently in.

Table 6-x Recommended OIAC Sink_Capabilities PDO (SOP) on Initial Connection

Bit(s)	Value	Parameter
B31..30	00b	Fixed Supply
B29	0b	Not Dual-Role Power
B28	0b	Not higher capability
B27	0b	Not unconstrained power
B26	1b	USB Communications Capable
B25	0b	Dual-Role Data
B24..23	00b	Fast Role Swap not supported
B22..20	000b	Reserved
B19..10	00 0110 0100b	5V in 50mV units
B9..0	00 0000 0000b	Operational current in 10mA units

Table 6-x Recommended OIAC Sink_Capabilities PDO (SOP) in Active Connection

Bit(s)	Value	Parameter
B31..30	00b	Fixed Supply
B29	0b	Not Dual-Role Power
B28	0b	Not higher capability
B27	0b	Not unconstrained power
B26	1b	USB Communications Capable
B25	As reported from Remote End	Dual-Role Data[1]
B24..23	00b	Fast Role Swap not supported
B22..20	000b	Reserved
B19..10	00 0110 0100b	5 V in 50 mV units
B9..0	00 0000 0000b	Operational current in 10 mA units

Notes: 1. Reflection of far side connection

6.3.5.3.2.1.2 Source_Capabilites

The OIAC plug ***shall*** respond to this message directly and the recommended responses are defined in Table x.x and Table x.x. depending on which phase of the link bring up the OIAC is currently in.

A recommended Sink RDO is provided as an example in Table 6-14 is the same for both the initial connection and when the OIAC is in normal active mode. The OIAC shall function when receiving the minimum Source PDO. The

The OIAC plug will request 5v 0mA

OIAC shall NOT support Unchuck Messages

Table 6-14 Recommended OIAC Active Sink RDO (SOP)

Bit(s)	Value	Parameter
B31	0b	Reserved
B20..28	0 0000 0001b	Object Position
B27	0b	No GiveBack flag
B26	0b	No Capabilities Mismatch
B25	1b	USB Communication Capable
B24	1b	USB Suspend
B23	0b	Unchunked Extended Messages
B22..20	000b	Reserved
B19..10	0b	Operating Current in 10 mA units[1]
B9..0	0b	Maximum current in 10 mA units[1]

Note 1: Thermal design must be considered.

6.3.5.3.2.2 "Rejected" Response from the local OIAC plug

The OIAC by definition does not have any copper wires, therefore must supply power from each end independently, which makes any type of power swapping not possible. The following messages shall be intercepted by the OIAC and responded with a "Reject."

PR_Swap

FR_Swap

Vconn_Swap

6.3.5.3.2.3 "Not Supported" Response from the local OIAC plug

Since the OIAC acting as sink (that must be powered by the local port) on both ends of the cable the following messages are not applicable. The OIAC shall respond with a "Not Supported."

Get_Source_Cap

Get Source_Cap Extended

EPR_Get_Source_Cap

EPR_Get_Sink_Cap

6.3.5.3.2.4 Handled/Ignored by the local OIAC plug

6.3.5.3.2.4.1 BIST

BIST is a function that needs to be supported by the OIAC plug. The BIST message from the port should intercepted and completely handled by the OIAC plug.

6.3.5.3.2.4.2 GoodCRC, PS_RDY

Both of these messages, GoodCRC and PS_RDY are confirmation messages that he previous message was successful. They just need to terminate in the OIAC plug.

6.3.5.3.2.4.3 GotoMin

GotoMin is a message that will just be completely IGNORED by the OIAC. As this should have no effect but is required to be terminated in the plug.

6.3.5.3.2.4.4 Soft Reset, Data Reset

See Section 6.3.5.2.1

6.3.5.3.2.5 Conditional Response Messages

6.3.5.3.2.5.1 Accept

The Accept Message is a ***Valid*** response to ONLY the following messages: Request, EPR_Request, PR_Swap, DR_Swap, Vconn_Swap, FR_Swap, Soft_Reset, and Enter_USB.

The OIAC, as the sink, will NEVER initiate any type of Power Swap or EPR request, therefore, an Accept response from the source for those messages (EPR_Request, PR_Swap, Vconn_Swap, FR_Swap) will NEVER occur.

Soft_Reset will be handled as a reset case and is defined in Section 6.x.x.x. There will never be an Accept message following a Soft_Reset.

A Request Message can and will initiate from the OIAC, so an Accept following that Request message will need to be processed within the OIAC plug and will NOT need to traverse the OIAC.

Both a DR_Swap and Enter_USB message can initiate from either end of the OIAC, and therefore may require an Accept message to traverse the OIAC.

6.3.5.3.2.5.2 Reject

The Reject Message is a ***Valid*** response to ONLY the following messages: Request, EPR_Request, PR_Swap, DR_Swap, Vconn_Swap, and Enter_USB.

The OIAC, as the sink, will NEVER initiate any type of Power Swap or EPR request, therefore, a Wait response from the source for those messages (EPR_Request, PR_Swap, Vconn_Swap) will NEVER occur.

A Request Message can and will initiate from the OIAC, so a Reject following that Request message will need to be processed within the OIAC plug and will NOT need to traverse the OIAC.

Both a DR_Swap and Enter_USB message can initiate from either end of the OIAC, and therefore may require a Reject message to traverse the OIAC.

6.3.5.3.2.5.3 Wait

The Wait Message is a ***Valid*** response to ONLY the following messages: Request, EPR_Request, PR_Swap, DR_Swap, Vconn_Swap, and Enter_USB.

The OIAC, as the sink, will NEVER initiate any type of Power Swap or EPR request, therefore, a Wait response from the source for those messages (EPR_Request, PR_Swap, Vconn_Swap) will NEVER occur.

A Request Message can and will initiate from the OIAC, so a Wait following that Request message will need to be processed within the OIAC plug and will NOT need to traverse the OIAC.

Both a DR_Swap and Enter_USB message can initiate from either end of the OIAC, and therefore may require a Wait message to traverse the OIAC.

6.3.5.3.2.6 Other PD Messages

6.3.5.3.2.6.1 Get Status SOP'

OIACs are not required to support SOP", however, when reporting to a Get_Status message, the OIAC must provide accurate temperature information on the worst case of either cable plug, the higher temperature reading. And it must provide thermal shutdown information of either cable plug.

6.3.5.3.3 Messages that Traverse the OIAC

All other USB-PD messages that are not listed in above section are considered "Generic" and will allowed to traverse the OIAC.

6.3.5.3.4 OIAC Cable Status

The *USB PD* ***Get_Status*** Command is used to discover the current state of the active cable. Cable status shall be reported on SOP'.

6.3.5.3.5 OIAC USB PD Message Forwarding Timing

Figure 6-4 OIAC USB PD Message Forwarding

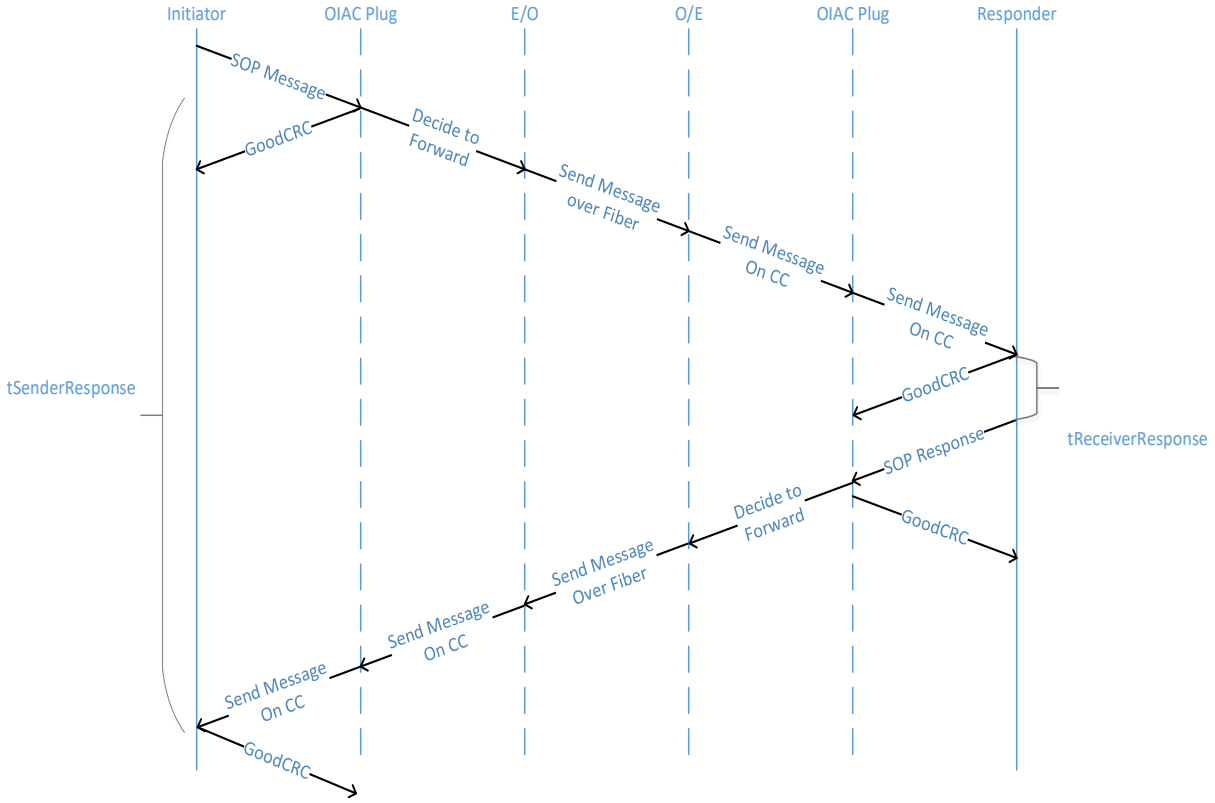


Table 6-7 OIAC USB PD Message Timing

Timer	Value (Min)	Value (Max)	Units	Reference
tDRSwapWait	100		ms	Time to wait if WAIT received before sending another DR_Swap. Defined in the *USB PD* Specification.
tForward		4	ms	Time to forward SOP Message one direction in OIAC.
tTransmit		195	µs	Time to send the GoodCRC. Defined in the *USB PD* Specification.
tInterFrameGap	25		µs	Time from the end of last bit of a Frame until the start of the first bit of the next Preamble. Defined in the *USB PD* Specification.
tReceiverResponse		15	ms	Time for SOP Receiver to respond. Defined in the *USB PD* Specification.
tSenderResponse	26	32	ms	Time for SOP Initiator to receive response. Defined in the *USB PD* Specification.
tBootupCRCHoldoff		50	ms	Hold off on GoodCRC until ready to respond with Operational RDO in Phase 3.

Note: The *USB PD* specification revision shall take precedence over this table if any discrepancies exist.

6.3.5.3.6 Example - Internal Cable Messages

All SOP messages shall be forwarded or terminated as defined in Section 6.2.2 and will not be further described in this section.

The messages defined in this section provide informative guidance on internal messages for OIACs. The actual definition and implementation of each message is left to the implementer.

In this section and Section 6.3, there is a defined Plug-A and Plug-B to support *USB PD* communication through the OIAC cable. These designations are established at the time of manufacture and are completely internal to the cable. They are used to simplify the cable initialization and internal messaging.

6.3.5.3.6.1 MSG_Keep_Alive

A low duty cycle message that is meant to inform the remote cable plug that the local cable plug is still operational.

A simple example is that only Plug-A will send MSG_Keep_Alive and Plug-B must respond with MSG_Keep_Alive_ACK. Each end will have its own timeout for MSG_Keep_Alive and MSG_Keep_Alive_ACK.

6.3.5.3.6.2 MSG_Keep_Alive_ACK

Acknowledgement message to the MSG_Keep_Alive.

A simple example is that only Plug-A will send MSG_Keep_Alive and Plug-B must respond with MSG_Keep_Alive_ACK. Each end will have its own timeout for MSG_Keep_Alive and MSG_Keep_Alive_ACK.

6.3.5.3.6.3 MSG_Port_Capabilities

This message contains all relevant local port capabilities including but not limited to:

- Chunked/Unchunked capability
- DRD/DFP/UFP capabilities

6.3.5.3.6.4 MSG_Cable_Config

This message contains the final cable configuration based on known system capabilities.

It will contain both relevant ports' capabilities and the final DFP/UFP roles for the system.

This message will also serve as the signal in Phase 2 for the cable plug to start the reboot process.

6.3.5.3.6.5 MSG_Release_Remote_SourceCap_GoodCRC

This is a synchronization message to attempt to bring up both ports at the same time.

It is used in Phase 3 and is the signal to release the GoodCRC message to the Source Capabilities message from the attached port. At the beginning of Phase 3, after each plug has been rebooted, and depending on the final DFP/UFP role, each plug should wait for MSG_Release_Remote_SourceCap_GoodCRC before it is allowed to release a GoodCRC in response to a Source_Capabilities message from the port.

6.3.5.3.6.6 MSG_DR_Swap_Init

Initial DR_Swap sent by Plug-A to Plug-B to perform a DR_Swap.

6.3.5.3.6.7 MSG_DR_Swap_Reject

Plug-B sends this message to report that the initial DR_Swap was rejected by its attached port.

This is needed by Plug-A to attempt to re-configure the cable such that the port associated to Plug-B can remain a DFP. This is part of the DR_Swap test in Phase 1, shown in the state diagram transition from M3 to M4 (or M3 to M5). It is also possible that this may be needed in Phase 3, if the port associated with Plug-B rejects the DR_Swap.

6.3.5.3.6.8 MSG_DR_Swap_Accept

Plug-B sends this message to report that the initial DR_Swap was accepted by its attached port.

This is needed by Plug-A to continue (M3 → M6 transition) in Phase 1 in the cable initialization.

6.3.5.3.6.9 MSG_Force_Detach

This message is to request the remote plug to disconnect from its attached port. The disconnect method can be done by raising the voltage on the CC line to above vRd-Connect or removing Rd.

This will cause the remote port to remove VCONN from the remote plug all the circuitry should be powered down, therefore resetting any action taken by the plug on the CC line to cause the disconnect.

6.3.5.3.6.10 MSG__Reset

This message is to forward any Reset (Hard, Cable, Data, Soft) signal to the remote plug and port.

An internal Reset message should be responded to with an Acknowledgement, but may not be necessary depending on implementation.

6.3.5.3.6.11 MSG_Acknowledgement

This message is to acknowledge that a message was received.

This message has been explicitly defined in a few specific cases but can be used more broadly.

6.3.5.3.7 Example - Data Role Swap in Active State

OIACs shall support Data Role Swaps on SOP. Each OIAC plug discovers its plug port partner and determines if it is capable of a Data Role Swap during the initialization process described in Section 6.3. OIAC cable plugs generate internal messages to communicate the DR_Swap, Accept, Reject, and Wait to the far side of the cable.

- The flow of a successful DR_Swap is shown in Figure 6-5.
- The flow of a Responder rejecting a DR_Swap is shown in Figure 6-6.
- The flow of a Responder issuing a Wait to a DR_Swap is shown in Figure 6-7. Note: The *USB PD* Wait and Retry timers shall follow all timing requirements in *USB PD*.
- The flow of an Initiator rejecting a cable plug DR_Swap due to an Accept from the Responder is shown in Figure 6-8.
- The flow of an Initiator issuing a Wait to a cable plug DR_Swap due to an Accept from the Responder is shown in Figure 6-9. Note: This does not follow the *USB PD* Wait timing, because a Hard Reset is initiated

Figure 6-5 OIAC Successful Data Role Swap

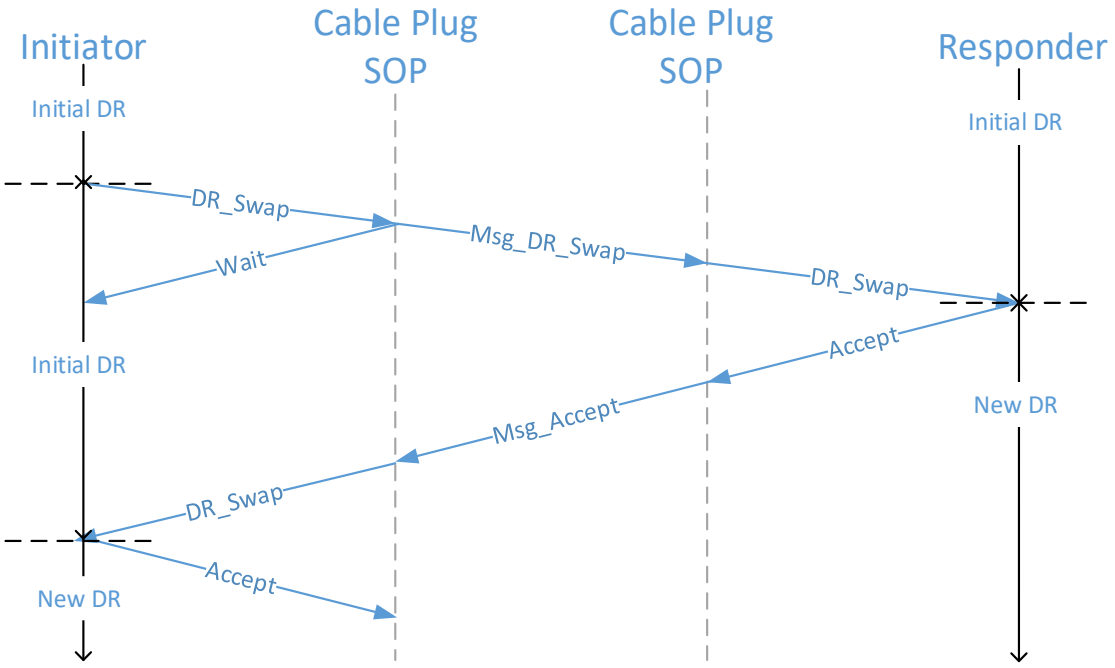


Figure 6-6 OIAC Rejected Data Role Swap

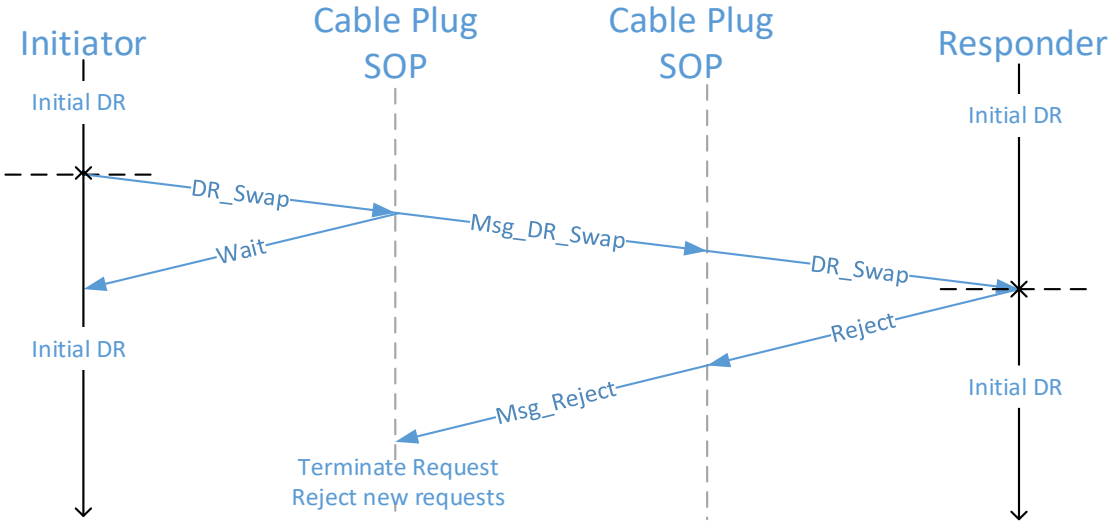


Figure 6-7 OIAC Wait Data Role Swap

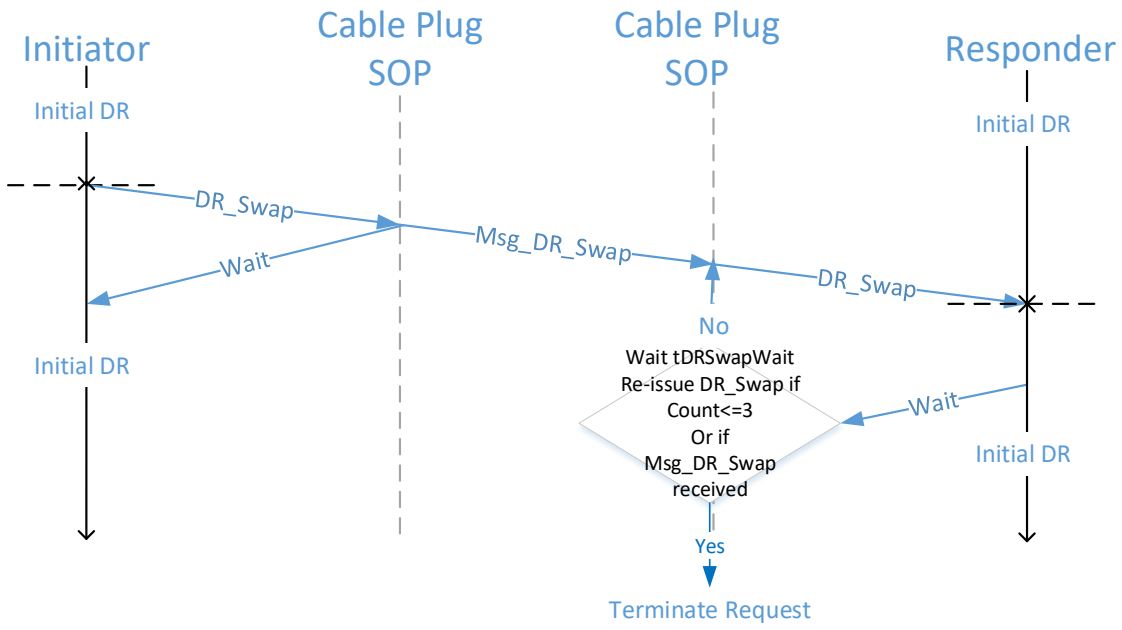


Figure 6-8 OIAC Initiator Reject Data Role Swap

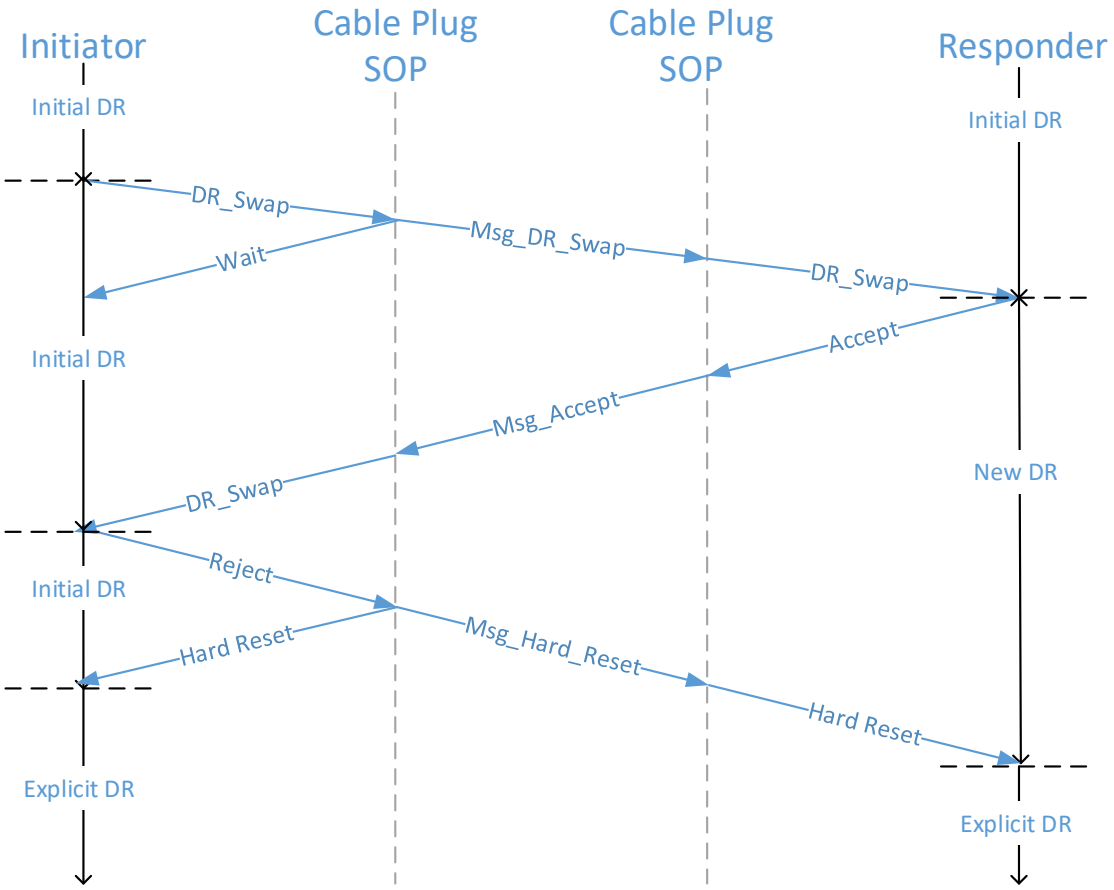
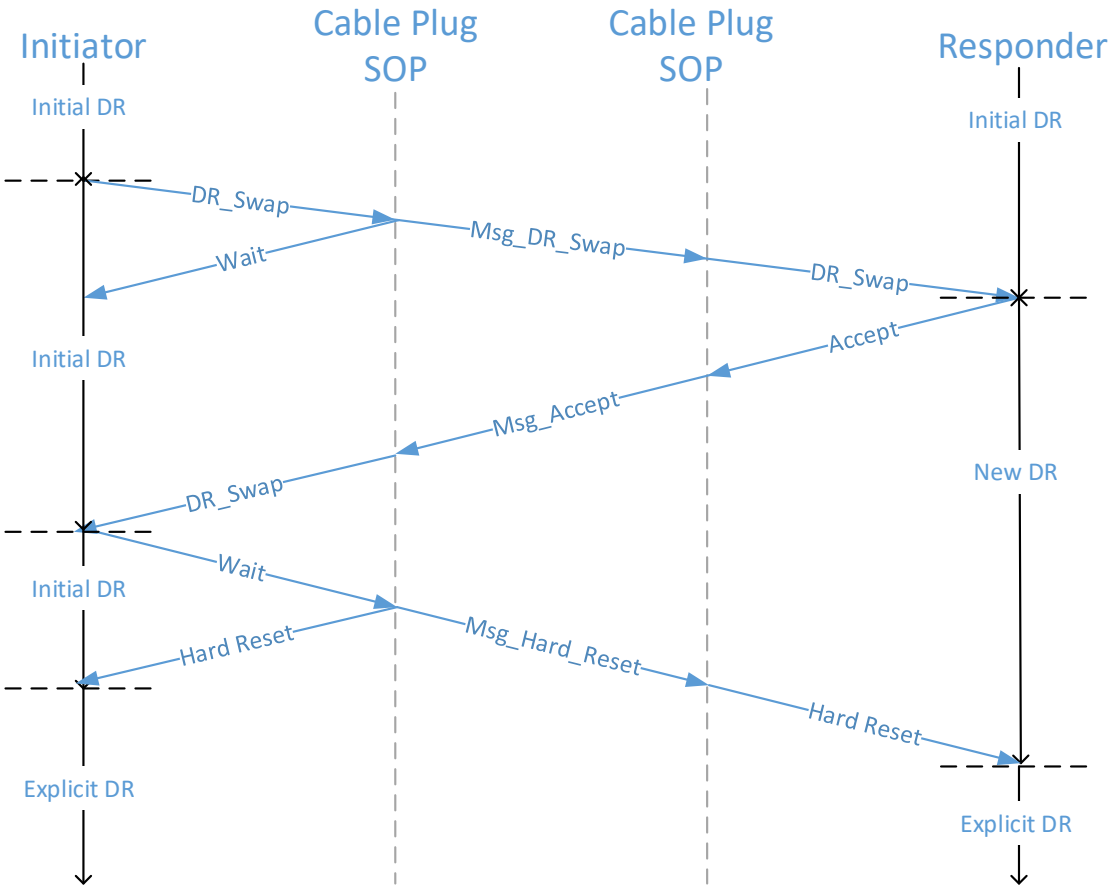


Figure 6-9 OIAC Initiator Wait Data Role Swap



6.3.6 OIAC Connection Flow and State Diagrams for USB3.x

This section defines the connection state diagrams for the OIAC.

OIAC plug defined at time of manufacture as either Plug-A or Plug-B for *USB PD* communication. This in no way indicates the plug has more or less capability, rather it allows for a consistent behavior when making the initial end to end connection.

The OIAC communicates using *USB PD* with its plug partners to determine the partner capabilities. The OIAC performs a series of connect/disconnects to establish the correct UFP/DFP data role for the cable plug. The possible combinations for ports and cable plugs is defined in Table 6-9.

The connection and establishment of data roles is performed in three phases.

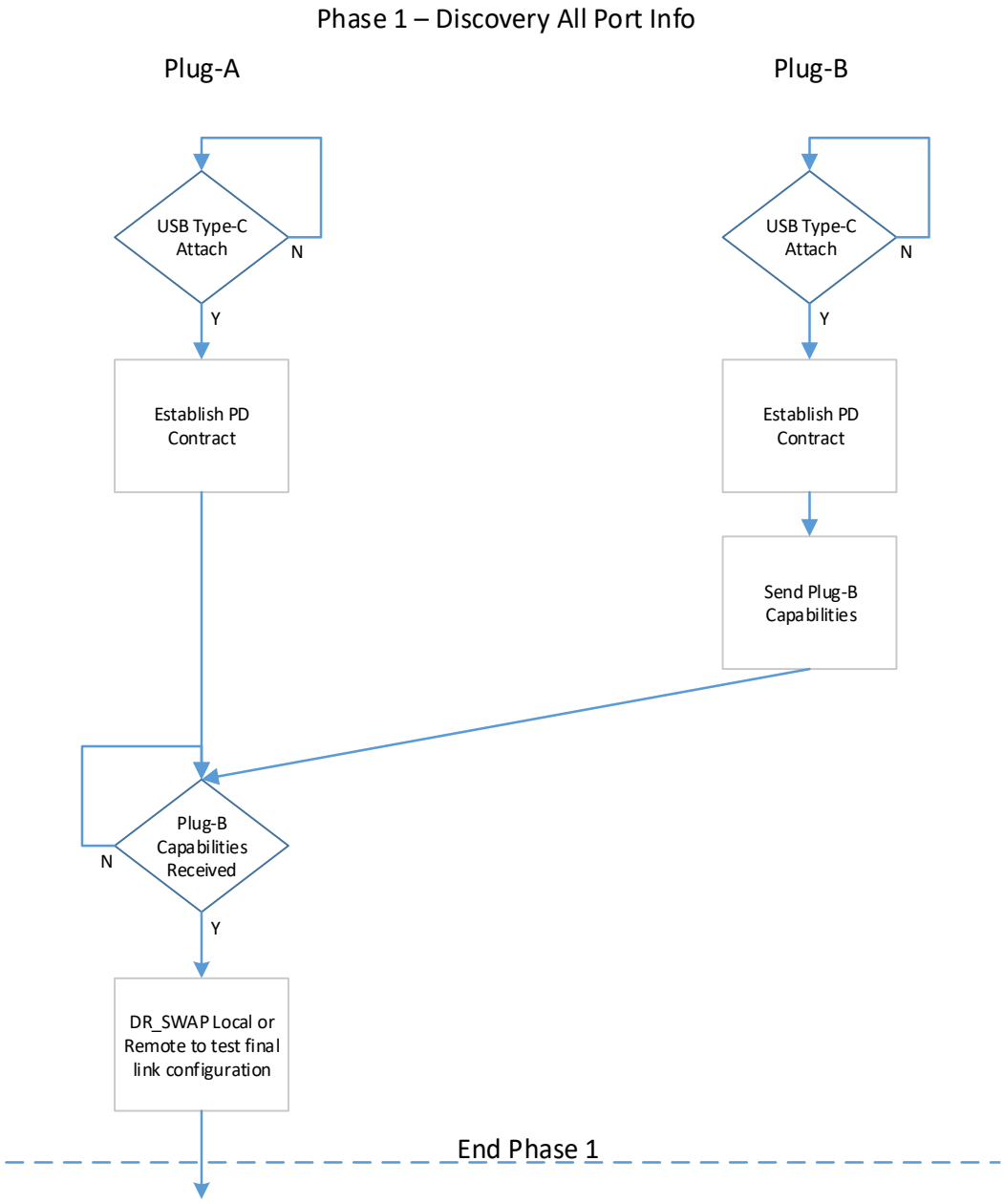
Table 6-9 Port and Plug Capabilities

Host/Device Port Capabilities	Cable Configuration		Host/Device Port Capabilities
	Plug-A Role	Plug-B Role	
DRD	DFP	UFP	DRD
DFP	UFP	DFP	DRD
DRD	DFP	UFP	DFP
DFP	Billboard		DFP
Any	Billboard if possible		UFP
UFP	Billboard if possible		Any

6.3.6.1 OIAC Connection Flow – Discovery – Phase 1

The OIAC cable plugs discover the capabilities of their port partners in the Discovery Phase.

Figure 6-10 OIAC Discovery – Phase 1



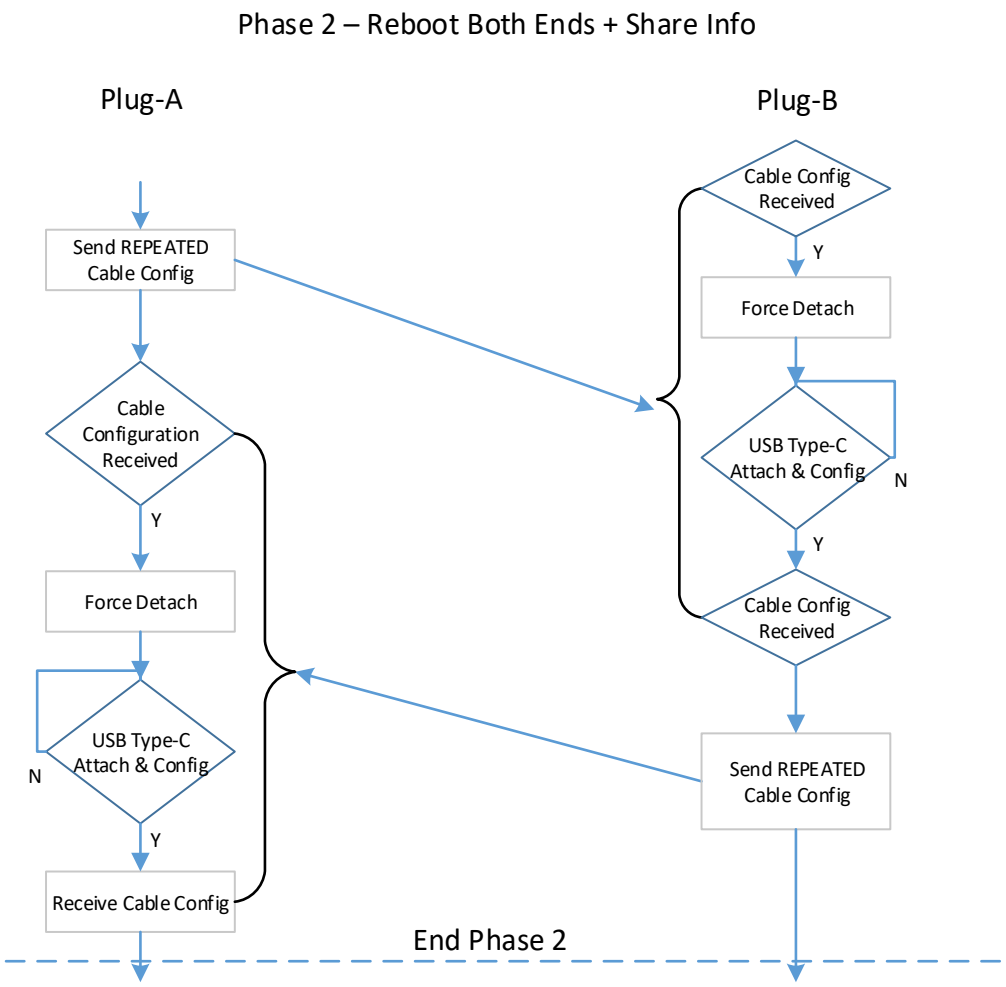
6.3.6.2 OIAC Connection Flow – Reboot – Phase 2

The OIAC cable plugs forward the capabilities of their plug partners and perform disconnect/reconnect.

- Plug-A will always start with repeatedly sending "MSG_Cable_Config" to Plug-B to start reboot.
- Plug-B Reboots.

- Plug-B sees "MSG_Cable_Config" and holds off on SourceCap GoodCRC until it is allowed to release it.
- Plug-B sends "MSG_Cable_Config" to the Plug-A.
- Plug-A Reboots.
- Plug-A sees "MSG_Cable_Config" and holds off on SourceCap GoodCRC until it is allowed to release it.

Figure 6-11 OIAC Reboot – Phase 2



6.3.6.3 OIAC Connection Flow – Configuration – Phase 3

The OIAC Plug-A determines DFP/UFP roles for Plug-A and Plug-B. Plug-A releases the PLUG to be configured as the DFP and initiates a DR_Swap. The side that issues the DR_Swap send a DR_Swap and releases the other side SourceCap GoodCRC.

Figure 6-12 OIAC Plug-A Configured as DFP – Phase 3

Host/Device Port		Cable			Host/Device Port
		Plug-A	Plug-B		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any

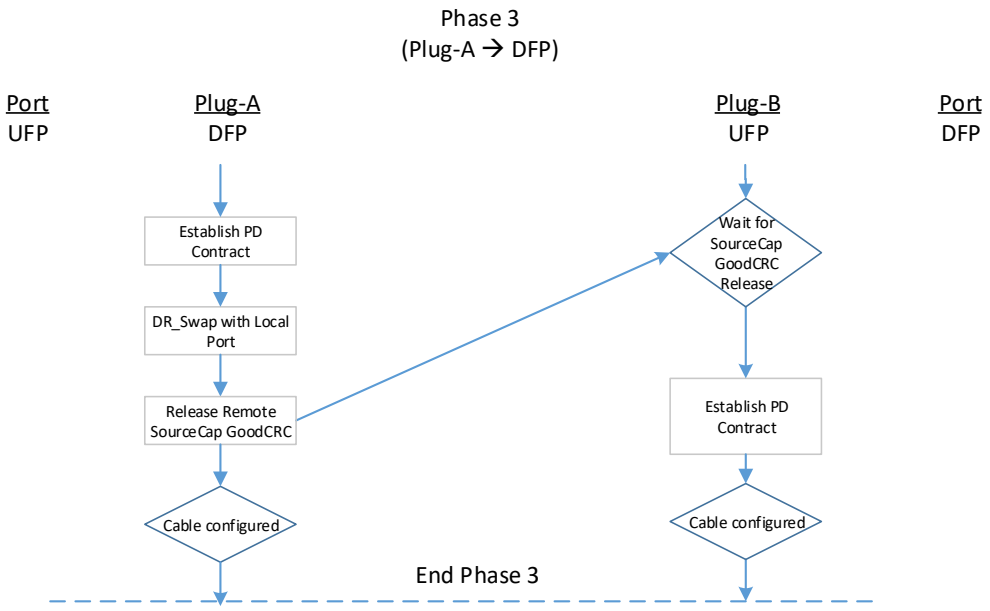


Figure 6-13 OIAC Plug-A Configured as UFP – Phase 3

Host/Device Port		Cable			Host/Device Port
		Plug-A	Plug-B		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any

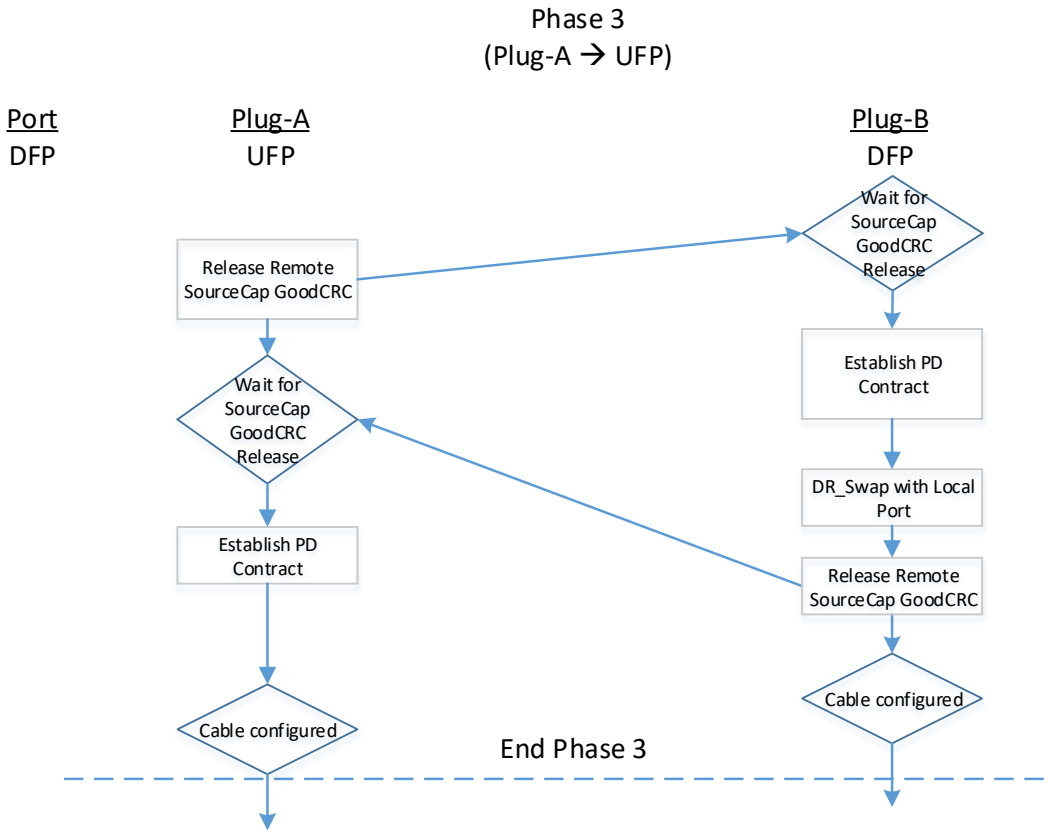
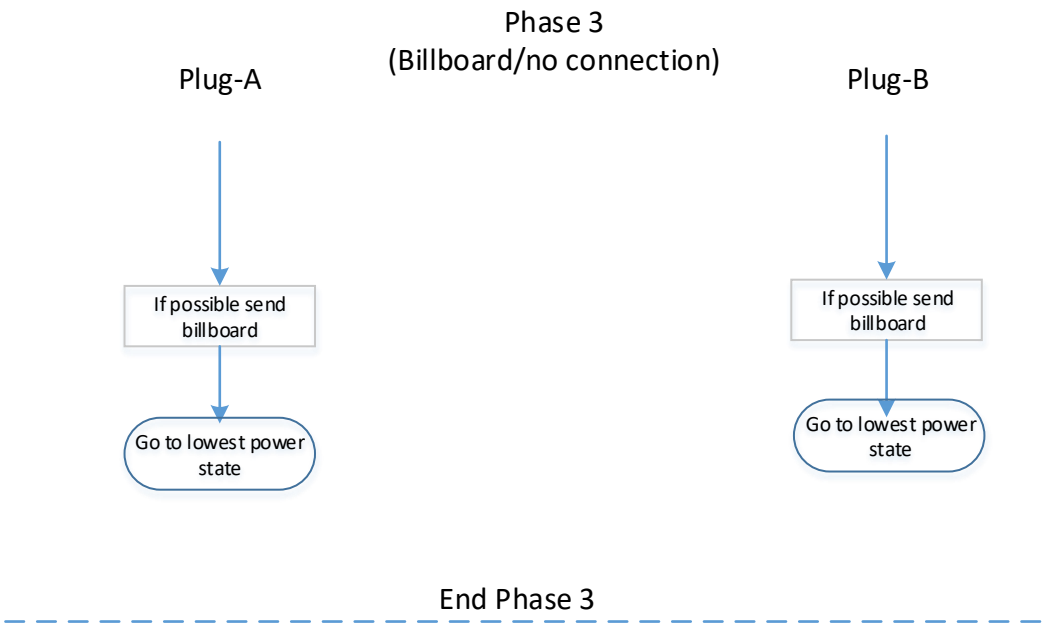


Figure 6-14 OIAC Plug-A No Connection Possible Billboard – Phase 3

Host/Device Port		Cable			Host/Device Port
		Plug-A	Plug-B		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any



6.3.6.4 OIAC Connection State Diagram Plug-A

The following sections details a possible OIAC state diagram for Plug-A.

Figure 6-15 OIAC Plug-A State Diagram Part 1 (Phase 1 and 2)

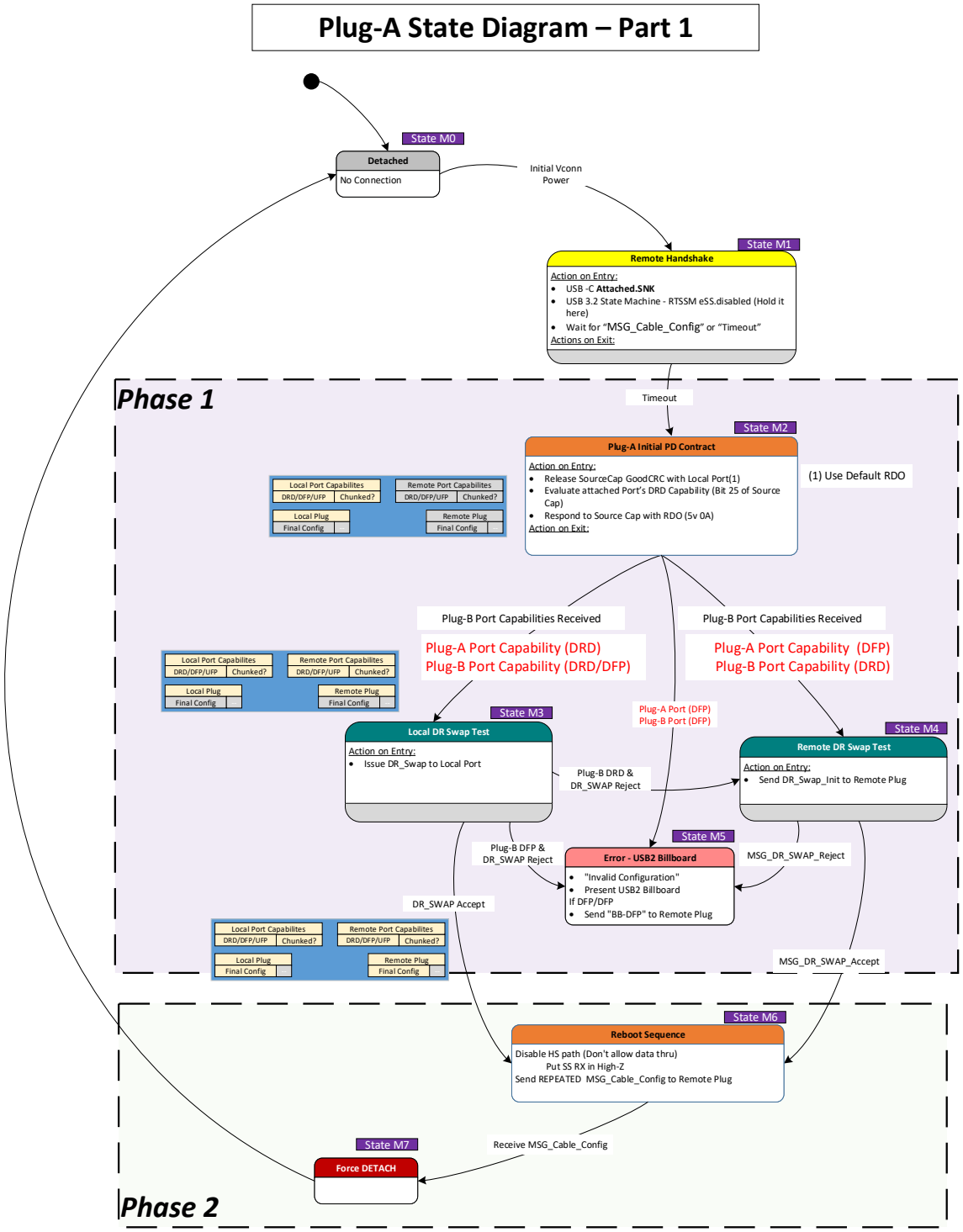
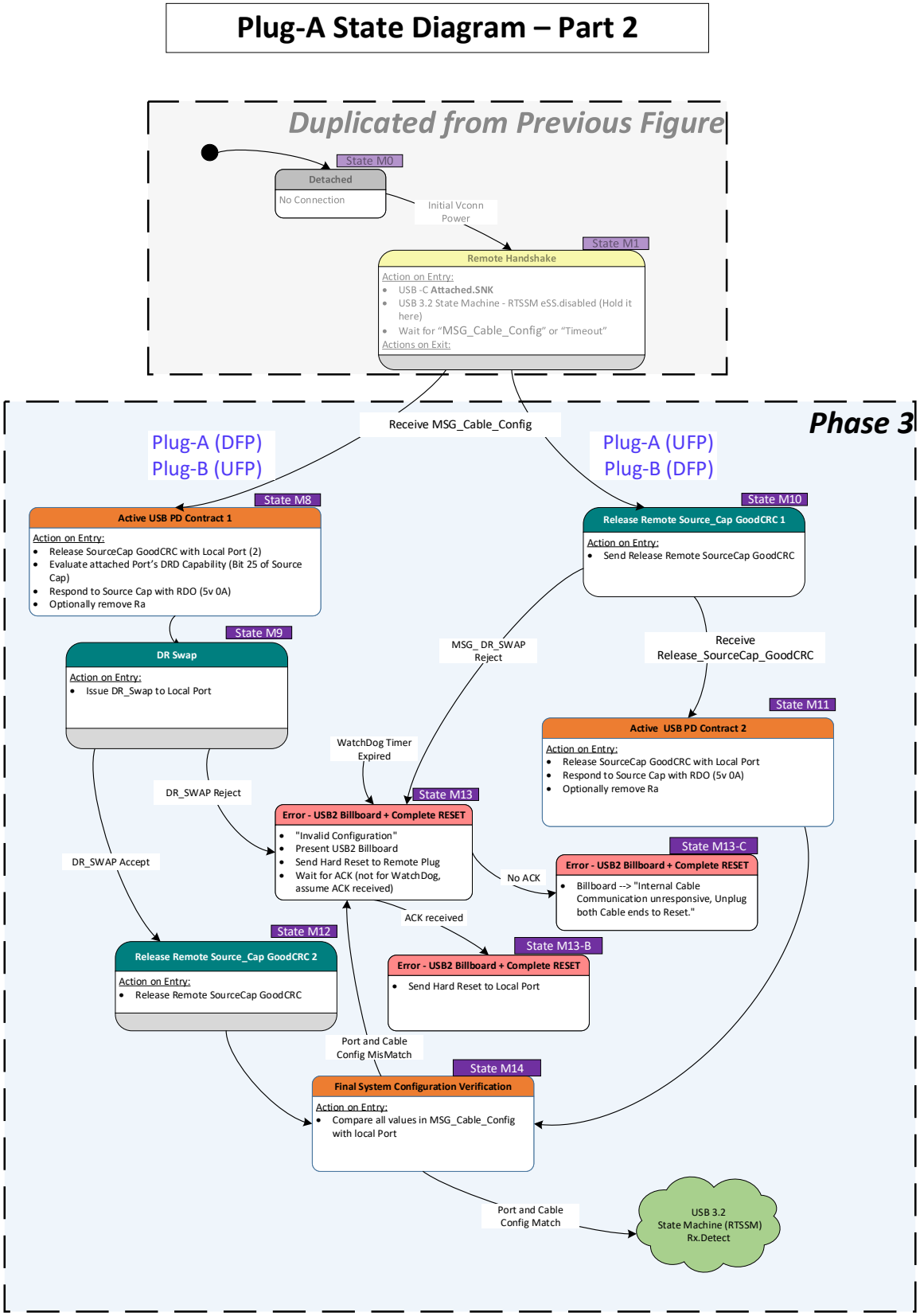


Figure 6-16 OIAC Plug-A State Diagram Part 2 (Phase 3)



6.3.6.4.1 Detached State (M0)

The plug is in ***Detached*** (M0) when no power is applied. The plug transitions to ***Remote Handshake*** (M1) when VCONN is applied.

6.3.6.4.2 Remote Handshake State (M1)

The plug is waiting for the "Timeout" timer expiration or a "MSG_Cable_Config" message from Plug-B.

Recommended Timeout time = ~100ms

The Timeout time is dependent on the duty cycle of Plug-B's Repeat Port Capabilities messages and the maximum cable latency.

The plug starts in the *USB 3.2* RTSSM eSS.Disabled and remains in eSS.Disabled until cable initialization is complete at the end of Phase 3.

6.3.6.4.2.1 Entry to Remote Handshake

The plug enters Attached.SNK followed by entry to ***Remote Handshake*** (M1).

6.3.6.4.2.2 Exit from Remote Handshake

The plug transitions to:

- ***Plug-A Initial PD Contract*** (M2) when the "Timeout" timer has expired,
- ***Active USB PD Contract 1*** (M8) upon receipt of a "MSG_Cable_Config" message when Plug-A resolves to a DFP and Plug-B will resolve to a UFP, or
- ***Release Remote Source_Cap GoodCRC 1*** (M10) upon receipt of a "MSG_Cable_Config" message when Plug-A resolves to a UFP and Plug-B will resolve to a DFP.

6.3.6.4.3 Plug-A Initial PD Contract State (M2)

When the plug is in ***Plug-A Initial PD Contract***, the plug has established an initial *USB PD* contract and evaluated its local port's DRD capability.

6.3.6.4.3.1 Entry to Plug-A Initial DP Contract

On Entry to ***Plug-A Initial PD Contract***, the plug shall:

1. Send a GoodCRC in response to a Source Capabilities message from the local attached port
2. Evaluate the local attached port's DRD capability (as indicated in the Source Capabilities message)
3. Respond to the Source Capabilities message with the "default" RDO specified in Table 6-11.

6.3.6.4.3.2 Exit from Plug-A Initial DP Contract

The OIAC plug shall transition to:

- ***Local DR Swap Test*** (M3) upon receipt of a MSG_Port_Capabilities where the Plug-A port is a DRD and the Plug-B port is either a DRD or DFP,

- ***Remote DR Swap Test*** (M4) upon receipt of a MSG_Port_Capabilities where the Plug-A port is a DFP and the Plug-B port is DRD, or
- ***Error – USB2 Billboard*** (M5) upon determination both Plug-A and Plug-B are connected to DFPs.

6.3.6.4.4 Local DR Swap Test State (M3)

The ***Local DR Swap Test*** is a test to ensure that the Plug-A port that is defined as a DRD will accept a DR_Swap request.

6.3.6.4.4.1 Entry to Local DR Swap Test

On entry to ***Local DR Swap Test***, the plug shall issue DR_Swap request to its local port.

If the local port responds to the DR Swap with "Wait," then the plug shall follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state ***Error – USB2 Billboard*** (M5).

6.3.6.4.4.2 Exit from Local DR Swap Test

The OIAC plug shall transition to:

- ***Remote DR Swap Test*** (M4) upon receipt of a Reject and the Plug-B port reported that it is a DRD,
- ***Error – USB2 Billboard*** (M5) upon receipt of a Reject and the Plug-B port reported that it is a DFP, or
- ***Reboot Sequence*** (M6) upon receipt of an Accept.

6.3.6.4.5 Remote DR Swap Test State (M4)

The ***Remote DR Swap Test*** is a test to ensure that the Plug-B port that is defined as a DRD will accept a DR_Swap request.

6.3.6.4.5.1 Entry to Remote DR Swap Test

On entry to ***Remote DR Swap Test***, the plug shall issue a DR_Swap_Init to the remote plug.

6.3.6.4.5.2 Exit from Remote DR Swap Test

The OIAC plug shall transition to:

- ***Reboot Sequence*** (M6) upon receipt of a MSG_DR_Swap_Accept, or
- ***Error – USB2 Billboard*** (M5) upon receipt of a MSG_DR_Swap_Reject.

6.3.6.4.6 Error – USB2 Billboard (M5)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: A DFP only device connected to one of the plugs."

6.3.6.4.6.1 Entry to Error – USB2 Billboard

On entry ***Error – USB2 Billboard***, the plug shall issue present a Billboard message over *USB 2.0* and then power down to its lowest possible state.

6.3.6.4.6.2 Exit from Error – USB2 Billboard

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.

6.3.6.4.7 Reboot Sequence State (M6)

When the plug is in the ***Reboot Sequence***, it will disable the High Speed Data path and start to initiate a remote plug reboot.

6.3.6.4.7.1 Entry to Reboot Sequence

On entry to Reboot Sequence, the plug shall:

1) Disable the HS path by changing the SS RX termination to High-Z.
2) Determine and store the final System Configuration for this link.
    a. The System Configuration will contain:
        i. Host/Device Port information
        ii. Final Plug-A/Plug-B roles
            1. If coming from State M3
                a. Plug-A → DFP (DR_Swap)
                b. Plug-B → UFP
            2. If coming from State M4
                a. Plug-A → UFP
                b. Plug-B → DFP (DR_Swap)
            3. If coming from State M9
                a. Plug-A → UFP
                b. Plug-B → DFP (DR_Swap)
3) Continuously send "MSG_Cable_Config" message to the remote plug.

6.3.6.4.7.2 Exit from Reboot Sequence

The OIAC plug shall transition to the ***Force Detach*** (M7) when a "MSG_Cable_Config" message is received that matches the final configuration that Plug-A sent to Plug-B.

6.3.6.4.8 Force Detach State (M7)

The plug shall transition to SRC.Open on both CC and VCONN and maintain this state for at least tSRCDisconnect.

6.3.6.4.8.1 Entry to Force Detach

On entry to ***Force Detach***, the plug shall raise the voltage on the CC-wire above vRd-Connect.

6.3.6.4.8.2 Exit from Force Detach

The plug transitions to ***Detached*** upon exit from ***Force Detach***.

6.3.6.4.9 Active USB PD Contract 1 State (M8)

Active USB Contract 1 is where OIAC Plug-A creates at *USB PD* contract with the local port.

6.3.6.4.9.1 Entry to Active USB PD Contract 1

The OIAC plug shall follow the steps listed below:

1. Begin responding to *USB PD* messages from its port partner with GoodCRCs.
2. Evaluate Fixed 5V PDO in the Source Capabilities message to check if its port partner is a DRD.
3. Request for a 5 V @ 0 A power contract.
4. May remove Ra to save power.

6.3.6.4.9.2 Exit from Active USB PD Contract 1

The plug transitions to the ***DR Swap*** (M9) when it receives an Accept followed by a PS_RDY message from its port partner.

6.3.6.4.10 DR Swap State (M9)

The ***DR Swap*** is used to set the final data role of the OIAC's Plug-A and signal to the OIAC Plug-B to complete its configuration.

6.3.6.4.10.1 Entry to DR Swap

The OIAC plug shall issue a DR_Swap to its port partner.

If the local port responds to the DR_Swap with "Wait," then the plug shall follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state ***Error – USB2 Billboard*** (M5).

6.3.6.4.10.2 Exit from DR Swap

If the DR_Swap message is responded to with:

- An Accept, it shall transition to the ***Release Remote Source_Cap GoodCRC 2 State*** (M12), or
- A Reject it shall transition to the ***Error - USB2 Billboard + Complete Reset*** (M13).

6.3.6.4.11 Release Remote Source_Cap GoodCRC 1 State (M10)

The OIAC is waiting to for Release_Remote_Source_Cap_GoodCRC to better synchronize the power on of the two OIAC plug ends.

6.3.6.4.11.1 Entry to Release Remote Source_Cap GoodCRC 1

The OIAC plug shall release the Remote SourceCap GoodCRC.

6.3.6.4.11.2 Exit from Release Remote Source_Cap GoodCRC 1

The OIAC plug shall transition to:

- ***Active USB PD Contract 2 State*** (M11), when a "MSG_ Release_Remote_SourceCap_GoodCRC" message is received, or
- ***Error – USB2 Billboard + Complete Reset*** (M13) upon receipt of a MSG_DR_Swap_Reject.

6.3.6.4.12 Active USB PD Contract 2 State (M11)

Active USB Contract 2 is where OIAC Plug-A creates at *USB PD* contract with the local port and should end with viable link.

6.3.6.4.12.1 Entry to Active USB PD Contract 2

The OIAC plug shall follow the steps listed below:

1. Begin responding to USB PD messages from its port partner with GoodCRCs.
2. Request a 5 V @ 0 A power contract.
3. May remove Ra to save power.

6.3.6.4.12.2 Exit from Active USB PD Contract 2

The plug shall transition to ***Final System Configuration Verification*** (M13) for final system verification.

6.3.6.4.13 Release Remote Source_Cap GoodCRC 2 State (M12)

OIAC Source Plug configuration is completed and the *USB 3.2* begins looking for a connection.

6.3.6.4.13.1 Entry to Release Remote Source_Cap GoodCRC 2

The OIAC plug shall release the Remote SourceCap GoodCRC.

6.3.6.4.13.2 Exit from Release Remote Source_Cap GoodCRC 2

The plug shall transition to ***Final System Configuration Verification*** (M13) for final system verification.

6.3.6.4.14 Error – USB2 Billboard + Complete Reset (M13)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: An invalid configuration occurred. Full link will be reset."

6.3.6.4.14.1 Entry to Error – USB2 Billboard + Complete Reset (M13)

On entry Error – USB2 Billboard + Complete Reset, the plug shall:

1) Present a USB2 Billboard message
2) Send a MSG_Hard_Reset to the remote Plug
3) Wait for Hard Reset Ack from Remote Plug (Unless entry is from an expired WatchDog Timer, in which case, go directly to M13-B)

   Received ACK (State M13-B):

4) Send Hard Reset to the Local Port

   Did NOT receive ACK (State M13-C):

5) Present USB2 Billboard Message: "Error: Internal Cable Communication Error. Unplug both cable ends to reset."

6.3.6.4.14.2 Exit from Error – USB2 Billboard + Complete Reset (M13 B/C)

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power from each port.

6.3.6.4.14.3 WatchDog Timer Entry

A watchdog timer should be implemented for internal cable messages that require a response. The watchdog timer will also provide an entry to an ***Error State*** (M13) if the far end plug is unresponsive for any reason.

There are a few states where the watchdog timer shall NOT be implemented including but not limited to M2, where it is possible that only a single end of the OIAC is connected and M6, where the reboot sequence can take a few seconds.

6.3.6.4.15 Final System Configuration Verification (M14)

Final System Configuration Verification is used to do one final check there were no unforeseen changes the local port and the final cable configuration defined by Plug-A.

6.3.6.4.15.1 Entry to Final System Configuration Verification

The OIAC plug shall check all values in the MSG_Cable_Config match that of the current local port's configuration.

6.3.6.4.15.2 Exit from Final System Configuration Verification

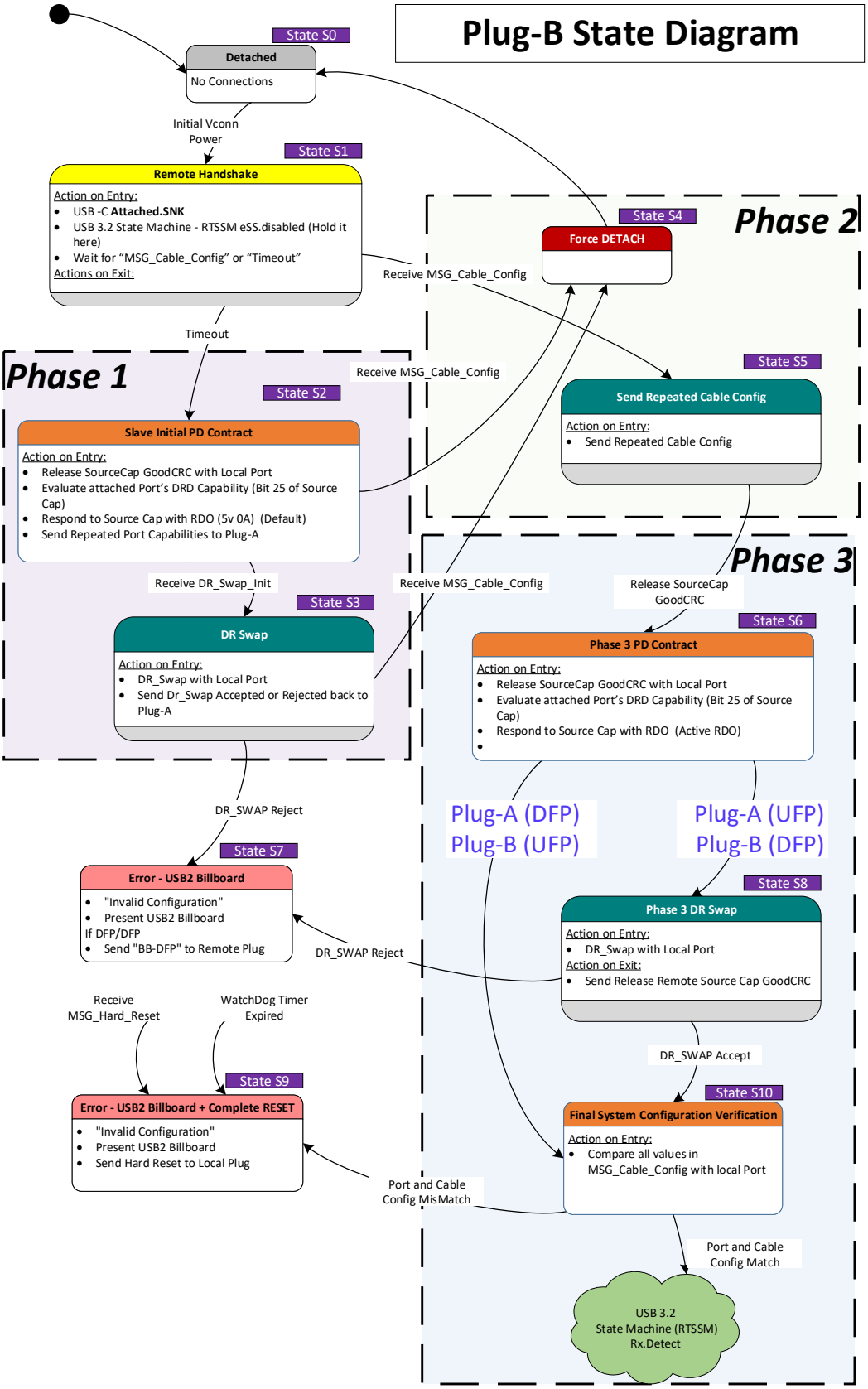
The plug shall transition to:

- ***Rx.Detect***, and start far-end receiver termination detection and the *USB 3.2* RTSSM State Machine after a successful match of the MSG_Cable_Config and the local port's configuration, or
- ***Error - USB2 Billboard + Complete RESET*** (State M14) after unsuccessful match of the MSG_Cable_Config and the local port's configuration.

6.3.6.5 OIAC Connection State Diagram Plug-B

The following sections details a possible OIAC state diagram for Plug-B.

Figure 6-17 OIAC Plug-B State Diagram


Plug-B State Diagram
State S0
Detached
No Connections
Initial Vconn Power
State S1
Remote Handshake
Action on Entry:
USB -C Attached.SNK
USB 3.2 State Machine - RTSSM eSS.disabled (Hold it here)
Wait for "MSG_Cable_Config" or "Timeout"
Actions on Exit:
Timeout
Phase 1
State S2
Slave Initial PD Contract
Action on Entry:
Release SourceCap GoodCRC with Local Port
Evaluate attached Port's DRD Capability (Bit 25 of Source Cap)
Respond to Source Cap with RDO (5v 0A) (Default)
Send Repeated Port Capabilities to Plug-A
Receive DR_Swap_Init
State S3
DR Swap
Action on Entry:
DR_Swap with Local Port
Send Dr_Swap Accepted or Rejected back to Plug-A
Receive MSG_Cable_Config
Phase 2
State S4
Force DETACH
Receive MSG_Cable_Config
State S5
Send Repeated Cable Config
Action on Entry:
Send Repeated Cable Config
Receive MSG_Cable_Config
Phase 3
Release SourceCap GoodCRC
State S6
Phase 3 PD Contract
Action on Entry:
Release SourceCap GoodCRC with Local Port
Evaluate attached Port's DRD Capability (Bit 25 of Source Cap)
Respond to Source Cap with RDO (Active RDO)
Plug-A (DFP)
Plug-B (UFP)
Plug-A (UFP)
Plug-B (DFP)
State S8
Phase 3 DR Swap
Action on Entry:
DR_Swap with Local Port
Action on Exit:
Send Release Remote Source Cap GoodCRC
DR_SWAP Reject
State S7
Error - USB2 Billboard
"Invalid Configuration"
Present USB2 Billboard
If DFP/DFP
Send "BB-DFP" to Remote Plug
DR_SWAP Reject
DR_SWAP Accept
State S10
Final System Configuration Verification
Action on Entry:
Compare all values in MSG_Cable_Config with local Port
Port and Cable Config MisMatch
Port and Cable Config Match
USB 3.2 State Machine (RTSSM) Rx.Detect
Receive MSG_Hard_Reset
WatchDog Timer Expired
State S9
Error - USB2 Billboard + Complete RESET
"Invalid Configuration"
Present USB2 Billboard
Send Hard Reset to Local Plug

6.3.6.5.1 Detached State (S0)

The plug is in ***Detached*** (S0) when no power is applied. The plug transitions to ***Remote Handshake*** (S1) when VCONN is applied.

6.3.6.5.2 Remote Handshake State (S1)

The plug is waiting for the "Timeout" timer expiration or a "MSG_Cable_Config" message from Plug-A.

Recommended Timeout time = ~100ms

The Timeout time is dependent on the duty cycle of the Plug-A's Repeat MSG_Cable_Config messages and the maximum cable latency.

6.3.6.5.2.1 Entry to Remote Handshake

The plug enters Attached.SNK followed by entry to ***Remote Handshake*** (S1).

The plug starts in the USB 3.2 RTSSM eSS.Disabled and remains in eSS.Disable until cable initialization is complete at the end of Phase 3.

6.3.6.5.2.2 Exit from Remote Handshake

The plug transitions to:

- ***Plug-B Initial PD Contract*** (S2) when the "Timeout" timer has expired, or
- ***Send Repeated Cable Config*** (S5) upon receipt of a "MSG_Cable_Config" message.

6.3.6.5.3 Plug-B Initial DP Contract (S2)

The plug takes the following actions in the order defined:

1. Send a GoodCRC in response to a Source Capabilities message from the local attached port.
2. Evaluate the local attached port's DRD Capability (as indicated in the Source Capabilities message).
3. Send the initial RDO (5 V/0 A) and negotiate an explicit power contract.
4. Send "MSG_Port_Capabilities" to Plug-A. The plug shall continue to send "MSG_Port_Capabilities" until it exits this state.

6.3.6.5.3.1 Entry to Plug-B Initial DP Contract

The plug enters ***Plug-B Initial PD Contract*** (S2) upon "Timeout" timer expiration.

6.3.6.5.3.2 Exit from Plug-B Initial DP Contract

The plug transitions to:

- ***DR Swap*** (S3) upon receipt of a "DR_Swap_Init" message from Plug-A, or
- ***Force Detach*** (S4) upon receipt of a "MSG_Cable_Config" message from Plug-A.

6.3.6.5.4 DR Swap (S3)

The plug determines if a DR_Swap can be performed with the local attached port or Plug-A configured itself.

6.3.6.5.4.1 Entry to DR Swap

Upon entry into DR Swap (S3) the plug shall:

1. Send DR_Swap message to the local attached port.
2. Send MSG_DR_Swap_Accept when the plug receives Accept message from the local attached port.
3. Send MSG_DR_Swap_Reject when the plug receives Reject message from the local attached port.

If the local port responds to the DR Swap with "Wait," then the plug shall follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state ***Error – USB2 Billboard*** (S7).

6.3.6.5.4.2 Exit from DR Swap

The plug shall transition to:

- ***Error – USB2 Billboard*** (S7) upon rejection of the local attached port DR_Swap, or
- ***Force Detach*** (S4) upon receipt of a "MSG_Cable_Config" message from Plug-A.

6.3.6.5.5 Force Detach (S4)

The plug shall transition to SRC.Open on both CC and VCONN and maintain this state for at least tSRCDisconnect.

6.3.6.5.5.1 Entry to Force Detach

The plug enters ***Force Detach*** (S4) upon receipt of a "MSG_Cable_Config"" message from Plug-A.

6.3.6.5.5.2 Exit from Force Detach

The plug transitions to ***Detached*** (S0) upon exit from ***Force Detach***.

6.3.6.5.6 Send Repeated Cable Config (S5)

The plug repeatedly sends "MSG_Cable_Config" messages in this state to inform Plug-A of the configuration of the local attached port.

6.3.6.5.6.1 Entry to Send Repeated Cable Config

The plug enters ***Repeated Cable Config*** (S5) upon receipt of a "MSG_Cable_Config" message from Plug-A.

6.3.6.5.6.2 Exit from Send Repeated Cable Config

The plug transitions to ***Phase 3 PD Contract*** (S6) upon receipt of a "Release SourceCap GoodCRC" message from the Plug-A port.

6.3.6.5.7 Phase 3 PD Contract (S6)

The plug performs the following actions in this state:

1. Send a GoodCRC in response to a Source Capabilities message from the local attached port.

2. Evaluate the attached local attached port's DRD Capability (as indicated in the Source Capabilities message).
3. Send the initial RDO (5 V/0 A) in response to the Source Capabilities message and negotiate an explicit power contract.

6.3.6.5.7.1 Entry to Phase 3 PD Contract

The plug enters ***Phase 3 PD Contract*** upon receipt of a "Release SourceCap GoodCRC" message from Plug-A.

6.3.6.5.7.2 Exit from Phase 3 PD Contract

The plug transitions to:

- ***Final System Configuration Verification*** (S10) for final system verification upon determination Plug-A is acting as a DFP and it is acting as a UFP, or
- ***Phase 3 DR Swap*** (S8) upon determination Plug-A is acting as a UFP and it is acting as a DFP.

6.3.6.5.8 Error – USB2 Billboard (S7)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: A DFP only device connected to one of the plugs."

6.3.6.5.8.1 Entry to Error – USB2 Billboard

The plug transitions to this state upon rejection of a DR_Swap by the local attached port.

6.3.6.5.8.2 Exit from Error – USB2 Billboard

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.

6.3.6.5.9 Phase 3 DR Swap State (S8)

The plug issues a DR_Swap with its local attached port in this state.

6.3.6.5.9.1 Entry to Phase 3 DR Swap

The plug enters ***Phase 3 DR Swap*** upon determination Plug-A is connected as a UFP and Plug-B should connect as a DFP.

6.3.6.5.9.2 Exit from Phase 3 DR Swap

The plug shall transition to:

- ***Final System Configuration Verification*** (S10) for final system verification after successful completion of the DR_Swap with the local attached port, or
- ***Error – USB2 Billboard*** (S7) after unsuccessful completion of the DR_Swap with the local attached port.

6.3.6.5.10 Error – USB2 Billboard + Complete RESET (S9)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: An invalid configuration occurred. Full link will be reset."

6.3.6.5.10.1 Entry to Error – USB2 Billboard + Complete RESET

On entry ***Error – USB2 Billboard + Complete RESET***, the plug shall:

1. Present a USB2 Billboard message.
2. Send Hard_Reset to the Local Plug.

6.3.6.5.10.2 Exit from Error – USB2 Billboard + Complete RESET

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.

6.3.6.5.10.3 WatchDog Timer Entry

A watchdog timer should be implemented for internal cable messages that require a response. The watchdog timer will also provide an entry to an ***Error State*** (M13) if the far end plug is unresponsive for any reason.

There are a few states where the watchdog timer shall NOT be implemented including but not limited to S5, where the reboot sequence can take a few seconds.

6.3.6.5.11 Final System Configuration Verification (S10)

The ***Final System Configuration Verification*** is used to one final check there were no unforeseen changes the local port and the final cable configuration defined by Plug-A.

6.3.6.5.11.1 Entry to Final System Configuration Verification

The OIAC plug shall check all values in the MSG_Cable_Config match that of the current local port's configuration.

6.3.6.5.11.2 Exit from Final System Configuration Verification

The plug shall transition to:

- ***Rx.Detect***, and start far-end receiver termination detection and the *USB 3.2* RTSSM State Machine after a successful match of the MSG_Cable_Config and the local port's configuration, or
- ***Error – USB2 Billboard + Complete RESET*** (State S9) after unsuccessful match of the MSG_Cable_Config and the local port's configuration.

6.3.6.6 OIAC Connection Flow for USB4

There is no additional unique link sequencing needed to bring the link up for USB4. This is assuming that the OIAC supports USB4 operations and is able to handle all USB4 messages as defined in Section 6.5.2

6.3.7 Additional Electrical Requirements for OIAC

6.3.7.1 Shielding Effectiveness Requirement

OIAC shall meet the shielding effectiveness requirement defined in Section 3.7.7 and Figure 3-65.

6.3.7.2 Low Speed Signal Requirement

6.3.7.2.1 CC Channel Requirements

Active cables shall meet the Low-Speed Signal Requirements in Section 3.7.2.4.

6.3.7.2.2 SBU Requirements

6.3.7.2.2.1 USB3.2

OIACs are not required to support SBU1/2 for *USB 3.2* support. SBUs are not usable until the cable has entered an Alternate Mode. OIACs which choose to support SBU signals shall meet the requirements of the Alternate Mode(s) they support. Definition of the SBU requirements for Alternate Modes is outside the scope of this document.

6.3.7.2.2.2 USB4

OIACs shall support SBTx and SBRx for USB4 support.

Any additional support for the SBx signaling is not OIACs

SBx's shall meet the same voltage swing requirements as Active cables as defined in Table 6-16.

6.3.7.3 USB 2.0

The OIAC is not required to support USB2.0, therefore USB2.0 is NOT expected to work.

The OIAC will take action to reset the link when the USB Device drops from *USB 3.2* to *USB 2.0*.

During the initial connection the OIAC shall present as a *USB 2.0* DFP and provide a 15K Ohm pull down on the D+/D– pins on both ends of the cable. The cable plug shall not issue a *USB 2.0* Reset in this state.

The OIAC cable plug shall issue a *USB 2.0* Reset upon detecting a *USB 2.0* connection on D+/D– (LS, FS, or HS *USB 2.0* connection). The cable plug shall issue a *USB 2.0* Bus Reset by pulling D+ and D– low for at least 50 ms.

The OIAC shall implement a tDisableCount counter to determine how many times the cable has transitioned from *USB 3.2* to *USB 2.0*. The tDisableCount counter shall be reset to zero on either condition:

- Power on Reset of the OIAC, or
- Successful transition to *USB 3.2* U0.

The OIAC shall present and latch a *USB 2.0* billboard when tDisableCount counter reaches three.

6.3.7.4 USB 3.2

OIAC shall meet the requirements in this section regardless of length. OIACs shall incorporate AC-coupling from the plug to repeater on both the *USB 3.2* TX and RX signals. OIACs shall provide a discharge path for discharging the AC-coupling capacitors in the cable on unplug per *USB 3.2*.

6.3.7.4.1 USB 3.2 Power-on and Rx.Detect

OIAC shall have the same power-on and far-end receiver termination as defined for the Active Cable defined in section 6.2.5.4.2.

OIACs shall reflect the receiver terminations across the cable to replicate the behavior of a passive cable.

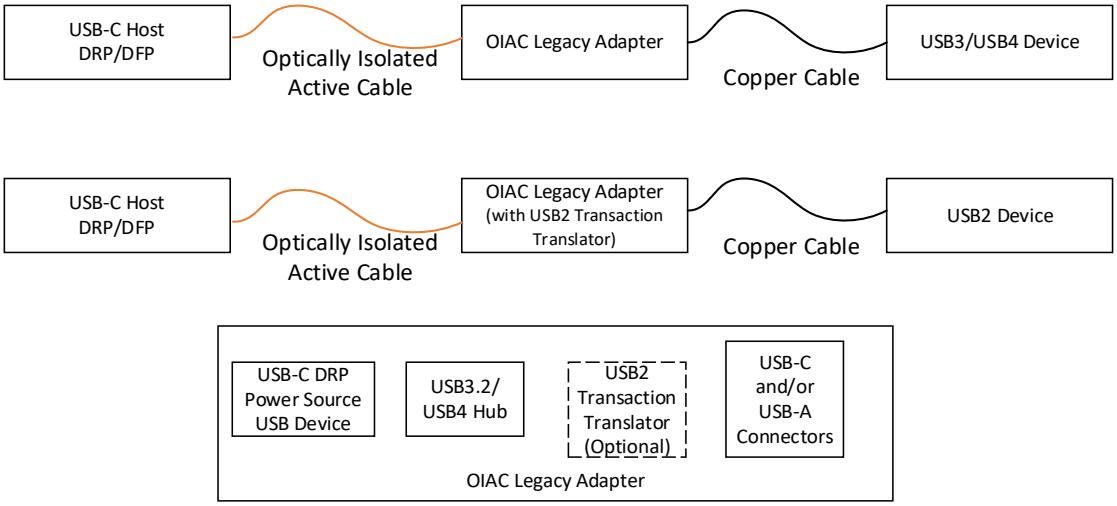
6.3.7.4.2 OIAC Legacy Adapter

The OIAC Legacy Adapter is specified here to provide a way to connect to a USB3/4 device that does not support OIACs. This adapter will need to be place between the OIAC and the device.

The OIAC Adapter requires the following capabilities:

1. USB Type-C DRP/Source on the upward facing port connected to the OIAC, (Self-Powered)
2. Self-Powered
    a. Need to power the upstream OIAC
    b. Needs to be able to power downstream device
3. *USB PD* on the upward facing port connected to the OIAC,
4. *USB 3.2* Hub
5. USB4 Hub (optional)
6. Optional: *USB 2.0* to *USB 3.2* transaction translator on the downstream facing port (only needed if connecting to *USB 2.0*-only devices, hubs, or hosts).

Figure 6-19 Illustrations of Usages for OIAC That Require an Adapter or Hub



6.3.7.4.3 USB 3.2 U-State Power Requirements

OIACs shall meet the VCONN power requirements for *USB 3.2* operation in Table 6-x. These requirements are for the entire cable not just a cable plug.

Table 6-x USB 3.2 OIAC U-State Requirements

State	Maximum Power Consumption VCONN	Power Consumption Notes
U0	1.0 W single-lane 1.5 W dual-lane	Applies to POLLING.LFPS, TRAINING, and RECOVERY states.
U1	≤ U0 power	Forwarding LFPS is required
U2	≤ U0 power	Forwarding LFPS is required
U3	≤ U0 power	Steady state power. eMarker in sleep.
Rx.Detect	≤ U0 power	Rx.Detect period may be lengthened when no *USB 3.2* terminations have been detected. eMarker in sleep.
eSS.Disabled	≤ U0 power	*USB 3.2* is disabled. eMarker in sleep.

6.3.7.4.4 USB 3.2 U-State Exit Latency

TBD

6.3.7.4.5 USB 3.2 Signal Swing

OIACs shall meet all the same electrical characteristics for USB3.2 Signal Swing as an active cable defined in Section 6.2.5.4.6.

6.3.7.5 USB4

The Optical Isolated Active Cable for USB4 is defined as a Linear Optical Active Cable. The electrical specification for USB4 is still being defined.

6.3.7.6 AC Coupling Capacitors

OIAC shall include AC-coupling capacitance between 135 nF and 265 nF inside their plugs placed at the output transmit path and between 300 nF and 363 nF at the input receive path. Discharge resistors between 200 KΩ and 242 KΩ shall be placed at the input receive path. See Figure 3-3 in the *USB4* specification for a diagram of the AC-coupling capacitors and discharge resistors.

6.3.7.7 USB4 CL-State Power Requirements

OIACs are not required to meet the same CL-State power requirements as active cables.

The OIACs shall meet the VCONN power requirements for *USB4* operation in Table 6-32. These requirements are for the entire cable not just a cable plug.

Table 6-32 USB4 CL-State Requirements

State	Maximum Power Consumption V_{CONN}	Power Consumption Notes
CL0	1.5 W	Applies to training states and CL0.
CL0s	≤ CL0 power	
CL1	≤ CL0 power	
CL2	≤ CL0 power	
CLd	≤ CL0 power	Steady state power

6.3.7.8 Return Loss

Return loss is defined in the *USB 3.2* specification.

6.3.8 Mechanical

All mechanical specifications for the OIAC are the same as all other Active Cables. Please refer to section 6.2.6.

Additional requirements for the OIAC are listed in this section.

6.3.8.1 Thermal

6.3.8.2 Thermal Shutdown

OIACs shall billboard in shutdown to both ports, regardless of which end of the cable plug is in thermal shutdown. For example: "Error: The Optical Cable has experienced a thermal shutdown."

6.3.8.3 Maximum Skin Temperature

OIAC plug's skin temperature shall not exceed a maximum operating temperature of 30 °C above the ambient temperature for a plastic/rubber housing and 15 °C for a metal housing in any operating mode.

6.3.8.4 Thermal Reporting

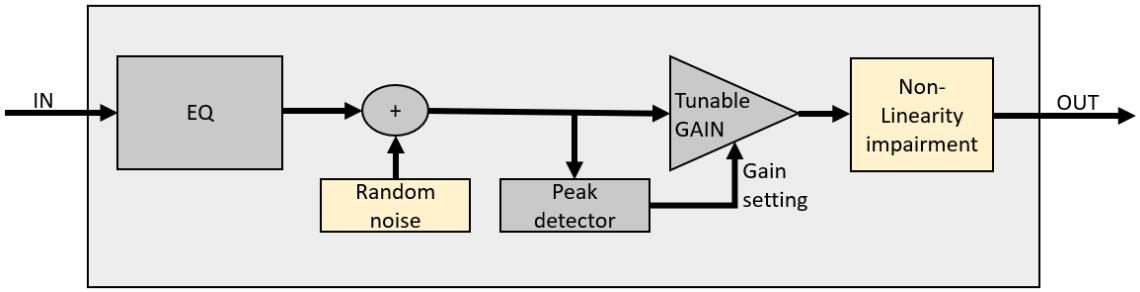
The OIAC shall implement reporting their maximum internal operating temperature in the *USB PD* ***Discover_ID*** Command.

The OIAC shall report their current internal operating temperature (of the higher of the two cable plugs) in the *USB PD* ***Get_Status*** Command on SOP'.

Appendix J
Design assumptions for the USB4-Gen4 LRD cable spec

This appendix describes the design assumptions that was used during the spec development of the Gen4 LRD cable. The description here is informative only and might be use as a referencefor design and/or system simulations.

This is the LRD IC model used for the spec development:



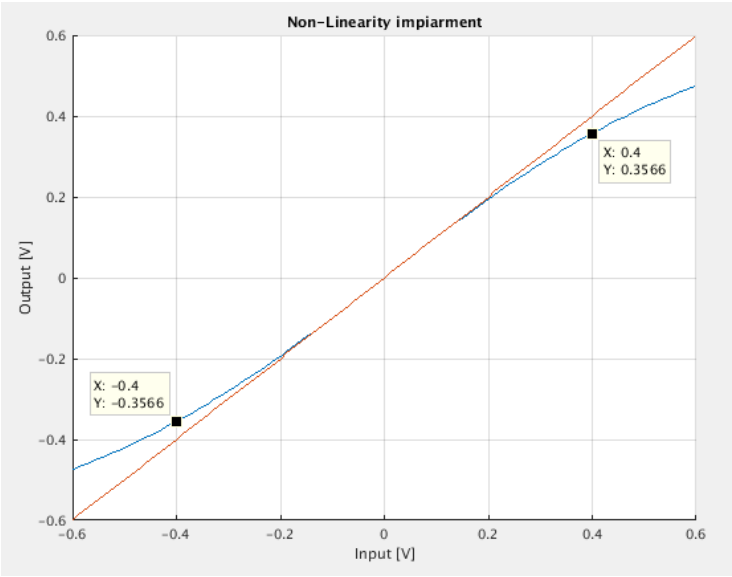
The following parameters where assumed:

1) Reference ctle is given by:

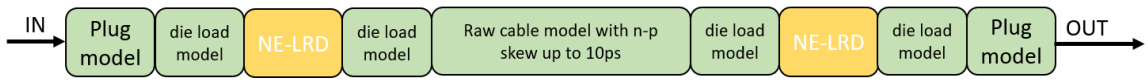
$$H(s) = \omega_{p2} \cdot \frac{S+10^{\frac{A_{DC}}{20}} \cdot \omega_{p1}}{(S+\omega_{p1}) \cdot (S+\omega_{p2})}$$

   a. Where:
      i. A_{DC} is the DC gain (in dB)
      ii. S is the frequency in Laplace domain
      iii. $\omega_{p1} = 2 \cdot \pi \cdot 4.26e9 \ \frac{rad}{sec}$
      iv. $\omega_{p2} = 2 \cdot \pi \cdot 20e9 \ \frac{rad}{sec}$

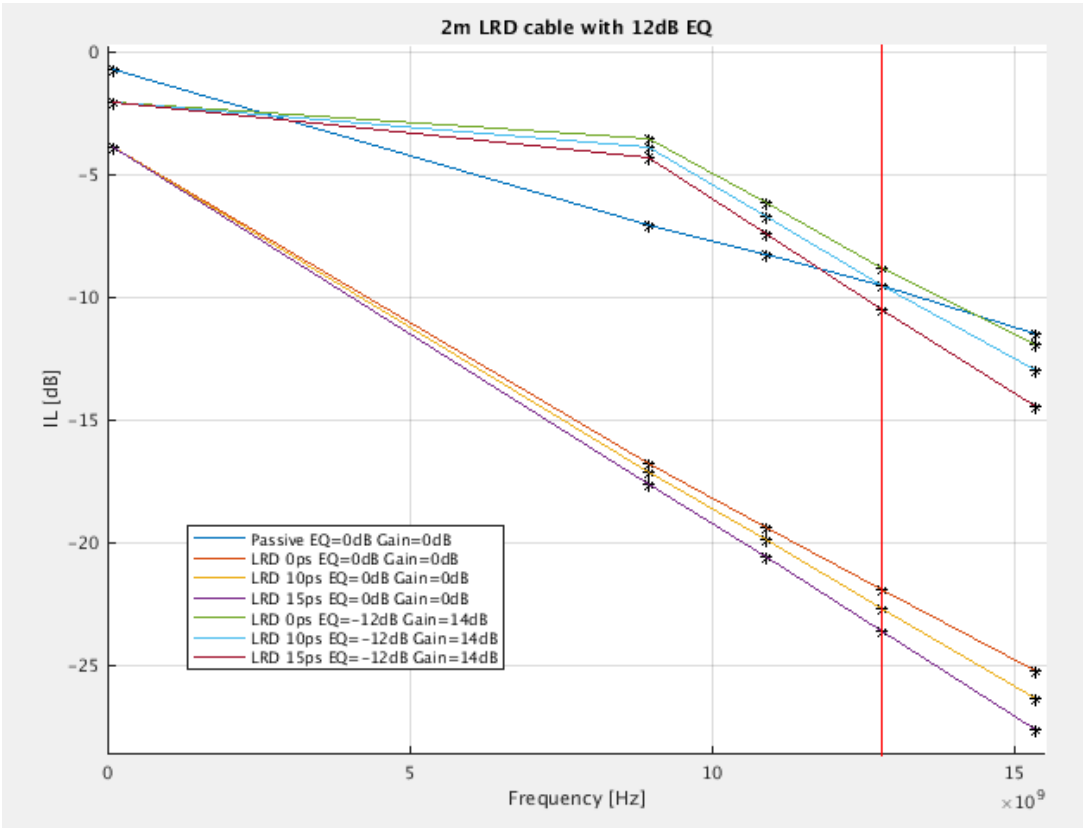
2) Random noise injection with 1.2mV
3) Tunable gain controlled by peak detector with thrashold set to 700mV-pp
4) Gain limit of 8dB
5) Non-linearity modeling with 1.53*tanh*(1/1.53)
   a. This reflect 1dB compression point of 800mV-pp (referred to input)



This is the cable system model used for the spec development:



The settings of the NE (near end- i.e. closer to the TX) and FE (far end – i.e. closer to the rX) LRD's is as following:

1) NE EQ settings: $A_{DC} = -7dB$
2) FE EQ settings: $A_{DC} = -5dB$
3) Self-tuned gain enabled in both NE and FE LRD's
4) Raw cable n-p skew is limited to 10ps

The response of the cable including the LRD's EQ and gain is: