USB 2.0 Electrical Compliance Test Specification

Version 1.07

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1 Summary

This document provides the compliance criteria and test descriptions for USB 2.0 high-speed electrical testing, full-speed electrical testing, and low-speed electrical testing. It is relevant for anyone building USB 2.0 silicon, USB 2.0 devices, USB 2.0 hubs or USB 2.0 hosts. The document is divided into two major areas. The first is compliance criteria and the second is test description.

Compliance criteria are provided as a list of assertions that describe specific characteristics or behaviors that must be met. Each assertion provides a reference to the specification or other document from where the assertion was derived. Also each assertion provides a reference to the specific test description where the assertion is tested.

Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what a test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

This document reflects compliance updates announced at compliance.usb.org.

2 Full Speed and Low Speed Electrical Compliance

Upstream Facing Port Tests:

- Low-speed signal quality
- Full-speed signal quality
- Inrush
- Back Voltage (for self-powered or battery powered upstream facing ports only)

*Note: Perform all tests listed above on each UFP. Multiple upstream facing ports are only allowed on USB products with USB Type-C™ connectors and only USB Type-C™ connectors.

Downstream Facing Port Tests:

- Low-speed signal quality
- Full-speed signal quality
- Drop/Droop

*Note: Perform all tests listed above on each DFP.

3 High Speed Electrical Compliance

3.1 General

EL_1 All high-speed capable devices must support the specified test modes for their ports
Reference documents: *USB 2.0 Specification*, Section 7.1.20

3.2 Transmitting

EL_2 A USB 2.0 high-speed transmitter data rate must be 480 Mb/s +-0.05%
Reference documents: *USB 2.0 Specification*, Section 7.1.11
Test description: Section 4.1

EL_3 A USB 2.0 downstream facing port must meet Template 1 transform waveform requirements measures at TP2 (each hub downstream port)
Reference documents: *USB 2.0 Specification*, Section 7.1.2.2
Test description: Section 4.1.3

EL_4 A USB 2.0 upstream facing port on a device without a captive cable must meet Template 1 transform waveform requirements measured at TP3.
Reference documents: *USB 2.0 Specification*, Section 7.1.2.2
Test description: Section 4.1.1

EL_5 A USB 2.0 upstream facing port on a device with a captive cable must meet Template 2 transform waveform requirements measured at TP2.
Reference documents: *USB 2.0 Specification*, Section 7.1.2.2
Test description: Section 4.1.1

EL_6 A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 300 ps as per compliance update #87.
Reference documents: *USB 2.0 Specification*, Section 7.1.2.2
Test description: Section 4.1.1

EL_7 A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.
Reference documents: *USB 2.0 Specification*, Section 7.1.2.2
Test description: Section 4.1.1

EL_9 When either D+ or D- is not being driven, the output voltage must be 0V +-20mV when terminated with precision 45 ohm resistors to ground as per compliance update #92.
Reference documents: *USB 2.0 Specification*, Section 7.1.1.3
Test description: Section 4.3

3.3 Receiving

EL_16 A high-speed capable device must implement a transmission envelope detector that indicates squelch (i.e. never receives packets) when a receiver input falls below 100 mV differential amplitude.
Reference documents: *USB 2.0 Specification*, Section 7.1
Test description: Section 4.2.1

El_17 A high-speed capable device must implement a transmission envelope detector that does not indicate squelch (i.e. reliably receives packets) when a receivers input exceeds 150 mV differential amplitude.
Reference documents: *USB 2.0 Specification*, Section 7.1
Test description: Section 4.2.1

El_18 A high-speed capable device's Transmission Envelope Detector must be fast enough to allow the HS receiver to detect data transmission, achieve DLL lock, and detect the end of the SYNC field within 12 bit times.
Reference documents: *USB 2.0 Specification*, Section 7.1
Test description: Section 4.2.1

3.4 Packet Parameters

EL_21 The SYNC field for all transmitted packets (not repeated packets) must begin with a 32 bit SYNC field.
Reference documents: *USB 2.0 Specification*, Section 8.2.
Test description: Section 4.5.1

EL_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of at least 8 bit times and not more than 192 bit times.
Note that for a host that implements a built-in hub, the delay through the hub, both upstream and downstream (see EL_48) and round trip time through a 5 meter cable (26 ns * 2), must be added to these times making the maximum time 192bits + 72bits + 52ns + 8ns. This results in a maximum time of 610 ns or 292 bit times.
Reference documents: *USB 2.0 Specification*, Section 7.1.18.2
Test description: Section 4.5.1

EL_23 Hosts transmitting two packets in a row must have an inter-packet gap of at least 88 bit times and not more than 192 bit times.
Reference documents: *USB 2.0 Specification*, Section 7.1.18.2
Test description: Section 4.5.1

EL_25 The EOP for all transmitters' packets (except SOFs) must be an 8 bit NRZ byte of 01111111 without bit stuffing. (Note that a longer EOP is waiverable)
Reference documents: *USB 2.0 Specification*, Section 7.1.13.2
Test description: Section 4.5.1

3.5 Speed Detection

EL_27 Devices must transmit a chirp handshake no sooner than 3.1ms and no later than 6.0ms when being reset from a non-suspended high-speed mode. The timing is measured from the beginning of the last SOF transmitted before the reset begins.
Reference documents: *USB 2.0 Specification*, Section 7.1.7.5
Test description: Section 4.4.1

EL_28 Devices must transmit a chirp handshake no sooner than 2.5us and no later than 6.0ms when being reset from a suspended state. Devices must transmit a chirp handshake no sooner than 2.5us and no later than 3ms when being reset from a full speed state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5
Test description: Section 4.4.1

EL_29 The chirp handshake generated by a device must be at least 1ms and no more that 7ms in duration.
Reference documents: *USB 2.0 Specification*, Section 7.1.7.5
Test description: Section 4.4.1

EL_31 During device speed detection, when a device detects a valid K-J-K-J-K-J sequence, the device must disconnect its 1.5K pull-up resistor and enable it high-speed termination within 500us.
Reference documents: *USB 2.0 Specification*, Section 7.1.7.5
Test description: Section 4.4.1

EL_33 Downstream ports start sending an alternating sequence of Chirp K's and Chirp J's within 100us after the device Chirp k stops.
Reference documents: *USB 2.0 Specification*, Section 7.1.7.5
Test description: Section 4.4.1

EL_34 Downstream port Chirp K and Chirp J durations must be between 40us and 60us duration.
Reference documents: *USB 2.0 Specification*, Section 7.1.7.5
Test description: Section 4.4.1

EL_35 Downstream ports must begin sending SOF's no sooner than 100us and no later than 500us from transmission of the last Chirp (J or K).
Reference documents: *USB 2.0 Specification*, Section 7.1.7.5
Test description: Section 4.4.1

3.6 Suspend/Resume

EL_38 A device must revert to full-speed no later than 125us after there is a 3ms idle period on the bus (3.000ms <= t <= 3.125ms)
Reference documents: *USB 2.0 Specification*, Section 7.1.7.6
Test description: Section 4.6

EL_39 A device must support the Suspend state.
Reference documents: *USB 2.0 Specification*, Section 7.1.7.6
Test description: Section 4.6

EL_40 If a device is in the suspend state, and was operating in high-speed before being suspended, then the device must transition back to high speed operation within two bit times from the end of resume signaling.
Reference documents: *USB 2.0 Specification*, Section 7.1.7.7
Test description: Section 4.6

EL_41 After resuming a port, the host must begin sending SOF's within 3ms of the start of the idle state.
Reference documents: *USB 2.0 Specification*, Section 7.1.7.7
Test description: Section 4.6

3.7 High Speed Repeater

3.7.1 Sync Truncation

EL_42 Hub repeaters must not truncate more than 4 bits from a repeated SYNC pattern.
Reference documents: *USB 2.0 Specification*, Section 7.1.10
Test description: Section 4.7.1, 4.7.2

EL_43 Hubs must no corrupt any repeater bits of the SYNC field.
Reference documents: *USB 2.0 Specification*, Section 7.1.10
Test description: Section 4.7.1, 4.7.2

3.7.2 EOP Dribble

EL_44 A hub may add at most 4 random bits to the end of the EOP field when repeating a packet.
Reference documents: *USB 2.0 Specification*, Section 7.1.13.2
Test description: Section 4.7.1, 4.7.2

EL_45 A hub must not corrupt any of the valid EOP bits when repeating a packet.
Reference documents: *USB 2.0 Specification*, Section 7.1.13.2
Test description: Section 4.7.1, 4.7.2

3.7.3 Jitter

EL_46 A hub upstream facing repeater must meet Template 1 transform waveform requirements measured at TP3.
Reference documents: *USB 2.0 Specification*, Section 7.1.14.2
Test description: Section 4.1.1

EL_47 A hub downstream facing repeater must meet Template 1 transform waveform requirements measured at TP2 (each downstream port).
Reference documents: *USB 2.0 Specification*, Section 7.1.14.2
Test description: Section 4.1.2

3.7.4 Delay

EL_48 A hub repeater may not delay packets for more than 36 bit time plus 4ns.
Reference documents: *USB 2.0 Specification*, Section 7.1.14.2
Test description: Section 4.7.1, 4.7.2

3.8 Host requirements

3.8.1 EOP length for SOF's

EL_55 Hosts transmitting SOF packets must provide a 40 bit EOP without bit stuffing where the first symbol of the EOP is a transition from the last data symbol
Reference documents: *USB 2.0 Specification*, Section 7.1.13.2
Test description: Section 4.5.2

4 High Speed Electrical Test Description

4.1 High Speed Signal Quality

These tests measure the ability of transmitters to do valid high speed signaling. High speed signal quality is measured on both upstream and downstream ports. A high speed scope with a minimum bandwidth of 2.5 GHz with 50 ohm inputs is used. The connection to the test fixture is through high quality SMA cables. The signal quality is analyzed using the USB_IF tool USBET.

4.1.1 Upstream port

This test is run for all devices and hosts on their upstream port. For devices that have a captive cable, measurements use the far-end template in USBET.

a) Using HSET (or XHSET), place the port under test in Test Mode TEST_PACKET.
b) Isolate Device Under Test from system while maintaining bus power.
c) Capture waveform on the high speed oscilloscope.
d) Analyze waveform using USBET with appropriate settings for near end, far end, etc.

4.1.2 Downstream Port (hub)

This test checks the hub repeater capability to transmit properly when repeating downstream traffic.

a) Using HSET (or XHSET), place the port under test in test mode TEST_FORCE_ENABLE.
b) Generate Test Packets from upstream source (host) using test mode TEST_PACKET.
c) Capture waveform on the high speed oscilloscope.
d) Analyze waveform using USBET with settings for downstream signal.

4.1.3 Downstream Port (host)

This test checks a host's capability to transmit properly.

a) *Place port in test mode TEST_PACKET.*
b) *Capture waveform on the high speed oscilloscope.*
c) *Analyze waveform using USBET with settings for downstream signal.*

4.2 Receiver Characteristics

These tests check the receive characteristics of upstream ports.

4.2.1 Upstream Port Receiver Sensitivity

Testing the upstream port and the criteria that will be tested are as follows:

a) Place the device under test in test mode SE0_NAK.
b) Isolate the device under test from the USB data bus.

c) *Connect data generator to the DUT data lines.*
d) *Have the data generator send IN packets to the DUT.*
e) *Vary the data amplitude and verify that all packets are NAK'd while signaling level is above the sensitivity level.*
f) *Vary the data amplitude and verify that no packets are NAK'd when the signaling level is below the squelch level.*
g) *Generate IN packets of compliance amplitude with a 12-bit SYNC field.*
h) *Verify that the device responds.*

4.3 J and K Voltage Levels

These tests measure the voltage levels on D+ and D- when they are not driven by the high speed drivers. Test should be conducted with pre-emphasis disabled on the device. These tests are performed on all ports.

a) *Place port in test mode TEST_J and apply ideal terminations.*
b) *Measure D+ and verify that it is within spec.*
c) *Reset device under test.*
d) *Place port in test mode TEST_K and apply ideal terminations.*
e) *Measure D- and verify that it is within spec.*
f) *Place port under test in test mode SE0_NAK and apply ideal terminations.*
g) *Measure D+ and D- to be 0V +-20mV.*

4.4 Speed Detection

These tests examine the chirp behavior for both upstream and downstream ports. For a hub, chirp must be tested both on the upstream (connecting the hub to a known good host) and all downstream ports (connecting a known good device). All downstream tests are done on hubs and host controllers.

4.4.1 Chirp Timing/Voltage Characteristics

This test examines the basic timings and voltages of both upstream and downstream parts during the speed detection protocol.

a) *Connect device under test to host through USB test fixture.*
b) *Capture signal using single ended probes on both data lines.*
c) *Analyze data for the following.*

Upstream Port (device reset from Full Speed)

1) *Full Speed idle voltage.*
2) *Time from beginning of Reset to Chirp K (2.5us to 2ms).*
3) *Chirp K amplitude (~800mV)*
4) *Chirp K Duration (1ms to not more than 7ms after start of Reset).*
5) *Number of KJ pairs before high-speed termination applied (at least 3 pairs).*
6) *Delay after KJKJKJ before device applies terminations.*

Upstream Port (device reset from High Speed)

1) *Time from beginning of Reset (last SOF) to Chirp K (3ms to 6ms).*
2) *Chirp K amplitude (~800mV).*
3) *Chirp K duration (1ms to not more than 7ms after start of Reset).*
4) *Number of KJ pairs before high-speed termination applied (at least 3 pairs).*

5) *Delay after KJKJKJ before device applies terminations (<500us).*

Upstream Port (device Reset from Suspend after being in High Speed)

1) *Full Speed idle voltage.*
2) *Time from beginning of reset to Chirp K (2.5us to 6ms).*
3) *Chirp K amplitude (~800mV).*
4) *Chirp K duration (1ms to not more than 7ms after start of Reset).*
5) *Number of KJ pairs before high-speed termination applied (at least 3 pairs).*
6) *Delay after KJKJKJ before device applies terminations(<500us).*

Downstream Port

1) *Hub Chirp response time (<=100us).*
2) *Hub Chirp J duration (40us to 60us).*
3) *Hub Chirp K duration (40us to 60us).*
4) *Hub Chirp J and K amplitudes (~400mV).*
5) *Time from end of Chirps to first SOF (100us to 500us).*

4.5 Packet Parameters

There several important packet characteristics for upstream and downstream signaling that are examined. They include the following.

4.5.1 Response Time

This test measures the amount of time it takes hosts and devices to respond. It also verifies device generated SYNCs and EOPs.

a) *Using HSET or XHSET execute test mode SINGLE_STEP_SET_FEATURE.*
b) *Capture Packets on the oscilloscope.*
c) *On the 3rd packet, measure 32 bit SYNC field and 8 bit EOP field.*
d) *Measure device response between Setup (2nd packet) and Data (3rd packet) (88 to 192 bits) (Response to Setup).*
e) *For hosts measure time between 1st and 2nd packets (back to back packets from host).*
f) *On HSET (or XHSET) execute Step.*
g) *Measure the time between packets (8 to 192 bits). For hosts with built-in hub the maximum is 264 bits + 8ns. Response to In.*

4.5.2 Host SOF Sync and EOP Bits

This test verifies that a host generates the proper SYNC and EOP fields for SOF packets.

a) Use oscilloscope to capture SOF from host.
b) Count SYNC field bits (32).
c) Count EOP field bits (at least 40).

4.6 Suspend and Resume

This test verifies that a device can be suspended and resumed while operating in high-speed and also that the device can be reset from the suspended state.

a) Attach and enumerate the device.
b) Using HSET (or XHSET) suspend the port where the device is attached.
c) Verify that the device reverts to full speed terminations within 3000us to 3125us.
d) Using HSET (or XHSET) resume the port where the device is attached.
e) Verify that the device has high speed terminations on for the first SOF.
f) Using HSET (or XHSET) suspend the port where the device is attached.
g) Using HSET (or XHSET) drive Reset from the port where the device is attached.

4.7 High Speed Repeater Tests

These tests measures hub repeater characteristics by attaching test fixtures on both the upstream and downstream ports of the hub under test. Data is captured at both ports and sync truncation, EOP dribble, and latency through the hub are measured.

4.7.1 Downstream Repeater Tests

This test measures sync truncation, EOP dribble and latency in the downstream direction.

a) Connect upstream port of the hub through the test fixture to a host and a high speed device through the test fixture to the downstream port under test.
b) Using HSET (or XHSET) enumerate the device.
c) Capture an SOF on both upstream and downstream ports.
d) Verify SYNC truncation (not more than 4 bits), EOP dribble (not more than 4 bits), and latency through the hub (not more than 36 bit times plus 4ns).

4.7.2 Upstream Repeater Tests

a) Connect upstream port of the hub through the test fixture to a host and a high speed device through the test fixture to the downstream port under test.
b) Using HSET (or XHSET) execute test mode SINGLE_STEP_SET_FEATURE.
c) Capture signal on both upstream and downstream ports.
d) Verify SYNC truncation (not more than 4 bits), EOP dribble (not more than 4 bits), and latency through the hub (not more than 36 bit times plus 4ns).