NOTICE: Any Company or Companies submitting a USB Power Delivery ECN proposal must be one of the following: a Promoter or Contributor of the USB 3.0 and 2.0 Specifications who have completed the USB Power Delivery addendum. If a group of Companies is submitting an ECR proposal, each company must be either a Promoter or Contributor of the USB 3.0 and 2.0 Specifications who have completed the USB Power Delivery addendum.

SPECIFICATION REVISIONS AND ADDENDA: At any point in time, there shall only be one current version of the USB PD CTS, termed the production version. At the same time, there may also be proposed revisions to the specification's design which are not yet approved and shall be held confidential as deemed necessary by the USB 3.0 and USB 2.0 Promoters and within the Group of Working Committee(s).

PROCEDURES FOR SUBMITTING PROPOSALS: Both members of the USB Implementers Forum as a whole and members of the USB 3.0 and USB 2.0 Promoters may submit requests to revise the USB PD CTS Specification. Such a request may be rejected or may result in a USB PD Engineering Change Notice (ECN), which is the official way USB specifications may be changed.

FORMAT OF PROPOSAL: The originator of a request to alter the USB PD CTS Specification may do so by posting this to the USB Power Delivery Compliance working group for review. Once the proposal has been reviewed by the working group it will be passed to the USB 3.0 and 2.0 Promoters for approval to publish.

RESUBMISSION AND APPEAL: The originator of a request that was not approved can redraft the original request. Rewritten proposal will be treated as a new proposal and will be evaluated using the procedures described above. The originator of a request that was not approved can also submit an appeal to the USB 3.0 and 2.0 Promoters. The appeal must be made in writing and addressed to the Secretary of the USB Implementers Forum.

ABOUT THE ENGINEERING CHANGE REQUEST FORM:

The Purpose of this Engineering Change Request Form is to expedite the review process of the proposal by providing explanations, background information, and examples of the proposed changes at a high level. This form serves as an executive summary to the actual proposal.

STEPS ON HOW TO SUBMIT A USB PD ENGINEERING CHANGE REQUEST:

1) Please fill out the Engineering Change Request Form on the following pages completely:
   a) Detail the names and contact details for each of the ECR contributors
   b) Update the ECR Title
   c) Give a minimum of 2-3 sentences for each description on the form outlining the background to the ECR
2) For each section/table/figure to be updated:
   a) Detail the section number, starting page and figure/table number to be updated as appropriate.
   b) Detail existing text under "From Text"
   c) Detail changed text under "To Text"
3) Save the file as "USB PD CTS 1.0 R 1" followed by the ECR Title as per step 1)b)
4) Post the ECR in the USB PD CTS Documents section under "ECR | New ECRs".
   a) This ECR will then be reviewed by the Power Delivery Compliance Working Group.
   b) Revisions to the ECR originating from the review should be submitted as document revision of the original ECR using "Add new document".

Name: Pat Crowe Email:

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Title: Restore Hard Reset Test from Previous Test Spec
Applied to: USB PD CTS Specification r1.p4 v6

Brief description of the functional changes proposed:
The original 'Protocol Engine' test spec fully tested a Hard Reset sequence, but this appears to have been omitted from the CTS version. This is a proposal to re-instate it. The test is proposed to start Hard Reset from both 5V and the highest Fixed voltage available as it has been found that either could be a worst case in practice.

Benefits as a result of the proposed changes:

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

An analysis of the hardware implications:

An analysis of the software implications:

An analysis of the compliance testing implications:

An analysis of the Vendor Info File (VIF) implications:

Add:TEST.PD.PS.SRC.5 Source Hard Reset Test

Description: As a Sink only, the Tester verifies that the Source UUT responds correctly to a Hard Reset from the Higest Voltage available.

Test Specific Tester Behavior: N/A

Test Conditions:

	Consumer Only	Provider Only, P/C, C/P, DRP
Rev2Src		✓
Rev3ChkdSrc		✓

Test Requirements:

Test Procedures:

1. There are 2 possible bring-up procedures:
    a. The UUT has VIF field PD_Port_Type set to Consumer/Provider, the Tester runs bring-up procedure with the UUT as a Source COMMON.PROC.BU.7.
    b. The UUT has VIF field PD_Port_Type set to anything else, the Tester runs bring-up procedure with the UUT as a Source COMMON.PROC.BU.1.
2. The Tester sends a Hard Reset signal.
3. The Tester makes the following checks:
    a. VBUS stays within present valid voltage range for tPSHardReset min after last bit of Hard Reset signal. [TEST.PD.PS.SRC.5#1]
    b. VBUS reaches vSafe0V max within tSafe0v max of tPSHardReset max. [TEST.PD.PS.SRC.5#2]
    c. VBUS rises above vSafe0V max after a delay of between tSrcRecover min and tSrcRecover max after reaching vSafe0V. [TEST.PD.PS.SRC.5#3]
    d. VBUS reaches vSafe5V within tSrcTurnOn max after rising above vSafe0v max [TEST.PD.PS.SRC.5#4]
    e. The UUT starts sending a Source Capabilities message within tFirstSourceCap max of VBUS reaching vSafe5v min. [TEST.PD.PS.SRC.5#5]
4. The Tester disconnects from the UUT and waits for at least 1s.
5. If no Fixed PDO greater than 5V is available from the UUT, the test ends here.
6. There are 2 possible bring-up procedures:
    a. The UUT has VIF field PD_Port_Type set to Consumer/Provider, the Tester runs bring-up procedure with the UUT as a Source COMMON.PROC.BU.7.
    b. The UUT has VIF field PD_Port_Type set to anything else, the Tester runs bring-up procedure with the UUT as a Source COMMON.PROC.BU.1.
7. The Tester makes a Request for the highest Fixed PDO available and checks that the contract is made. The Tester does not draw any current. [TEST.PD.PS.SRC.5#6]
8. The Tester sends a Hard Reset signal.

9. The Tester makes the following checks:
    a. VBUS stays within present valid voltage range for tPSHardReset min after last bit of Hard Reset signal. [TEST.PD.PS.SRC.5#7]
    b. VBUS reaches vSafe5V max within tSafe5v max of tPSHardReset max. [TEST.PD.PS.SRC.5#8]
    c. VBUS reaches vSafe0V max within tSafe0v max of tPSHardReset max. [TEST.PD.PS.SRC.5#9]
    d. VBUS rises above vSafe0V max after a delay of between tSrcRecover min and tSrcRecover max after reaching vSafe0V. [TEST.PD.PS.SRC.5#10]
    e. VBUS reaches vSafe5V within tSrcTurnOn max after rising above vSafe0v max [TEST.PD.PS.SRC.5#11]
    f. The UUT starts sending a Source Capabilities message within tFirstSourceCap max of VBUS reaching vSafe5v min. [TEST.PD.PS.SRC.5#12]
10. The Tester disconnects from the UUT.