Embedded High-speed Host Electrical Test Procedure

Revision 1.01

May 5, 2006

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1. Preamble

1.1 Revision History

Revision	*Issue Date*	*Comments*
0.5	2/3/2004	Initial Draft
0.7	9/22/2004	Write specifically for high-speed OPT use
0.8	2/1/2005	Update based on OTG F2F Review 1. Split SINGLE_STEP_GET_DEVICE_DESCRIPTOR into two parts, rename, and added new VID = 0x0108 2. Break Test J/K/SEO_NAK from one table into 3 separate tables
0.85	3/2/2005	Minor text corrections. Split Host Controller Packet Parameters into two tables.
0.86	3/9/2005	Correct PID assignment discrepancy for TestJ and TestK. Value assigned in the table rules.
.90	3/25/2005	Re-named and re-worded GET_DEVICE_DESCRIPTOR_SETUP and GET_DEVICE_DESCRIPTOR_EXECUTE. Reformatted document, changed from proposal to test procedure.
1.0	11/1/2005	1.0 out for review
1.01	5/5/2006	1.01 Corrected EL_XX parameters included in tests

1.2 Reference Documents

1. Universal-Serial-Bus revision 2.0 Specification – available at http://www.usb.org/developers/docs/
2. Host High-Speed Electrical Test Procedure revision 1.2 – available at http://www.usb.org/developers/docs/

1.3 Acronyms

FS	Full-Speed
HHSETP	Host High-Speed Electrical Test Procedure document. Available at www.usb.org/developers/docs
HS-OPT	High-Speed On-The-Go Protocol Tester
HS	High-Speed
OTG	USB On-The-Go
USB	Universal Serial Bus

2. Background

In order to use the USB High-speed logo, all high-speed hosts must pass compliance tests defined by the USB-IF. The electrical compliance tests require host controllers to support test modes as defined in Section 7.1.20 of the USB 2.0 specification.

To activate a test mode, the USB 2.0 specification defines the `SetFeature()` command as the desired interface. This requires software with a user interface to run on the host system. The USB-IF offers a High-speed Electrical Test tool (HSET), which is Windows based, to activate the various test modes and operations. Alternately, a vendor may provide their own equivalent HSET utility to use on their host system.

With the introduction of USB On-The-Go, high-speed host controllers are expected to be embedded into small devices with very limited resources (printers, disk drives, cell-phones, etc.) Some systems may not provide a user interface sophisticated enough to support a program that a test engineer can manipulate easily. Other systems may not have sufficient resources available to execute such a program. But most importantly, these devices are not expected to be running WindowsXP or Windows2000 and have an EHCI controller – requirements for the USB-IF HSET utility.

Relying on silicon vendors and integrators to provide equivalent HSET capabilities has the potential of introducing many problems, not only for the vendor, but for the USB-IF as well. For example, the method chosen by the vendor to initiate test modes may be necessarily very intrusive on the device rendering the quality of the certification results on the consumer device questionable. Inconsistencies in the initiation of test modes make it very difficult to budget test time at workshops and test facilities due to learning curves.

This document describes the preferred method for vendors to initiate test modes on embedded hosts. Vendors have the option of not supporting these methods to enter the test modes, but must provide an interface that allows all the test modes to be executed to be eligible for certification.

3. Test Mode Support

One method of initiating the host test modes is to run an application on the host, which is what the Windows HSET utility or equivalent vendor-supplied software do. An alternative is to have the embedded host support a test fixture that initiates the test modes. Upon enumeration by the host, the test fixture presents a VID/PID pair that defines a test mode or operation to execute.

The VID is specified in Section 6.6.6 of the OTG Supplement as the Test Device. Its value is 0x1A0A. Upon enumerating a device with VID of 0x1A0A, the embedded host must perform a set of operations based on the PID presented. The test mode or operation must occur on the port where the test fixture is attached.

The Hi-Speed On-the-Go Protocol Tester (HS-OPT) is a programmable tool developed to test devices for compliance with the Hi-Speed On-The-Go protocol. It is used as the Test Fixture to supply the VID/PID pairs that initiate test modes on embedded hosts.

3.1 Scope of this Document

This document is not intended to define the passing or failing criteria for each test, nor does it describe in depth how to set up the scope and make measurements. These are already defined in the USB 2.0 Specification and the Host High-Speed Electrical Test Procedure.

This document is intended to define a method for initiating test modes on embedded hosts, as the Windows HSET utility is unsuitable in the embedded world. Readers are referred to the documents mentioned for how to setup the oscilloscope and make timing measurements.

3.2 Test Setup

The test setup is illustrated in Figure 1 below. In a typical test, the HS-OPT will connect to the embedded host and present a specific VID/PID combination. Upon detecting the VID/PID combiniation the embedded host enters a test mode. The termination switch on the HS Test Jig is then flipped and the oscilloscope is used to make measurements on the embedded host.

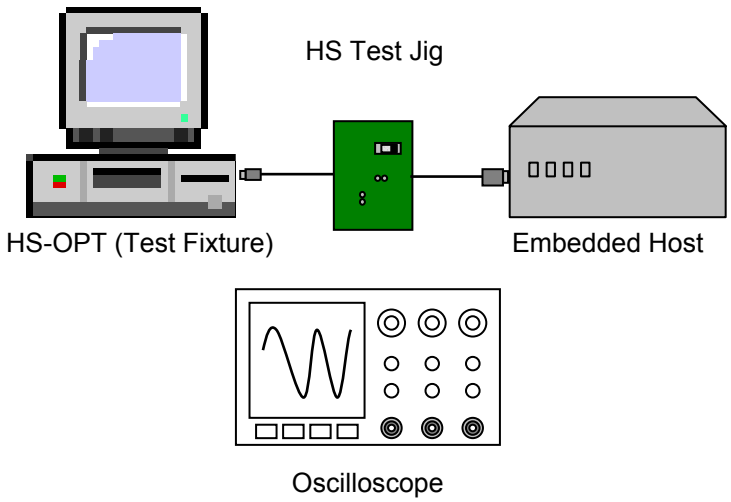

Figure 1. Test Configuration

3.3 Test Modes PID Definitions

The PIDs presented by the test fixture correspond to the following test modes. The VID is 0x1A0A.

PID	Test Mode
0x0101	TEST_SEO_NAK
0x0102	TEST_J
0x0103	TEST_K
0x0104	TEST_PACKET
0x105	Reserved.
0x0106	HS_HOST_PORT_SUSPEND_RESUME
0x0107	SINGLE_STEP_GET_DEV_DESC
0x0108	SINGLE_STEP_SET_FEATURE

3.4 Test Modes

The Test Modes described below are related to Section 7.1.20 of the USB 2.0 Specification and associated errata.

TEST_SE0

Upon enumerating VID 0x1A0A/PID 0x0101, the host's downstream port must enter a high-speed receive mode as described in Section 7.1.20 of the USB 2.0 Specification and drives an SE0 until the controller is reset.

TEST_J

Upon enumerating VID 0x1A0A/PID 0x0102, the host's downstream port must enter a high-speed J state as described in Section 7.1.20 of the USB 2.0 Specification until the host controller is reset.

TEST_K

Upon enumerating VID 0x1A0A/PID 0x0103, the host's downstream port must enter a high-speed K state as described in Section 7.1.20 of the USB 2.0 Specification until the host controller is reset.

TEST_PACKET

Upon enumerating VID 0x1A0A/PID 0x0104, the host must begin sending test packets as described in Section 7.1.20 of the USB 2.0 Specification until the host controller is reset.

HS_HOST_PORT_SUSPEND_RESUME

Upon enumerating VID:0x1A0A/PID 0x0106, the host must continue sending SOFs for 15 seconds, then suspend the downstream port under test per Section 7.1.7.6.1 of the USB 2.0 specification. After 15 seconds has elapsed, the host must issue a ResumeK state on the bus, then continue sending SOFs.

SINGLE_STEP_GET_DEVICE_DESCRIPTOR

When the host discovers a device with VID:0x1A0A/PID 0x0107, the following steps are executed by the host and the device.

1. The host enumerates the test device, reads VID:0x1A0A/PID 0x0107, then completes its enumeration procedure.
2. The host issues SOFs for 15 seconds allowing the test engineer to raise the scope trigger just above the SOF voltage level.
3. The host sends GetDescriptor(Device)
4. The device ACKs the request, triggering the scope. (Note: SOFs may follow the IN transaction).

SINGLE_STEP_SET_FEATURE

When the host discovers a device with VID:0x1A0A/PID 0x0108, the following steps are executed by the host and the device.

1. The host enumerates the test device and reads VID:0x1A0A/PID 0x0108, then completes its enumeration procedure
2. After enumerating the device, the host sends another GetDescriptor()
3. The device ACKs the request
4. The host issues SOFs for 15 seconds allowing the test engineer to raise the scope trigger just above the SOF voltage level
5. The host sends an IN packet
6. The device sends data in response to the IN packet, triggering the scope
7. The host sends an ACK in response to the data. (Note: SOFs may follow the IN transaction).

4. Test Procedures

4.1 High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7)

This test corresponds to "4.4 High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7)" in the HHSETP document. Please refer to Section 4.4 of the HHSETP for instructions on scope setup and passing and failing criteria.

#	Test Fixture	Host
1.	Attach the 5V power supply to J8 of the Host High-speed Signal Quality test fixture and verify the green Power LED (D1) is illuminated. Set the Test switch (S1) of the test fixture to TEST and verify the yellow TEST LED is illuminated.	
2.	Attach the differential probe to J7 of the test fixture. Ensure + on probe lines up with D+ on fixture.	
3.	Connect the Test port of the Host High-speed Signal Quality test fixture into the port under test of the Host controller.	
4.	Connect the Init port of the Host High-speed Signal Quality test fixture into the OPT	
5.	Execute "*EHSET. 1 - TestPacket.xml*" on the HS OPT. The HS OPT connects and presents the TEST_PACKET PID to the host when enumerated.	
6.		The host enumerates the HS OPT and responds to the TEST_PACKET PID by continuously sending test packets
7.	Capture EOP data (refer to *Host High-Speed Electrical Test Procedure* section 4.4)	
8.	Verify the Signal Eye, EOP Width, and Signaling Rate all pass using Matlab scripts.	
9.	Repeat on all remaining downstream ports	

4.2 Host Controller Packet Parameters (EL_21, EL_22, EL_23, EL_25, EL_55)

This test corresponds to "4.5 Host Controller Packet Parameters (EL_21, EL_23, EL_25, EL_55)" in the HHSETP document. It has been broken up into two sub-tests for clarity.

Please refer to Section 4.5 of the HHSETP for instructions on scope setup and instructions on how to measure the EL_XX parameters.

4.2.1 SINGLE_STEP_DEV_DESC (EL_21, EL_25, EL_23)

#	Test Fixture	Host
1.	Attach the differential probe to J7 on the test fixture. Ensure + on probe lines up with D+ on fixture.	
2.	Connect test fixture to root port under test. Ensure that there is a 5 meter cable between the test fixture and the port under test.	
3.	Attach the HS OPT	
4.	Execute "*EHSET.2 - SINGLE_STEP_DEV_DESC*" on the HS OPT	
5.		The host enumerates the HS OPT and begins to issue SOFs to the HS OPT for 15 seconds
6.	Verify SOFs are being transmitted and raise the scope's trigger until SOFs are no long detected	
7.		After 15 seconds of SOFs, the host initiates the setup phase of the GetDescriptor() command. The host sends SETUP and DATA (first and second) packets back to back
8.	The HS-OPT sends an ACK (third) packet in response to the SETUP and DATA from the host. The scope triggers on the ACK from the HS-OPT	
9.	EL_21: Verify sync field in the SETUP and DATA (first and second) packets is 32 bits at 2.08 ns/bit	
10.	EL_25: Verify EOP of the DATA (second) packet is 8 bits at 2.08 ns/bit	
11.	EL_23: Measure interpacket gap between the SETUP and DATA (first and second) packets from the host is between 88 – 192 bits at 2.08 ns/bit.	

4.2.2 SINGLE_STEP_SET_FEATURE (EL_22, EL_55)

#	Test Fixture	Host
1.	Attach the differential probe to J7 on the test fixture. Ensure + on probe lines up with D+ on fixture.	
2.	Connect test fixture to root port under test. Ensure that there is a 5 meter cable between the test fixture and the port under test.	
3.	Attach the HS OPT	
4.	Execute "*EHSET.3 - SINGLE_STEP_SET_FEATURE*" on the HS OPT	
5.		The host enumerates the HS-OPT
6.		After completing the enumeration, the host sends a GetDescriptor() to the HS-OPT
7.	The HS-OPT sends an ACK in response to the GetDescriptor().	
8.		The host sends SOFs for 15 seconds (it does NOT send the IN packet immediately.)
9.	Verify SOFs are being transmitted and raise the scope's trigger until SOFs are no long detected	
10.		The host issues an IN (first) packet
11.	The HS-OPT sends DATA (second) packet. This triggers the scope.	
12.		The host sends an ACK (third) packet.
13.	EL_22: Measure response time between the DATA and ACK (second and third) packets. This must be between 8-192 bits at 2.08 ns / bit.	
14.	Lower the scope's trigger so that it triggers on an SOF. Stop the scope.	
15.	EL_55: Measure the EOP width of the SOF packet. This must be 40 bits at 2.08 ns / bit	
16.	Repeat on all remaining downstream ports	

4.3 Host CHIRP Timing (EL_33, EL_34, EL_35)

This test corresponds to "4.7 Host CHIRP Timing (EL_33, EL_34, EL_35)" in the HHSETP document.

NOTE: ON THIS TEST ONLY, the HS-OPT can verify all the required parameters. If the HS-OPT reports "Success!" at the end of the test the Host passed this test. No measurements with the oscilloscope are required for this test.

#	Test Fixture	Host
1.	Connect Test Fixture to root port of host	
2.	Connect HS OPT to the test fixture.	
3.	Execute "*EHSET.4 – CHIRP Timing*" on the HS OPT	
4.	The HS OPT connects by asserting D+	
5.		The host responds by asserting SE0
6.	HS OPT drives chirpK 1ms after detecting SE0	
7.	HS OPT stops driving chirp K after 4ms	
8.		The host responds by issuing KJ pairs
9.	EL_33: HS OPT measures when host begins first HS chirpK	
10.	EL_34: HS OPT measures chirpK and chirpJ widths	
11.	HS OPT applies HS terminations 250 microseconds after seeing 3 chirp KJ pairs from the host	
12.		The host begins sending SOFs
13.	EL_35: HS OPT measures the time between last chirpJ or K and first SOF.	
14.	Repeat on all remaining downstream ports	

4.4 Host Suspend/Resume Timing (EL_39, EL_41)

This test corresponds to "4.8 Suspend/Resume Timing (EL_39, EL_41)" in the HHSETP document. The same test is run twice to measure two different parameters in the SUSPEND/RESUME sequence. The first run measures the SOF-to-Suspend time. The second run measures the ResumeK-to-SOF time. The HOST response to the PID is the same in both tests, the operator just makes different measurements.

Please refer to Section 4.8 of the HHSETP for instructions on scope setup and instructions on how to measure the EL_XX parameters.

NOTE: There is a typographical error in step 9 of this test in the HHSETP document. It says, "Measure the time from the falling edge of D+ to the first SOF...". It should read, "Measure the time from the falling edge of ***D-*** to the first SOF...".

4.4.1 SUSPEND (EL_39)

Note that the timing measurement made in this test does not measure a timing parameter of the Host. The time from the last SOF to the J-state on the bus is controlled by the HS-OPT. This test simply verifies that the Host has de-asserted its terminations which is necessary for the bus to enter a SUSPEND state.

#	Test Fixture	Host
1.	Connect Test Fixture to root port of host	
2.	Connect HS OPT to test fixture	
3.	Execute "*EHSET.5 – SUSPEND-RESUME*" on the HS OPT	
4.		Host identifies SUSPEND/RESUME VID/PID, waits 15 seconds for scope setup and suspends the root port
5.	EL_39: Measure time from last SOF to full-speed J-state (transition to full-speed 3.0ms – 3.125ms)	
6.		After 15 seconds, the host drives a ResumeK state on the root port, then starts sending SOFs.
7.	Repeat on all remaining downstream ports	

4.4.2 RESUME (EL_41)

#	Test Fixture	Host
8.	Connect Test Fixture to root port of host	
9.	Connect HS OPT to test fixture	
10.	Execute "*EHSET.5 – SUSPEND-RESUME*" on the HS OPT	
11.		Host identifies SUSPEND/RESUME VID/PID, waits 15 seconds for scope setup and suspends the root port
12.		After 15 seconds of SUSPEND, the host drives a ResumeK state on the root port, then starts sending SOFs.
13.	EL_41: Measure time form falling edge of D- to the first SOF (< 3ms)	
14.	Repeat on all remaining downstream ports	

4.5 Host Test_J (EL_8, EL_9)

This test corresponds to the TEST_J test of "4.9 Test J/K, SE0_NAK (EL_39, EL_41)" in the HHSETP document.

Please refer to Section 4.9 of the HHSETP for instructions on scope setup and instructions on how to measure the EL_XX parameters.

#	Test Fixture	Host
1.	Connect test fixture to root port of host	
2.	Connect the HS OPT to the test fixture	
3.	Execute "*EHSET.6 -TEST_J*" on the HS OPT	
4.		The host identifies the TEST_J VID/PID and enters HS J state
5.	EL_8: Measure D+ and D- voltage	
6.	Repeat on all remaining downstream ports	

4.6 Host Test_K (EL_8, EL_9)

This test corresponds to the TEST_K test of "4.9 Test J/K, SE0_NAK (EL_39, EL_41)" in the HHSETP document.

Please refer to Section 4.9 of the HHSETP for instructions on scope setup and instructions on how to measure the EL_XX parameters.

#	Test Fixture	Host
1.	Connect test fixture to root port of host	
2.	Connect the HS OPT to the test fixture	
3.	Execute "*EHSET.7 TEST_K*" on the HS OPT	
4.		The host identifies the TEST_K VID/PID and enters a HS K state
5.	EL_8: Measure D+ and D- voltage	
6.	Repeat on all remaining downstream ports	

4.7 Host Test_SE0 (EL_8, EL_9)

This test corresponds to the TEST_SE0_NAK test of “4.9 Test J/K, SE0_NAK (EL_39, EL_41)” in the HHSETP document.

Please refer to Section 4.9 of the HHSETP for instructions on scope setup and instructions on how to measure the EL_XX parameters.

#	Test Fixture	Host
1.	Connect test fixture to root port of host	
2.	Connect the HS OPT to the test fixture	
3.	Execute SE0_NAK on the HS OPT	
4.		The host identifies the SE0_NAK VID/PID and drives an SE0
5.	EL_9: Measure D+ and D- voltage	
6.	Repeat on all remaining downstream ports	