USB4™ Cable Electricals and System Design

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Agenda

• Cable Electricals
  • Electrical Spec
    • Cables
    • Mated Connectors
  • Design Challenges
  • Compliance Test

• System Design Guidelines
  • Electrical Design Considerations
  • Physical Design Considerations
    • Trace geometries
    • Routing practices, vias, and component placements
    • Layout design
  • Component selection
Cable Electricals

Yun Ling,
Sr. Principal Engineer, Intel
USB Type-C® Cables and Connectors

- Focus on C-to-C cable high speed electricals
- No change to mechanical spec
USB4™ Gen2 Cable Spec

• USB4 Gen2 cable electrical spec is identical to USB3.2!
  • It uses the same integrated S-parameters, avoiding the S-parameter mask as much as possible.

• Key spec items include:
  • Insertion Loss Fit at Nyquist
  • Integrated Multi-Reflection
  • Integrated Return Loss
  • Integrated Crosstalk

S-parameter mask-based spec creates too many false failure cases!
Insertion Loss Fit and Multi-Reflection

• Insertion loss, $IL(f)$, represents the remaining signal after it travels thru the cable.
• $IL(f)$ may be decomposed into Insertion loss fit, $IL_{fit}(f)$ and multi-reflection, $MR(f)$.
  • $IL_{fit}$: uses a smooth function to fit the IL, representing the signal.
  • $MR = IL - IL_{fit}$, representing the multi-reflection noise.
• $IL$ fit at Nyquist frequency = $IL_{fit}$ (Nyquist frequency):

USB4 Gen2 or USB 3.2 Gen2:

$$IL_{fit} = a + b \times \sqrt{f} + c \times \sqrt{f^2} + d \times \sqrt{f^3}$$

USB4 Gen3:

$$IL_{fit} = a + b \times \sqrt{f} + c \times \sqrt{f^2} + d \times \sqrt{f^3} + e \times \sqrt{f^4}$$

Added a $f^2$ term to make the fitting more robust.
System loss budget

- Host/device loss includes everything in the signal path from die to connector tongue.
- USB4 Gen2 supports a 12 dB (2m) cable while USB3.2 Gen2 support only a 6 dB (1m) cable due to the difference in system loss budget.
- Host/device loss budgets are informative only.

<table>
<thead>
<tr>
<th></th>
<th>Host</th>
<th>Cable</th>
<th>Device</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB3.2 Gen2 (10 Gbps)</td>
<td>8.5 dB</td>
<td>6 dB</td>
<td>8.5 dB</td>
<td>23 dB</td>
</tr>
<tr>
<td>USB4 Gen2 (10 Gbps)</td>
<td>5.5 dB</td>
<td>12 dB</td>
<td>5.5 dB</td>
<td>23 dB</td>
</tr>
<tr>
<td>USB4 Gen3 (20 Gbps)</td>
<td>7.5 dB</td>
<td>7.5 dB</td>
<td>7.5 dB</td>
<td>23 dB</td>
</tr>
</tbody>
</table>
Insertion Loss Fit Spec

- **USB 3.2 Gen2**
  - $\geq -4$ dB at 2.5 GHz
  - $\geq -6$ dB at 5 GHz
  - $\geq -11$ dB at 10 GHz

- **USB4 Gen2 (2m)**
  - $\geq -7.0$ dB at 2.5 GHz
  - $> -12$ dB at 5 GHz

- **USB4 Gen3**
  - $\geq -1$ dB at 100 MHz
  - $\geq -4.2$ dB at 2.5 GHz
  - $\geq -6$ dB at 5 GHz
  - $\geq -7.5$ dB at 10 GHz
  - $\geq -9.3$ dB at 12.5 GHz
  - $\geq -11$ dB at 15 GHz

- Cable length mentioned in the spec is for reference only. Performance spec dictates cable length.

- Consideration to HVM variation is a must!
  - Spec is meant for the worst-case, not the mean value. For example, to meet the $\geq -7.5$ dB $\text{IL}_{\text{fit}}\text{ at } 10\text{GHz}$ spec, the mean has to be significantly $> -7.5$ dB to account for HVM variation
Integrated Multi-Reflection Spec

$IMR = dB \left( \sqrt{ \frac{\int_0^{f_{\text{max}}} |MR(f)|^2 |V_{\text{in}}(f)|^2 df}{\int_0^{f_{\text{max}}} |V_{\text{in}}(f)|^2 df} } \right)$

Input signal pulse frequency spectrum

Multi-reflection

$|V_{\text{in}}(f)| = \left| \frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b} \right|$

Normalization factor

$f_{\text{max}} = 12.5 \text{ for } USB4 \text{ Gen 2 and } 20 \text{ GHz for } USB4 \text{ Gen3}$

$T_b = \text{Unit Interval, 100 ps for } USB4 \text{ Gen2 and 50 ps for } USB4 \text{ Gen3}$

- IMR is normative for USB4 Gen2
- IMR is informative for USB4 Gen3
  - A larger IMR is allowed if cable loss is smaller
Integrated Return Loss

$$IRL = dB \left( \sqrt{\frac{\int_{0}^{f_{\text{max}}} |Vin(f)|^2 |SDD21(f)|^2 (|SDD11(f)|^2 + |SDD22(f)|^2) df}{\int_{0}^{f_{\text{max}}} |Vin(f)|^2 df}} \right)$$

Integrated Return Loss measures the undesired interaction/reflection between the cable and host/device.

• IRL is a normative requirement.
• More IRL is allowed if cable loss is smaller.
Integrated Crosstalk

\[ \text{IXTi}_{\text{DP or USB}} = \text{dB} \left( \frac{\int_0^{f_{\text{max}}} |V_{\text{in}}(f)|^2 \sum_j |S_{\text{DD}ij}|^2 df}{\int_0^{f_{\text{max}}} |V_{\text{in}}(f)|^2 df} \right) \]

• USB4 Gen3 specifies the combined total crosstalk in USB mode and DP alt-mode.
  • USB mode: 2 NEXT +1 FEXT
  • DP mode: 3 FEXT

• It is a better way to control crosstalk as compared to specify crosstalk between each pairs.
  • Easier to meet the spec for the same effect
Mode Conversion

- Mode conversion is relaxed from -20 dB to -17 dB (to 10 GHz) for USB4 Gen3 due to industry capability reality
COM – Channel Operation Margin

• COM is a figure of merit to measure channel electrical quality defined by IEEE 802.3. It is a Signal-to-Noise Ratio developed in a similar way to Statistical Analysis

• Collaterals needed to calculate COM:
  • Measured cable S-parameters
  • Reference hosts/devices
  • Reference Tx/Rx termination
  • COM configuration file
Reference Host – 1/2

- Topology of the Reference Host/device

Die model is used for collection of Insertion Loss and Return Loss. But it is not in the reference host.

Variables permutations from which two reference hosts are selected
- Impedance of traces
- Attenuation of traces
- Trace length
- Location of the ESD

Two reference hosts/devices are defined: long host/device and short host/device.
Long host/device has about -7.5 dB loss at 10 GHz (with die-loading)
Short host/device has the minimum loss possible
Reference Host – 2/2

- Insertion loss up to receptacle’s tongue include die load

- Return loss at TP2 (w/ die load attached)
COM Config File for USB4™ Gen3

- All equalization settings are based on the USB4 Specification.
  - Tx FFE
  - RX CTLE and DFE
- Tx random jitter and deterministic jitter are derived from the USB4 specification.
- The input voltage swing (A_v, A_fe, and A_ne) is assumed to be the typical range of 0.8 to 1.2 V (differential peak-to-peak)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Setting</th>
<th>Unit</th>
<th>Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_b</td>
<td>20</td>
<td>GBd</td>
<td>USB4 Gen 3 data rate</td>
</tr>
<tr>
<td>C_d</td>
<td>[0 0]</td>
<td>nF</td>
<td>Tx and Rx capacitive loading. It is set to zeros as the die-loading is treated as part of the channel</td>
</tr>
<tr>
<td>R_d</td>
<td>[42.5 42.5]</td>
<td>Ohm</td>
<td>Tx and Rx termination resistance</td>
</tr>
<tr>
<td>ffe_preset</td>
<td>Table 3-4 of USB4 Specification</td>
<td></td>
<td>Tx equalization presets</td>
</tr>
<tr>
<td>g_DC</td>
<td>[-9:1:0]</td>
<td>dB</td>
<td>CTLE DC gain</td>
</tr>
<tr>
<td>f_p1</td>
<td>5</td>
<td>GHz</td>
<td>CTLE pole 1</td>
</tr>
<tr>
<td>f_p2</td>
<td>10</td>
<td>GHz</td>
<td>CTLE pole 2</td>
</tr>
<tr>
<td>f_z</td>
<td>3.55</td>
<td>GHz</td>
<td>CTLE zero</td>
</tr>
<tr>
<td>A_v</td>
<td>0.4</td>
<td>V</td>
<td>Signal swing</td>
</tr>
<tr>
<td>A_fe</td>
<td>0.4</td>
<td>V</td>
<td>FEXT aggressor swing</td>
</tr>
<tr>
<td>A_ne</td>
<td>0.6</td>
<td>V</td>
<td>NEXT aggressor swing</td>
</tr>
<tr>
<td>N_b</td>
<td>1</td>
<td></td>
<td>Number of DFE tap</td>
</tr>
<tr>
<td>b_max(1)</td>
<td>0.7</td>
<td></td>
<td>DFE bound, ratio to cursor</td>
</tr>
<tr>
<td>Sigma_RJ</td>
<td>0.01</td>
<td>UI</td>
<td>Tx random jitter, rms.</td>
</tr>
<tr>
<td>A_DD</td>
<td>0.085</td>
<td>UI</td>
<td>Tx deterministic jitter, mean-to-peak</td>
</tr>
<tr>
<td>DER_0</td>
<td>1e-12</td>
<td></td>
<td>Target raw bit-error-rate</td>
</tr>
<tr>
<td>eta_0</td>
<td>3.3e-8</td>
<td>V^2/GHz</td>
<td>One sided noise spectral density</td>
</tr>
<tr>
<td>SNR_TX</td>
<td>40</td>
<td>dB</td>
<td>Tx signal to noise ratio</td>
</tr>
<tr>
<td>COM Threshold</td>
<td>3</td>
<td>dB</td>
<td>Pass/fail criterion</td>
</tr>
</tbody>
</table>
Spec Validation

- Spec cables: “worst-case” cables that hit the spec limits at various ILfit @10 GHz.
  - The spec cables marginally pass/fail COM

- Measured cables: measured TBT3 cables from different vendors
  - Almost all known TBT3 cables pass the integrated parameter and COM spec.

<table>
<thead>
<tr>
<th>Host#</th>
<th>Device#</th>
<th>Cable#</th>
<th>Victim</th>
<th>ILfitatNq</th>
<th>Signal_mV</th>
<th>ISI_mV</th>
<th>Crosstalk</th>
<th>COM</th>
<th>COM Limit</th>
<th>Pass/Fail</th>
<th>Integrated Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Spec long cable</td>
<td>Tx2</td>
<td>-22.9182</td>
<td>47.53322</td>
<td>20.7</td>
<td>7.86</td>
<td>2.925708</td>
<td>3</td>
<td>Fail</td>
<td>Border Line</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>Spec short cable</td>
<td>Tx2</td>
<td>-11.0043</td>
<td>142.7662</td>
<td>72.44</td>
<td>17.72</td>
<td>2.936699</td>
<td>3</td>
<td>Fail</td>
<td>Border Line</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>Measured Cable26</td>
<td>Rx1</td>
<td>-17.7044</td>
<td>76.09064</td>
<td>28.88</td>
<td>21.9</td>
<td>2.681497</td>
<td>3</td>
<td>Fail</td>
<td>Fail IXT</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Measured Cable27</td>
<td>Tx2</td>
<td>-22.2626</td>
<td>50.48604</td>
<td>21.25</td>
<td>6.17</td>
<td>3.528888</td>
<td>3</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Measured Cable29</td>
<td>Tx2</td>
<td>-22.7136</td>
<td>49.78228</td>
<td>21.08</td>
<td>5.83</td>
<td>3.45617</td>
<td>3</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Measured Cable30</td>
<td>Tx2</td>
<td>-21.4544</td>
<td>54.79757</td>
<td>22.36</td>
<td>7.8</td>
<td>3.683021</td>
<td>3</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Measured Cable31</td>
<td>Rx1</td>
<td>-21.2108</td>
<td>53.77911</td>
<td>23.54</td>
<td>6.63</td>
<td>3.375939</td>
<td>3</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Measured Cable33</td>
<td>Tx2</td>
<td>-22.299</td>
<td>49.82818</td>
<td>22.82</td>
<td>5.46</td>
<td>3.150423</td>
<td>3</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Measured Cable32</td>
<td>Tx2</td>
<td>-19.5524</td>
<td>66.52476</td>
<td>33.3</td>
<td>12.65</td>
<td>2.522059</td>
<td>3</td>
<td>Fail</td>
<td>Fail IRL</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Measured Cable22</td>
<td>Tx1</td>
<td>-19.9512</td>
<td>64.03106</td>
<td>28.25</td>
<td>10.45</td>
<td>3.248895</td>
<td>3</td>
<td>Pass</td>
<td>Marginal on IRL</td>
</tr>
</tbody>
</table>
**Mated Connector Spec**

- USB 3.2 and USB4 Gen 2 have only the informative receptacle/mated connector electrical spec.
- But for USB4 Gen3, this is Normative.
- Need to define the “Golden Plug”.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>IL fit</td>
<td>≥ −0.6 dB @ 2.5 GHz</td>
</tr>
<tr>
<td></td>
<td>≥ −0.8 dB at 5.0 GHz</td>
</tr>
<tr>
<td></td>
<td>≥ −1.0 dB @ 10 GHz</td>
</tr>
<tr>
<td></td>
<td>≥ −1.25 dB @ 12.5 GHz</td>
</tr>
<tr>
<td></td>
<td>≥ −1.5 dB @ 15 GHz</td>
</tr>
<tr>
<td>IMR</td>
<td>≤ −39 dB</td>
</tr>
<tr>
<td>INEXT</td>
<td>≤ −43 dB</td>
</tr>
<tr>
<td>IFEXT</td>
<td>≤ −43 dB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDDXT (Corssstalk between Tx/Rx and D+/D-)</td>
<td>≤ −50 dB</td>
</tr>
<tr>
<td>IRL</td>
<td>≤ −15 dB</td>
</tr>
<tr>
<td>SCD12/SCD21 (Mode Conversion)</td>
<td>≤ −20 dB (100 MHz to 10 GHz)</td>
</tr>
</tbody>
</table>
Cable Shielding Effectiveness

- The same shielding effectiveness requirement for USB 3.2 Type-C-to-Type-C cables is applicable for the USB4 cables.
Design Challenges

• USB4 Gen3 has tighter electrical requirements for cables and connectors.
• Everything along the signal path should be optimized.
  • Loss, reflection, crosstalk
Design for Signal Integrity

- Raw cable – managing loss and skew
  - Loss per inch
  - Skew
  - Impedance
- Connector – minimizing discontinuities
  - Footprints
  - Contact geometries
  - Middle GND plates
- Paddle card – isolating coupling
  - Pin/wire-out
  - Footprints
  - Layer count
- Wire termination
Compliance Test

• The USB4 Gen3 cable compliance spec is still under development.
• The goal is to have a robust cable/connector eco-system without prohibitive cost adders.
• Key challenges:
  • How to ensure the worst-case cable (within HVM limits) passes the spec?
  • How to check if a certified cable will continue to meet the spec?
USB4™ cable Spec Summary

- The main spec items for USB4 Gen3 cables are:
  - Insertion fit (normative)
  - IMR (informative)
  - IRL (normative)
  - IXT_USB/IXT_DP (normative)
  - COM (normative)
  - Mode conversion
  - Shielding effectiveness

- USB-IF will provide necessary supporting collaterals to extract/calculate the spec parameters
  - Tools and models

- The USB4 Cable/Connector Compliance Spec is still under development.
USB4™ System Design Guidelines

Reza Zamani— Intel
USB4™ System Design Guidelines

- Electrical Design Considerations
- Physical Design Considerations
  - Trace geometry
  - Routing practices, vias, and component placement
  - Layout design
- Component selection
Host and Device Interconnects

- This presentation covers three categories of design considerations for the host and device interconnects/channels:
  1. **Electrical**
  2. **Physical/Layout**
  3. **Component selection and specifications**
Pre-Retimer and Post-Retimer Interconnects

- Various topologies of the router assembly is shown
- For this presentation, let’s say we have two categories of interconnects. These have differences and demand potentially different design priorities. This presentation covers both

<table>
<thead>
<tr>
<th>Pre-Retimer Interconnect</th>
<th>Post-Retimer Interconnect</th>
</tr>
</thead>
<tbody>
<tr>
<td>• No explicit electrical/compliance target. Dependent on Tx and Rx PHYs at either ends.</td>
<td>• Explicit electrical/compliance design targets defined per the spec</td>
</tr>
<tr>
<td>• Likely long =&gt; insertion loss becomes a design priority =&gt; PCB stack up selection, trace geometry optimization, etc.</td>
<td>• Likely short =&gt; return loss becomes a design priority</td>
</tr>
<tr>
<td>• Has fewer discrete components: AC-cap</td>
<td>• Has more discrete components: AC-cap, ESD, bleed resistor, etc. =&gt; component selection, placement and routing are important</td>
</tr>
</tbody>
</table>
• **Electrical Design Considerations**

• **Physical Design Considerations**
  • Trace geometry
  • Routing practices, vias, and component placement
  • Layout design

• **Component selection**
Electrical Design Considerations

- **Insertion Loss:** The informative differential Insertion loss of the router assembly from the receptacle's tongue to the USB4 transceiver is limited to:
  - This includes the die load, IC package, PCB routing, discrete components, and receptacle's tongue
  - Note that the USB4 Gen2’s host budget is smaller than USB3.2’s. This is for supporting a 2m cable

<table>
<thead>
<tr>
<th>Router Assembly Support</th>
<th>Informative Insertion Loss Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB4 Gen 3</td>
<td>&lt; 7.5 dB at 10GHz</td>
</tr>
<tr>
<td>USB4 Gen 2</td>
<td>&lt; 5.5 dB at 5GHz</td>
</tr>
<tr>
<td>USB3.2</td>
<td>&lt; 8.5 dB at 5GHz</td>
</tr>
</tbody>
</table>

- **Tx and Rx Compliance Tests:** The router assembly must meet Tx and Rx compliance. Even though performance of the silicon affects most of the compliance metrics, performance of the interconnect will impact the following:
  - Tx and Rx return loss
  - Total Jitter (TJ) is impacted by the way of:
    1. Tx data dependent jitter (DDJ), which is impacted primarily by the insertion loss
    2. Cross talk in the interconnect contributes to Uncorrelated Deterministic Jitter (UDJ)
  - Rx stressed eye test (a.k.a. BER tolerance test)
  - Secondary effect on a few other compliance metrics, e.g. Tx AC Common mode voltage, etc.
Return Loss Spec

- The Return loss spec defined at **TP2 for Tx** and **TP3' for Rx**
  - The necessary VNA measurements are collected with a compliance plug test board (See 3.3.6.1)
  - The measurement shall be referenced to single-ended impedance of 42.5 Ω
- The differential return loss for both **Tx and Rx** shall not exceed

\[
SDD22(f) = \begin{cases} 
-8.5 & 0.05 < f_{GHz} \leq 3 \\
-3.5 + 8.3 \cdot \log_{10}\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 
\end{cases}
\]

- The common mode return loss for both **Tx and Rx** shall not exceed

\[
SCC22(f) = \begin{cases} 
-6 & 0.05 < f_{GHz} \leq 2.5 \\
-3 & 2.5 < f_{GHz} \leq 12 
\end{cases}
\]
USB4™
System Design Guidelines

• Electrical Design Considerations
• **Physical Design Considerations**
  • Trace geometry
  • Routing practices, vias, and component placement
  • Layout design
• Component selection
Trace Geometry and Impedance

• Choose a trace geometry (width and spacing) that yields nominal differential impedance of 80-85 Ohms

  • For short interconnects, the exact value in that range may be of importance. Recommend COM or return loss simulations to find the optimized value
  • For long channels, the exact impedance in the range is not that important. Trace loss/attenuation should become the primary design concern

• Consider the variation of impedance when assessing your design. This is important for short interconnects
  • Example: notice the impact of impedance variation on return loss and on COM

<table>
<thead>
<tr>
<th>Diff. Return Loss at TP2 (dB)</th>
<th>Frequency (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Target Zdiff – 10%</td>
<td>Baseline - 0.4dB</td>
</tr>
<tr>
<td>Target Zdiff</td>
<td>Baseline</td>
</tr>
<tr>
<td>Target Zdiff + 10%</td>
<td>Baseline - 1dB</td>
</tr>
</tbody>
</table>

Target Zdiff – 10%
Target Zdiff
Target Zdiff + 10%
Trace Geometry and Loss/Attenuation

• If your objective is long reach, reduce the attenuation of traces by optimizing the trace geometry

• The PCB vendor’s recommended minimum trace width/spacing likely have not optimized loss
  • **Design Tip:** you can spend more area (i.e. larger trace width and/or spacing) to reduce loss.

• Example: for 8” of microstrip trace, the differential loss can be cut from 16dB @ 10GHz to ~14dB by optimizing the trace width/spacing from 3.5/3 mils to 5/6 mils

• Consider the variation of loss when assessing your design. See the table for an example
  • Note that aside from manufacturing variations, temperature and humidity can impact attenuation of traces

---

<table>
<thead>
<tr>
<th>Loss at 10GHz/Length</th>
<th>2”</th>
<th>4”</th>
<th>6”</th>
<th>8”</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Loss</td>
<td>3.4 dB</td>
<td>6.6</td>
<td>9.1</td>
<td>11.7</td>
</tr>
<tr>
<td>Typical Loss</td>
<td>4 dB</td>
<td>7.6</td>
<td>10.9</td>
<td>13.9</td>
</tr>
<tr>
<td>Maximum Loss</td>
<td>4.8 dB</td>
<td>8.9</td>
<td>12.2</td>
<td>16.4</td>
</tr>
</tbody>
</table>

Simulations data based on variation due to manufacturing and environmental conditions, not measurement.
Trace Geometry and Cross Talk

- Pair-to-pair spacing (P2PS) modulates the cross talk contribution from the traces.
  - Let us define pair-to-pair spacing as a multiple of dielectric height. Example, P2PS=20xH (for stripline, H = min (H1, H2))

- To minimize the trace cross talk to a small level, consider the following rough guidelines

<table>
<thead>
<tr>
<th>Dielectric 1</th>
<th>Dielectric 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>H1</td>
<td>H2</td>
</tr>
<tr>
<td>Ground</td>
<td>Ground</td>
</tr>
</tbody>
</table>

Spacing where Cross-talk reduces significantly:

- Microstrip, far-end cross talk: > ~13xH
- Microstrip, near-end cross talk: > ~7xH
- Stripline, near-end cross talk: > ~4xH
USB4™ System Design Guidelines

Electrical Design Considerations

Physical Design Considerations
- Trace geometry
- Routing practices, vias, and component placement
- Layout design

Component selection
Routing on Microstrip Layer

- Routing on microstrip presents a challenge from far-end cross talk (FEXT) between two adjacent Tx or Rx pairs which increases as routing length increases.
  - Example: an 8” of routing can have up to 4% FEXT when spacing is 7xH.

- Mitigation options:
  - Use more than one layer to avoid placing two Tx or Rx pairs adjacent to each other.
  - Use large spacing as shown in previous slide.

- Consider interleaved routing, where you can increase the effective distance between two Tx or Rx without spending more board area. The trade-off is some additional near-end cross talk (NEXT).

*Microstrip, far-end cross talk*

<table>
<thead>
<tr>
<th>Spacing &gt; ~13xH</th>
</tr>
</thead>
</table>

**Non-interleaved Routing**

- Tx
- Rx

| 7xH | 7xH | 7xH |

| FEXT, 4% | NEXT, 0.2% | NEXT, 0.1% |

**Interleaved Routing**

- Tx
- Rx

| 7xH | 7xH | 7xH |

| FEXT, 0.3% | NEXT, 0.2% | NEXT, 0.2% |
Vertical Transitions

- Avoid via stubs or minimize the length of the stub. Long stubs will negatively impact return loss, insertion loss, (hence ISI, hence DDJ), and ultimately end to end margins (e.g. COM)

<table>
<thead>
<tr>
<th>COM</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Stub</td>
</tr>
<tr>
<td>Short Stub (250um)</td>
</tr>
<tr>
<td>Long Stub (840 um)</td>
</tr>
<tr>
<td>Baseline</td>
</tr>
<tr>
<td>Baseline - 0.2dB</td>
</tr>
<tr>
<td>Baseline - 0.8dB</td>
</tr>
<tr>
<td>Failed COM</td>
</tr>
</tbody>
</table>

- As mitigation options, consider the following
  1. Optimize impedance discontinuity by adjusting via pitch, diameter, pad/anti-pad size
  2. Other via technologies: Back-drilled via or uVia (Type-4 PCB)
  3. Routing only on surface layers
  4. If a via stub is inevitable, assess your design w/ return loss or COM simulations.

=> A long via stub will likely cause compliance and/or margin failure. Must avoid it!
## Component Placement

- Each device/components presents an impedance discontinuity because of its internal structure as well as its parasitic (e.g. its SMT pads).

- Placing as many discontinuities (devices, SMT components, vias, etc) as you can close to each other can help improve return loss (hence ISI, hence DDJ) and/or end to end margins (e.g. COM).

  **Design Tip:** Avoid placing the ESD, ac-cap, and bleed resistors halfway between the IC package and the USB-C connector. Try to place them closer to either the IC package or the USB-C connector.

| Close to USB-C | COM
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline</td>
<td>Baseline + 1dB</td>
</tr>
<tr>
<td>Close to the IC PKG</td>
<td>Baseline - 0.9dB</td>
</tr>
<tr>
<td>Halfway between</td>
<td>Baseline</td>
</tr>
</tbody>
</table>

---

![Diagram showing component placement and graph of return loss vs frequency](image-url)
• Electrical Design Considerations

• **Physical Design Considerations**
  • Trace geometry
  • Routing practices, vias, and component placement
  • **Layout design**

• Component selection
Layout Design Guidelines - 1/7

- With signal vias, there needs to be proper stitching/return vias. For instance, a L1-L4 transition requires stitching via from L2 to L3 as well as L5 (L3 and L5 are reference planes for trace when it is routed on L4). **Pay special attention to this on Type4 PCBs**

- Symmetric placement of stitching vias is desired to minimize mode conversion
Layout Design Considerations/Examples - 2/7

• Adjacent via pairs must be isolated with GND vias to minimize cross talk
  • Staggering the via pair left and right should provide room for placing GND via
Layout Design Considerations/Examples - 3/7

- USB4 traces should not be routed over voids or reference plane splits
  - In fact, it’s best to maintain a 3xH (H: height of dielectric) between trace edge and void to minimize impedance discontinuity and mode conversion
Layout Design Considerations/Examples - 4/7

• Entrance to and exit from vias should be symmetric
Layout Design Considerations/Examples - 5/7

- Void under SMT pads for better SI. The larger the pad size, the more important this is

- **Single-ended voids** are recommended for most cases/components

- **Differential voids** for larger pads and/or thin dielectric height (<~60um)
  - These voids can over-compensate (increase impedance too much). So analysis/3D modeling may be needed

- Ensure that layer under the void (surface-2) is not a source of noise, e.g. power plane. It’s best to have ground on surface-2 under the void
Layout Design Considerations/Examples - 6/7

- P/N length mismatch may be inevitable (due to pin out for example). Adequate P/N length matching should be considered. Any technique to achieve matching should consider the following:
  - P/N length matching should occur as close as possible to where the mismatch happens
  - Serpentine/sawtooth routing is a way to reduce P/N length mismatch, but shape of serpentine/sawtooth should be optimized
Layout Design Considerations/Examples - 7/7

• The bends on USB4 traces should be smoothened. This should improve return loss at high frequencies

[Images showing high speed traces routed with sharp bends and smooth bends]
Fiberweave Effect

- PCBs are constructed from woven fiberglass fabric bound together with epoxy resin. The glass and epoxy have different dielectric constants.

- One half of a differential pair can run over epoxy and the other half over glass weave. Therefore, propagation delay is different between D+ and D- causing skew, which causes degraded insertion loss as well as common mode noise (i.e. mode conversion)
  - The degradation increases as the length of trace increases

- **Mitigation options are required for USB 4 speeds**

  - Layout mitigation techniques:
    - Angled routing
    - Zig-zag routing
    - PCB vendor rotates image of the board
    - Tighter weaves
    - Many more ....
USB4™
System Design Guidelines

• Electrical Design Considerations
• Physical Design Considerations
  • Trace geometry
  • Routing practices, vias, and component placement
  • Layout design

• Component selection
AC-Caps and Discharge Resistors

- Smaller size components (e.g. 0201) will have smaller parasitic and therefore better return loss than larger ones (0402). Consider using 0201 components.

<table>
<thead>
<tr>
<th>AC-Cap Between ICs/Retimers</th>
<th>Value</th>
<th>Voltage Rating</th>
<th>Tx</th>
<th>Rx</th>
</tr>
</thead>
<tbody>
<tr>
<td>135-265nF</td>
<td>5V</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Tx AC-Cap</td>
<td>25V</td>
<td>X</td>
<td>NA</td>
<td>X</td>
</tr>
<tr>
<td>Rx AC-Cap</td>
<td>300-363nF</td>
<td>25V</td>
<td>NA</td>
<td>X</td>
</tr>
<tr>
<td>Rx bleed/Discharge resistor</td>
<td>200-242 KΩ</td>
<td>25V</td>
<td>NA</td>
<td>X</td>
</tr>
</tbody>
</table>

X: Mandatory  O: Optional  NA: Not Applicable

0201 w/void under pad
0402 w/ void under pad
**ESD**

- Selection of an ESD is very important as it introduces a significant impedance discontinuity.
- Recommend using an ESD whose return loss and insertion loss is similar or better than shown below:

**Example: Impact of a poorly selected ESD:** an ESD that fails the RL guideline by ~4.3 dB and the IL by 0.4 dB has a large impact to COM and degrades return loss at TP2 when used in short channel.

<table>
<thead>
<tr>
<th>COM</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Good ESD</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Baseline</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bad ESD</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Baseline - 0.9 dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>=&gt; Failing COM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Referenced to 85 Ohms differential.*
PCB Material

- **PCB Thickness**: The tradeoff for thinner PCBs (=>thinner dielectric) is higher trace loss
  - Example: notice the dependence of loss per inch to dielectric height for a microstrip

<table>
<thead>
<tr>
<th>Dielectric height</th>
<th>2.7 mils</th>
<th>2.5</th>
<th>2.3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Loss @ 10GHz (dB/inch)</td>
<td>1.66</td>
<td>1.72</td>
<td>1.82</td>
</tr>
</tbody>
</table>

- **Mitigation options for reducing loss, especially in thin PCBs**:  
  - PCB material and copper selection  
  - Optimizing trace geometry (less effective for thin PCBs)

- **Dielectric Loss**  
  - Low loss and mid loss materials can recover the interconnect reach when using a thin PCB

<table>
<thead>
<tr>
<th></th>
<th>Diff. Loss Per Inch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Regular loss (Df = 0.015)</td>
<td>1.8dB/inch</td>
</tr>
<tr>
<td>Mid loss (Df = 0.011)</td>
<td>1.6dB/inch</td>
</tr>
<tr>
<td>low loss (Df = 0.005)</td>
<td>1.2 dB/inch</td>
</tr>
</tbody>
</table>

- **Example**: Stripline w/ D1/D2~=60um

- **Copper Foil Roughness**  
  - At USB4 Gen 3 data rate, copper roughness impacts loss.

<table>
<thead>
<tr>
<th>Loss per inch @ 10GHz</th>
<th>Ultra-smooth</th>
<th>Smooth</th>
<th>Less rough</th>
<th>Very Rough</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microstrip</td>
<td>1.34</td>
<td>1.43</td>
<td>1.52</td>
<td>1.6</td>
</tr>
<tr>
<td>Stripline (thin PCB)</td>
<td>1.66</td>
<td>1.83</td>
<td>2</td>
<td>2.16</td>
</tr>
</tbody>
</table>
Summary

• Two categories of channel/interconnect => different design targets/priorities
• Explicit electrical design targets per the USB4 spec
  • Loss => ISI => DDJ
  • Return loss
• Optimize trace geometry for Impedance, loss, and cross talk
• Routing practices
  • Reduce cross talk by interleaved routing
  • Avoid via stubs
  • Optimize the placement of discrete components (e.g. AC-caps, ESD, etc)
• Layout design guidelines
• Fiberweave effect and mitigation techniques
• Correct values and voltage rating of Rs and Cs
• Choose an ESD with better or equal to the recommended electrical performance
• PCB dielectric material and copper has large impact on trace loss at USB4 data rates
Time for Q&A