USB4™ Electricals Layer

Ehud (Udi) Shoor *– Sr. Principal Engineer, Intel*

USB Developer Days 2019 – Taipei, Taiwan

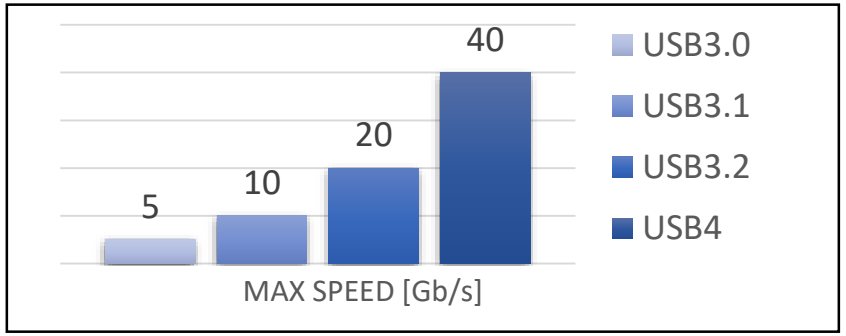
November 19, 2019

Agenda

- Background
- Transmitter Specifications
- Receiver Specifications
- Testability

General Background

- USB4™ standard supports speeds of up 40Gb/s per port, obtained by dual-lane operation with up to 20Gb/s per lane



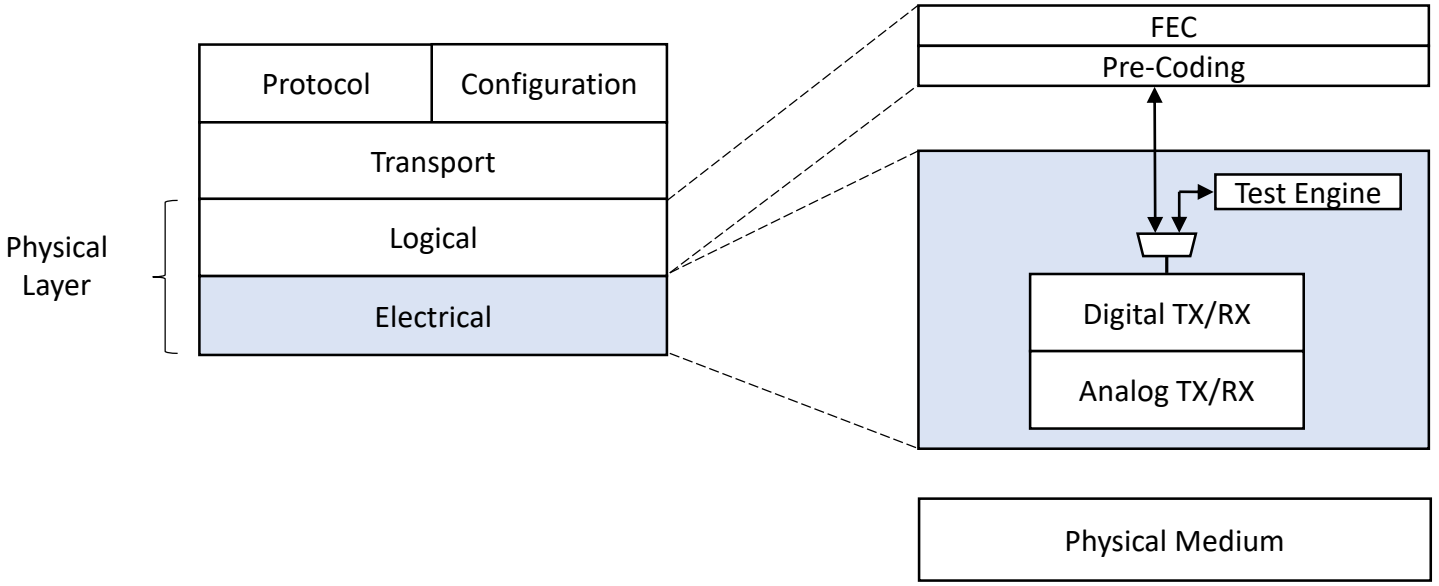
- New Forward Error Correction capabilities added for obtaining enhanced data integrity needed for supporting compressed display
- USB4™ Interconnect Configurations:

Speed per Lane	Passive Cables	Active Cables
Gen2 (10Gb/s)	2m (1)	10's of meters
Gen3 (20Gb/s)	0.8m (2)	10's of meters

(1) Normative cable spec of 12dB at 5GHz
(2) Normative cable spec of 7.5dB at 10GHz

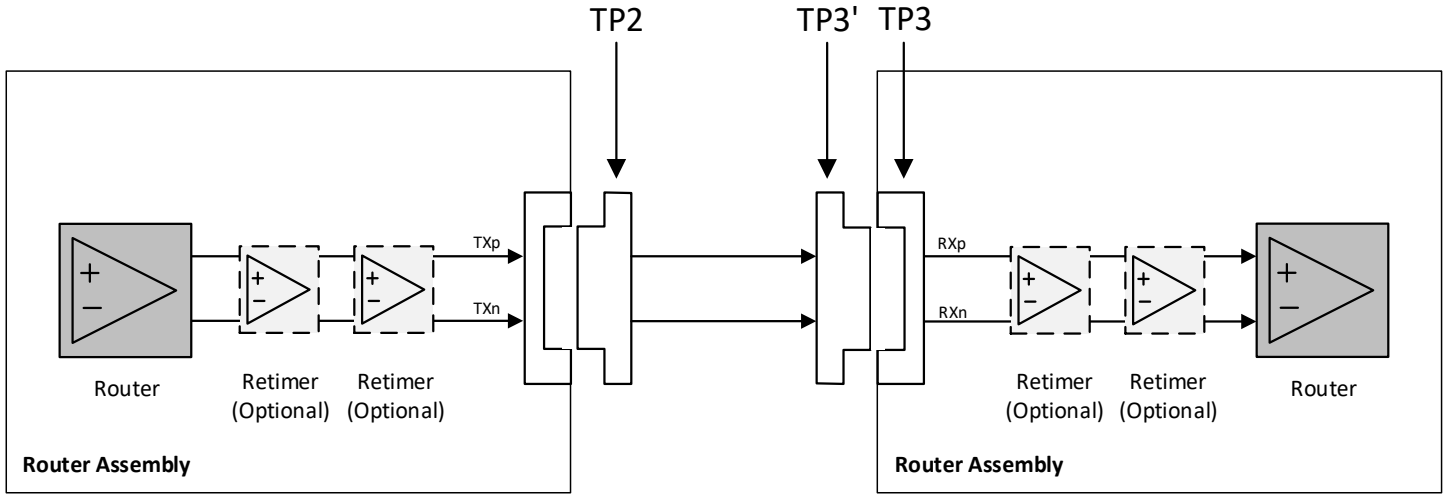
Electrical Layer Background

- The Electrical Layer specifications detail the requirements and testing methodologies required for achieving reliable communication over USB4™ channels
  - Characterized in stand-alone manner, without depending on the upper layers of the protocol for obtaining simplicity



Electrical Compliance Testing

- The electrical specifications are defined for a Router Assembly and measured at the USB Type-C® connector using compliance plug and receptacle fixtures



* Router Assembly is comprised of a Router and up to 2 Re-timers placed between the Router and the USB Type-C connector

** Informative Insertion-Loss of the internal Router Assembly channel: 5.5dB @ 5GHz, 7.5dB @ 10GHz

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- **Transmitter Specifications**
- Receiver Specifications
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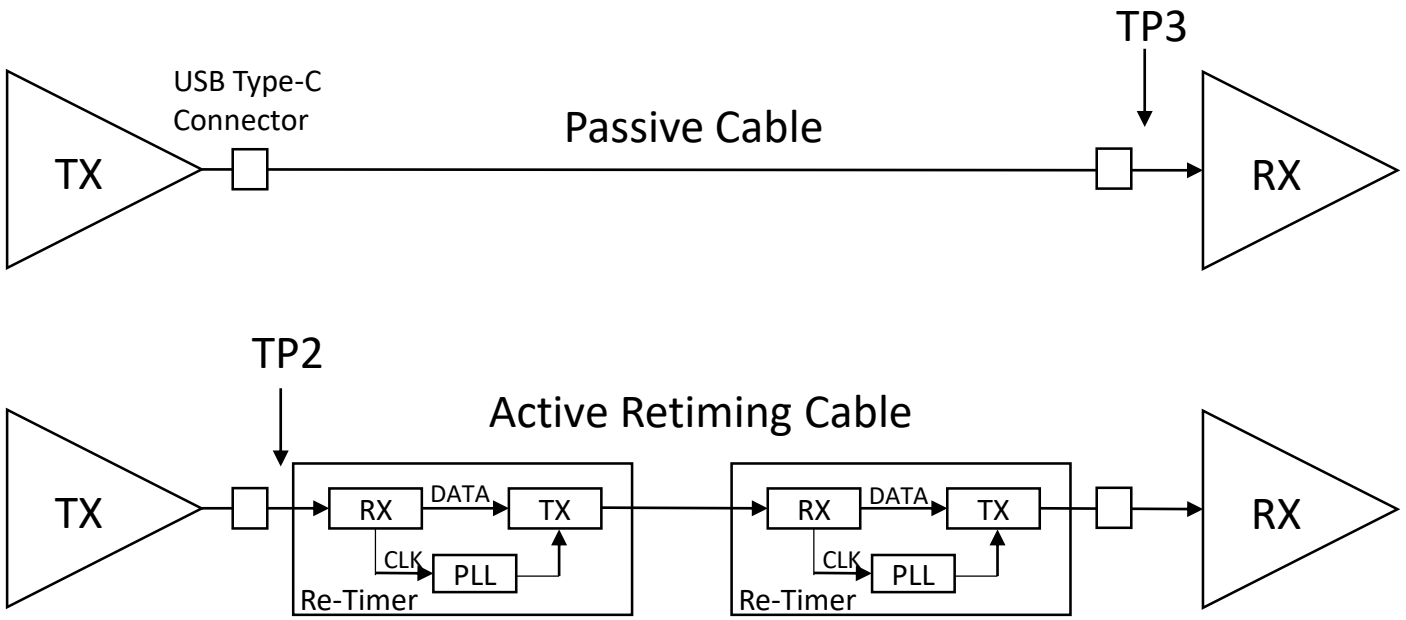
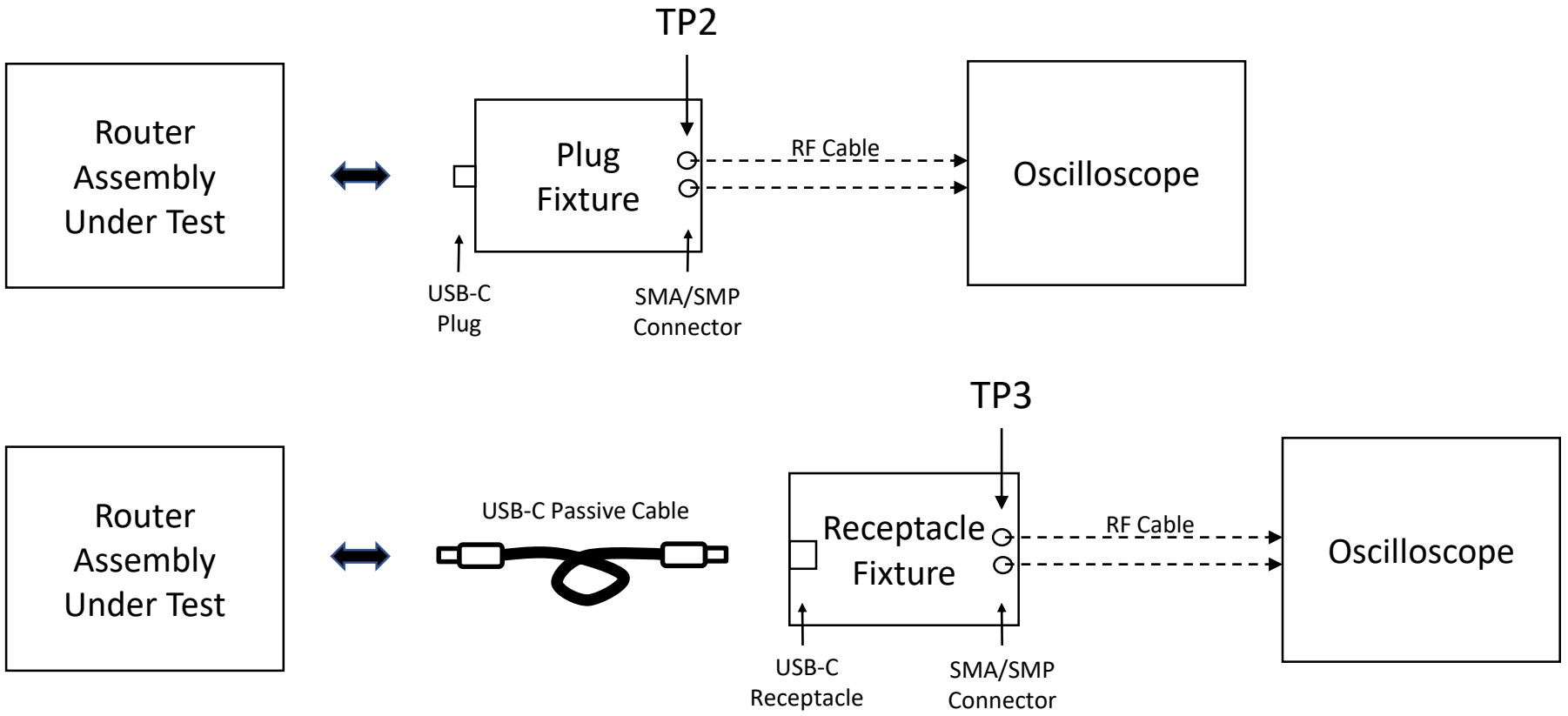
Transmitter Measurement Points

- The Transmitter compliance testing is defined at TP2 and TP3 measurement points:



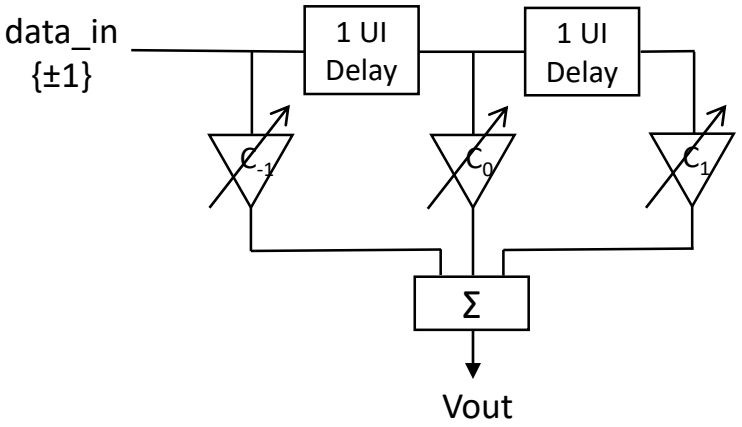
Transmitter Measurement Setup

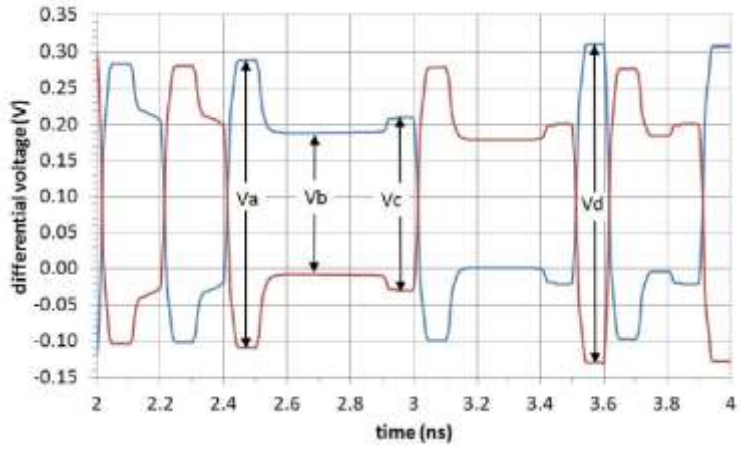
- TP2 measurements are done using plug-fixture connected to the near receptacle
- TP3 measurements are done using receptacle fixture connected to cable output



Transmitter Equalization

- Tunable TX equalizer is supported, configured by the RX during the training period





Preset Number	Pre-shoot [dB]	De-emphasis [dB]	Informative Filter Coefficients		
			C_{-1}	C_0	C_1
0	0	0	0	1	0
1	0	−1.9	0	0.90	−0.10
2	0	−3.6	0	0.83	−0.17
3	0	−5.0	0	0.78	−0.22
4	0	−8.4	0	0.69	−0.31
5	0.9	0	−0.05	0.95	0
6	1.1	−1.9	−0.05	0.86	−0.09
7	1.4	−3.8	−0.05	0.79	−0.16
8	1.7	−5.8	−0.05	0.73	−0.22
9	2.1	−8.0	−0.05	0.68	−0.27
10	1.7	0	−0.09	0.91	0
11	2.2	−2.2	−0.09	0.82	−0.09
12	2.5	−3.6	−0.09	0.77	−0.14
13	3.4	−6.7	−0.09	0.69	−0.22
14	3.8	−3.8	−0.13	0.74	−0.13
15	1.7	−1.7	−0.05	0.55	−0.05

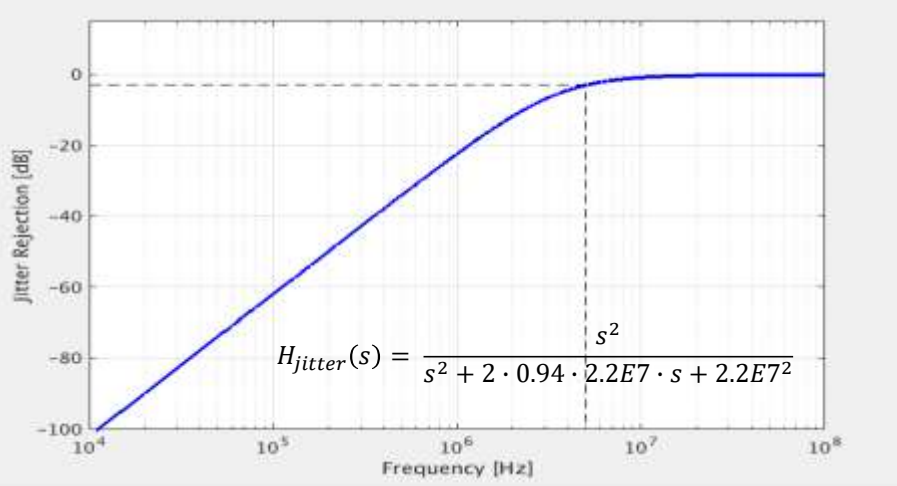
$$Preshoot = 20 \cdot log\left(\frac{V_c}{V_b}\right) = 20log_{10}\left(\frac{-C_{-1} + C_0 + C_1}{C_{-1} + C_0 + C_1}\right)$$

$$Deemphasis = 20 \cdot log\left(\frac{V_b}{V_a}\right) = 20log_{10}\left(\frac{C_{-1} + C_0 + C_1}{C_{-1} + C_0 - C_1}\right)$$

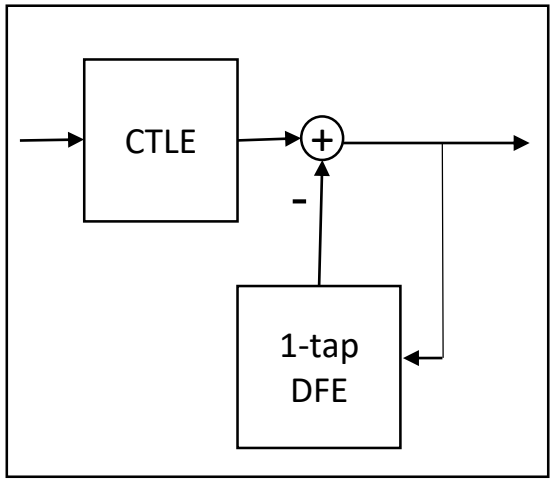
Transmitter Eye Measurement

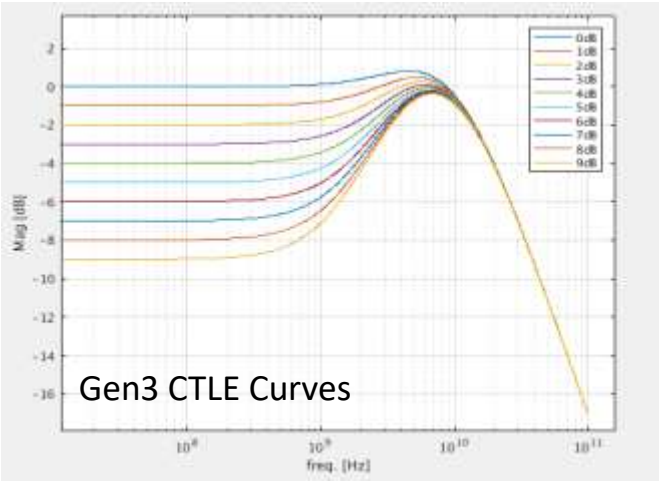
- The Transmitter eye measurements are performed using reference CDR and Receiver equalization functions
- The reference CDR is modeled by a 2nd order PLL response (type II)
- The reference RX equalizer is defined with CTLE and 1-tap DFE, applied on TP3 (post cable) measurements

Jitter Rejection Function (|1-CDR(s)|)

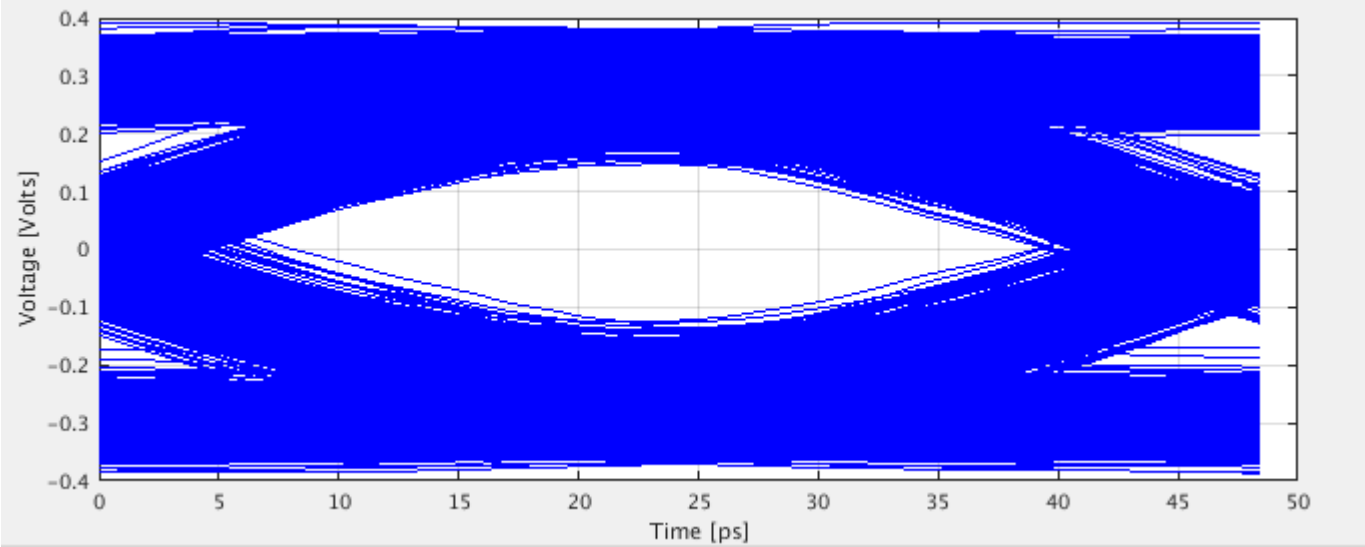


Reference RX Equalizer





Transmitter Voltage Requirements



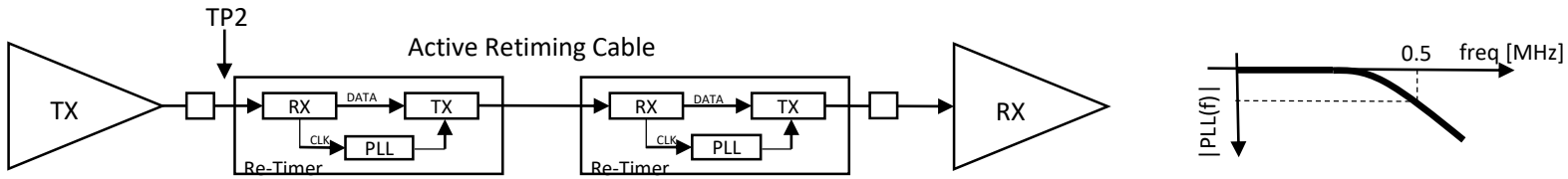
Speed per Lane	Eye Height @ TP2	Eye Height @ TP3
Gen2 (10Gb/s)	140 mV pk	47 mV pk
Gen3 (20Gb/s)	120 mV pk	49 mV pk

- Measured over 10^6 UI
- Eye-Height at TP3 is measured after applying reference receiver equalizer

Transmitter Jitter Requirement

	Gen2		Gen3		Units
	TP2	TP3	TP2	TP3	
Total Jitter (TJ)	0.38	0.60	0.46	0.60	UI pk-pk
Uncorrelated Jitter (UJ)	0.31	0.31	0.31	0.31	UI pk-pk
Uncorrelated Deterministic Jitter (UDJ)	0.17	0.17	0.17	0.17	UI pk-pk
Data-Dependent Jitter (DDJ)	0.15	NA	0.21	NA	UI pk-pk
Duty-Cycle-Distortion (DCD)	0.03	NA	0.03	NA	UI pk-pk
Low Frequency UDJ (UDJ_LF)	0.04	NA	0.07	NA	UI pk-pk

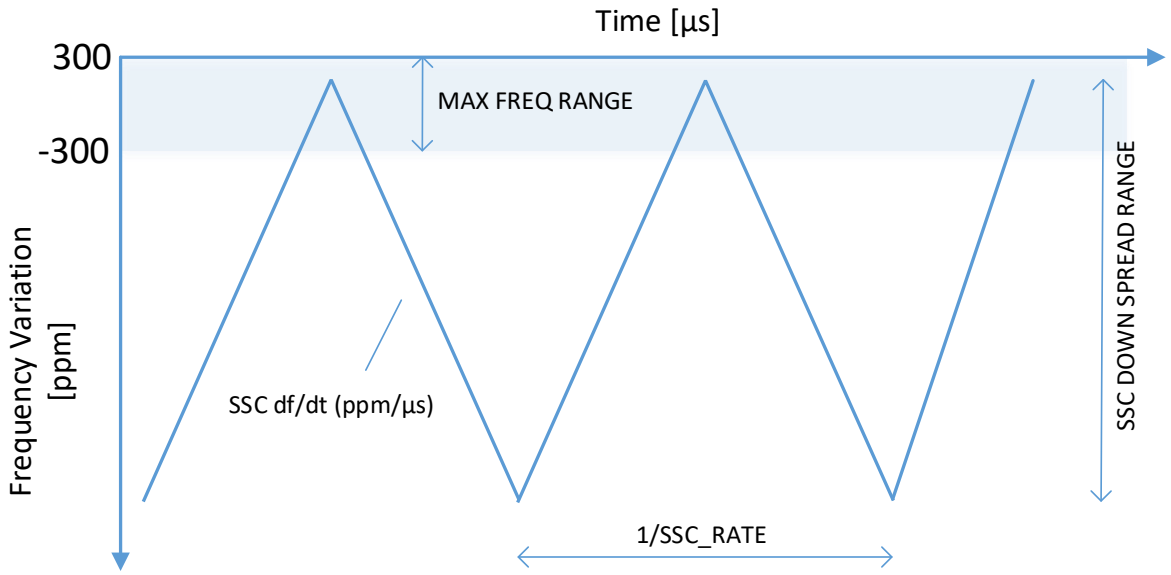
* The TJ and UJ are referenced to 1E-13 statistics (adding some margin with respect to the 1E-12 target BER)



Transmitter SSC

- The transmitter is required to support Spread-Spectrum-Clocking (SSC) in its steady-state operation

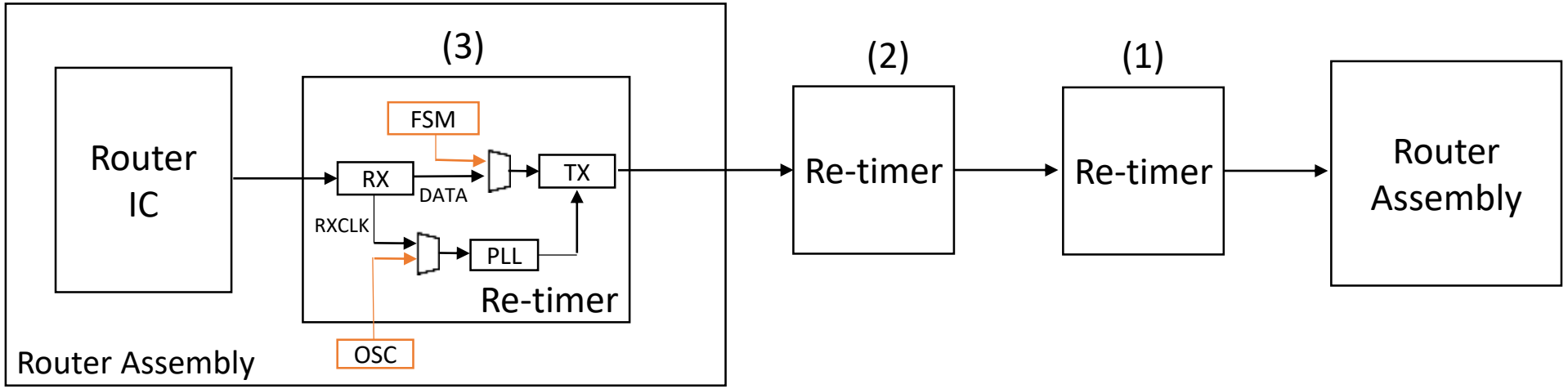
Example Transmitter Frequency During Steady-State



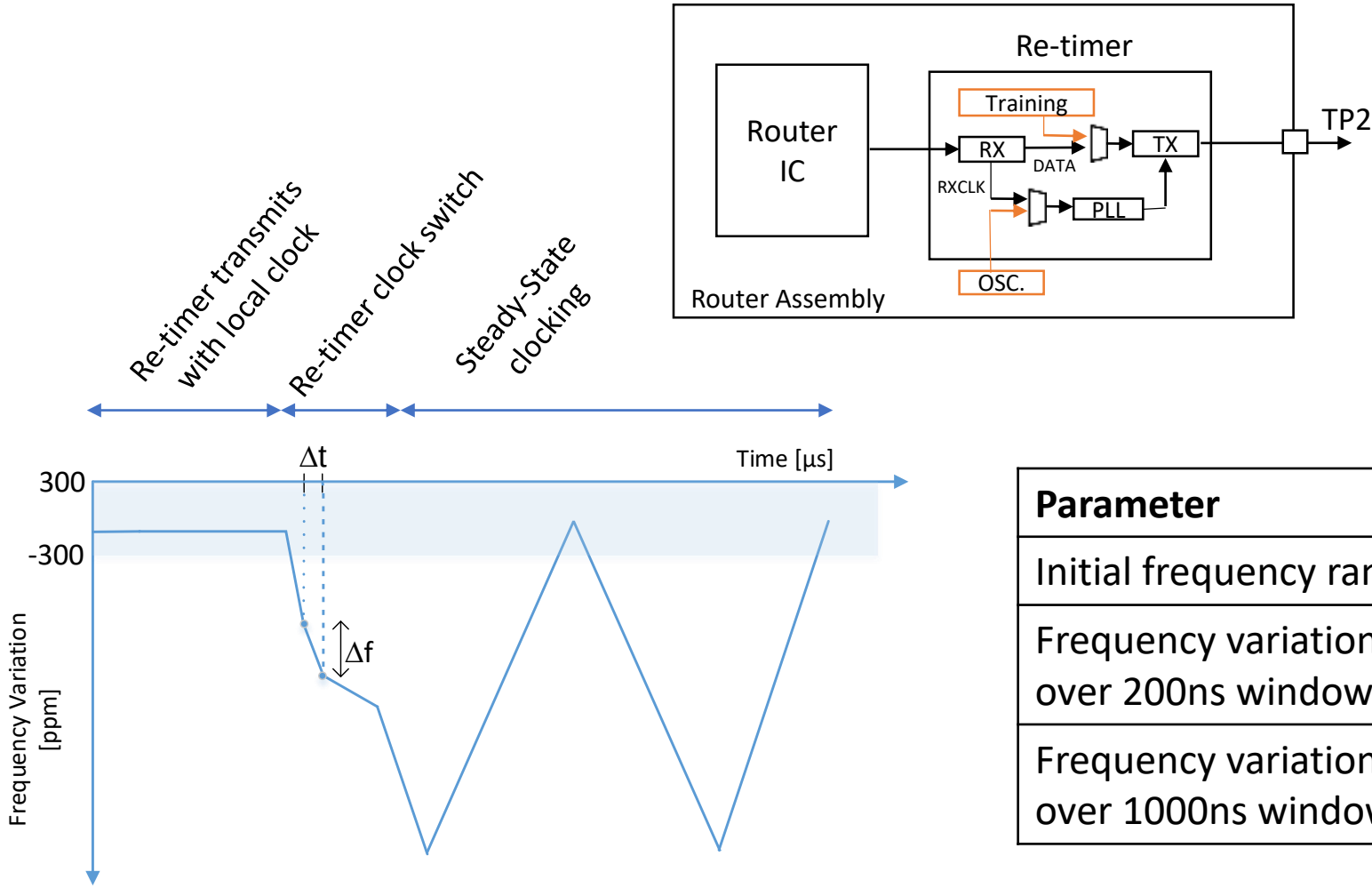
Parameter	Min	Max	Units
MAX Freq Range	-300	300	ppm
Down-Spread Range	0.4	0.5	%
SSC Rate	30	33	KHz
SSC df/dt		1250	ppm/us
SSC Phase Deviation	2.5	22	ns p-p

Transmitter Clocking During Training

- Router Assembly may include up to 2 Re-timers on top of the Router IC
- Link training flow:
  - Initially, all Re-timers transmit local training data using local clock (without SSC) for training the entire link segments in parallel
  - When the receivers are trained, the Re-timers sequentially switch to forward the incoming data using the recovered clock
- Specifications are defined for constraining the output frequency variations during the transition from initial training to steady state operation



TX Frequency Variations During Training

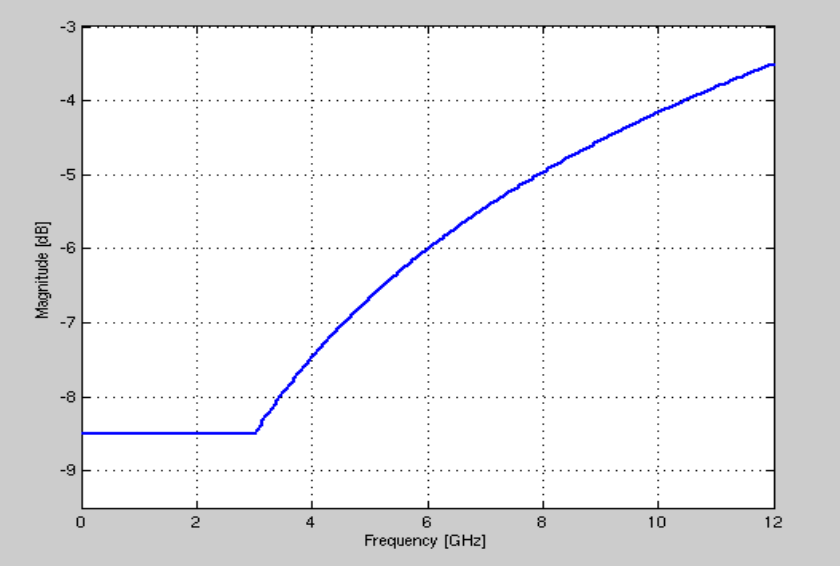


Parameter	Min	Max	Units
Initial frequency range	–300	300	ppm
Frequency variation over 200ns window		1400	ppm
Frequency variation over 1000ns window		2200	ppm

Transmitter Return-Loss

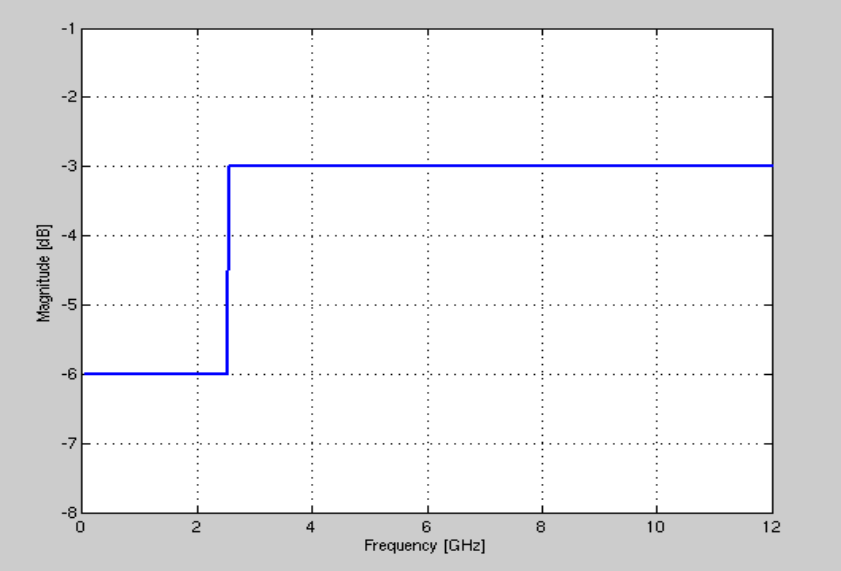
- The Router Assembly Transmitter Return-Loss is measured at the near connector in TP2 reference point (at the output of a compliance plug fixture) referenced to a single-ended impedance of 42.5 Ω

TX Differential Return-Loss Mask



$$\text{SDD22(f)} = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$

TX Common-Mode Return-Loss Mask



$$\text{SCC22(f)} = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$

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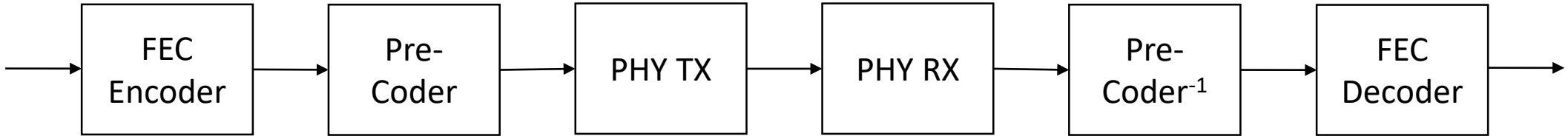
- Transmitter Specifications
- **Receiver Specifications**
- Testability

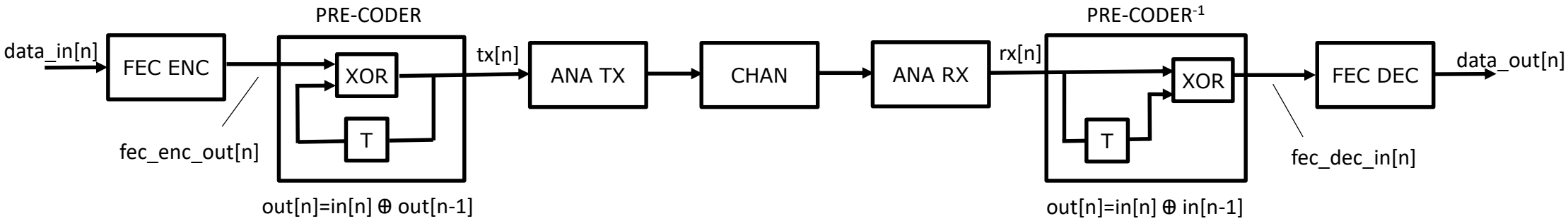
Introduction



- USB4™ data path employs combination of Forward Error Correction (FEC) and Pre-Coding for obtaining enhanced data integrity
- The FEC is based on low-complexity/low-latency Reed-Solomon RS(198,194) over GF(2^8) with two correctable errors per block
- The Pre-Coder is designed for converting bursts of consecutive bit-errors into two errors at the beginning and end of the burst, supported by the RS FEC
- As a result, high level of protection is obtained for long bursts of errors, which might be introduced by Decision-Feedback-Equalizers (DFE)
- Therefore, the coded BER performance is not affected by long bursts of errors but mainly by the uncoded BER and by secondary DFE effect of multi error bursts

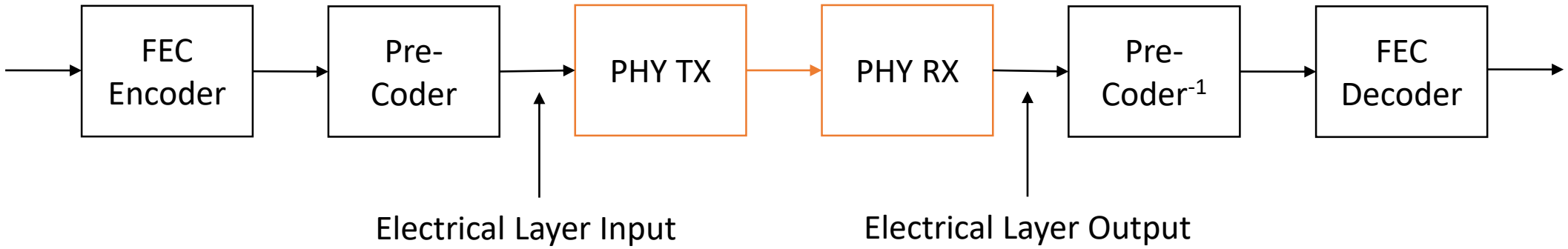
USB4 Data-Path Example

- Bursts of errors are converted by the pre-coding into 2 errors at the beginning and end of the burst, supported by the RS FEC



fec_enc_out[n]		1	0	1	1	0	1	0	0	1	1	1	0	1	0	1
tx[n]	0	1	1	0	1	1	0	0	0	1	0	1	1	0	0	1
rx[n]	0	1	1	0	0	0	1	1	1	0	1	0	1	0	0	1
fec_dec_in[n]		1	0	1	0	0	1	0	0	1	1	1	1	1	0	1

RX Testing Methodology

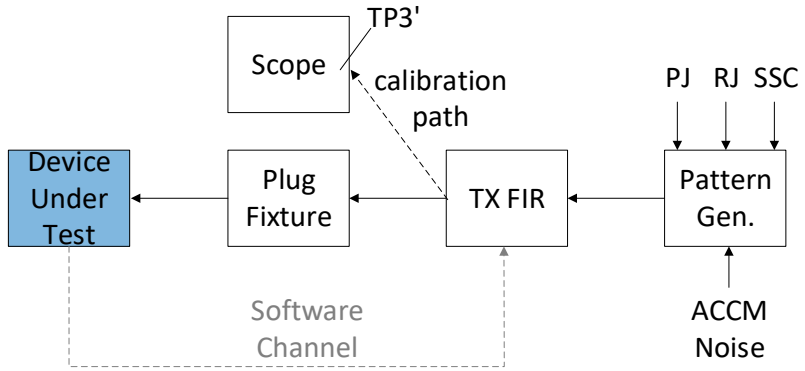


- The Electrical performance is tested in stand-alone mode without applying Pre-Coding nor Forward-Error-Correction
  - The testing is based on PRBS patterns driven by pattern-generator
- The coded BER performance cannot be measured directly due to the large measurement window needed (several years…) and therefore validated indirectly based on electrical layer indicators

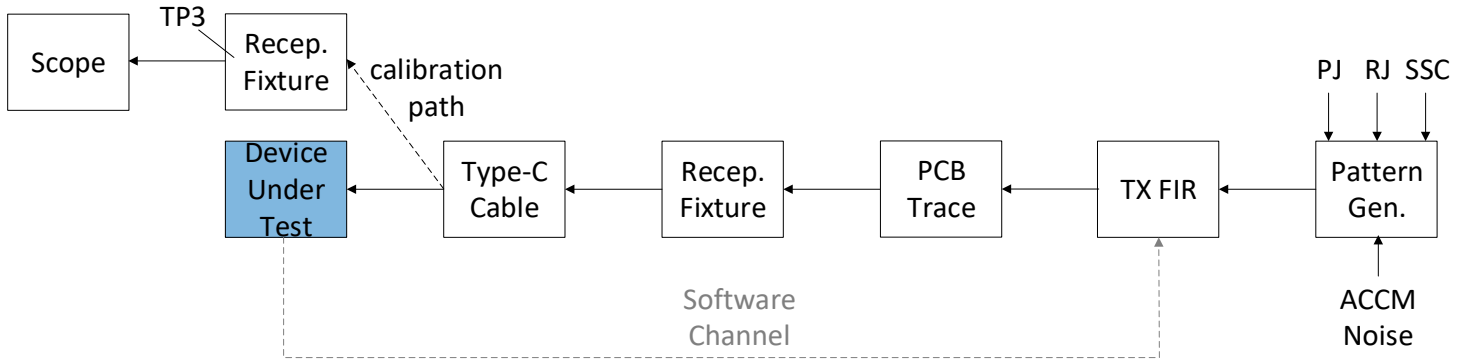
Receiver Uncoded BER

- The Receiver shall operate at uncoded BER of 1E–12 with stressed signal applied
- Two test setups are used for evaluating the receiver tolerance:
  - “Case 1” addressing installations with low Insertion-Loss
  - “Case 2” addressing installations with maximum Insertion-Loss

Case 1:



Case 2:



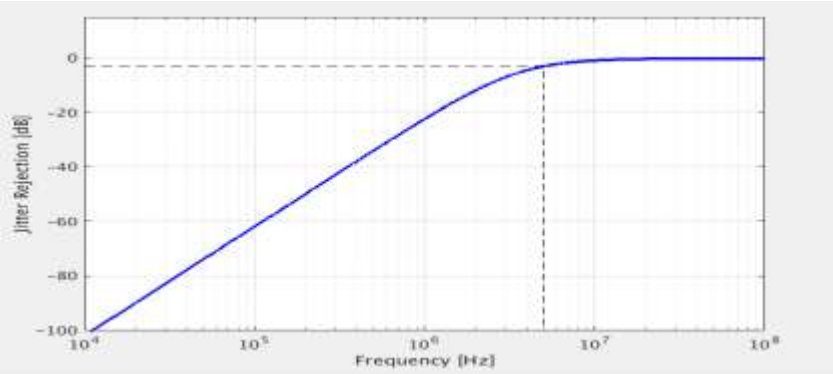
Uncoded BER Test Setup

- The Receiver tolerance test is performed with PRBS31 pattern and calibrated as following:

Speed	Test Case	Inner Eye [mV pk]	RJ [UI pp]	PJ [UI pp]	TJ [UI pp]
Gen2	Case1 (TP3')	350	0.14	0.17	0.35
	Case2 (TP3)	47	0.14	0.17	0.60
Gen3	Case1 (TP3')	350	0.14	0.17	0.38
	Case2 (TP3)	49	0.14	0.17	0.60

PJ Freq. [MHz]	Absolute Value [UI pp]	Filtered value [UI pp]
1	2.22	0.17
2	0.66	0.17
10	0.19	0.17
50	0.17	0.17
100	0.17	0.17

- Each test is repeated for several different PJ frequencies, calibrated to 0.17UI pk-pk at the output of the jitter rejection mask

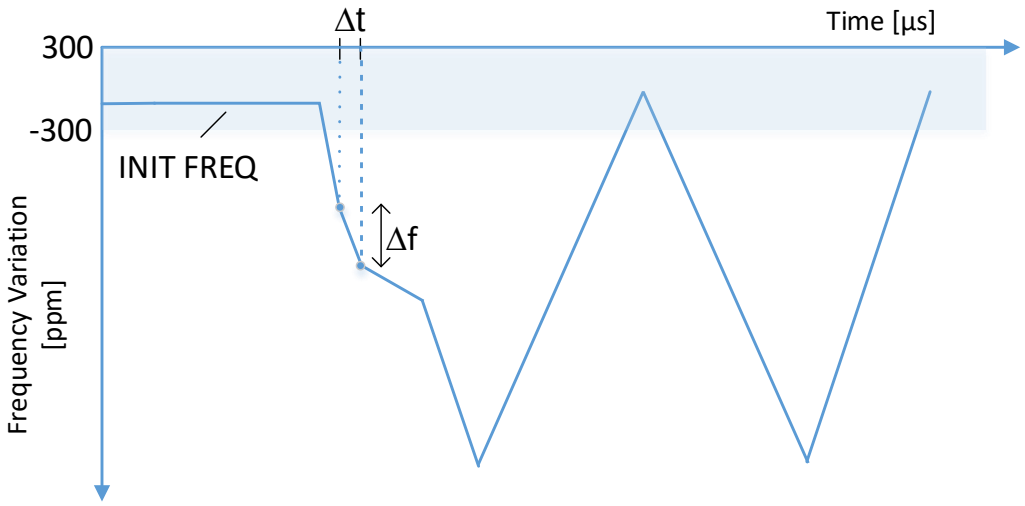


Multi Error Burst Probability

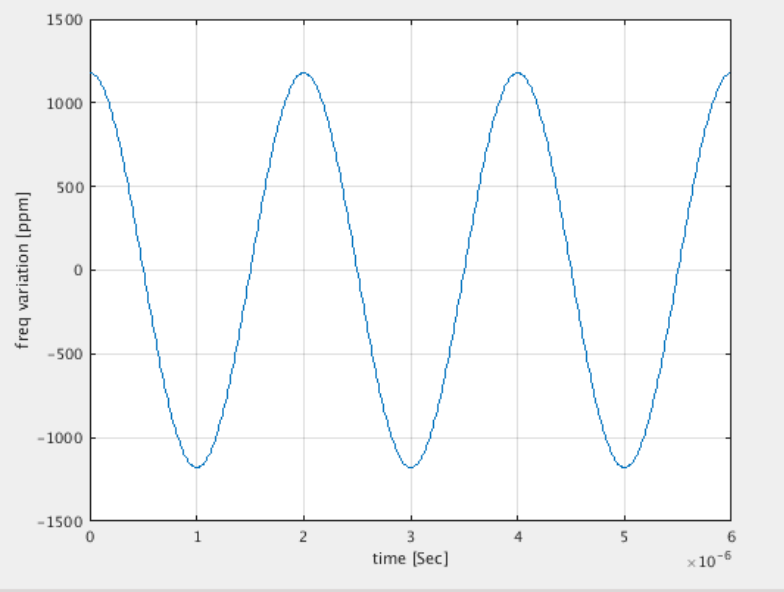
- When a Receiver employs DFE with more than 1-tap, it shall take steps to limit the probability that a burst of errors is restarted after receiving one or more correct bits
  - When error burst ends, the 1st DFE tap is fed with correct data but errors still exist in the DFE pipeline
- The Burst Restart probability is characterized as following:
  - Initialize the test setup to “Case 2” configuration, with PJ frequency of 100MHz (PRBS31 pattern, neither FEC nor Pre-Coding is applied)
  - Increase the PJ magnitude to the point where uncoded BER of 1E–8 is observed
  - The Receiver under test shall trigger on random bit-errors and capture errors that follow (referenced as Error Captures)
    - Error Capture shall start with bit-error that is preceded by at least 32 consecutive bits without errors
  - The probability for obtaining Burst Restart events shall not exceed 5E–7 (i.e., one error burst restart per 2 million error captures on average)

Input Phase Variations During Training

- The Receiver shall track incoming frequency variations during the link training created by far-end Re-timer's transmitter clock switching
  - No need for meeting BER<1E–12 but only to maintain the CDR tracking



The CTS specifies equivalent test using PJ tones with similar df/dt characteristics



Receiver Return-Loss

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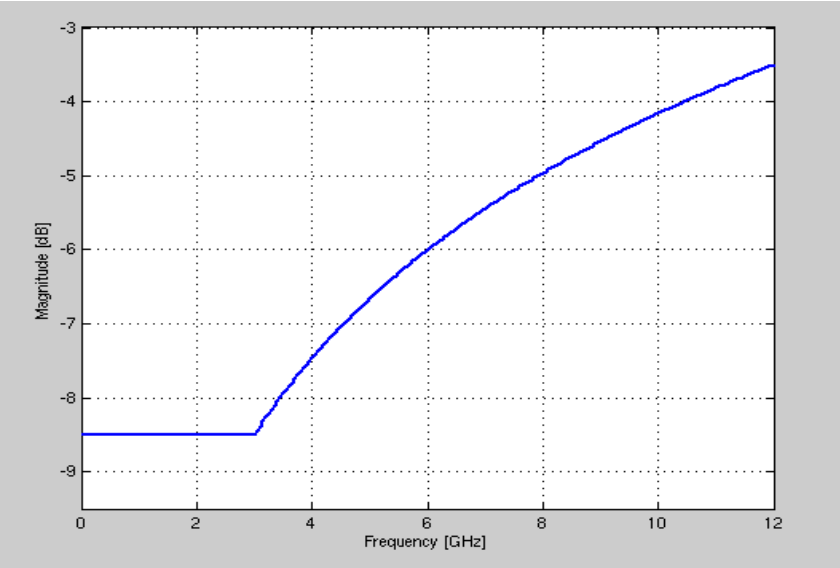
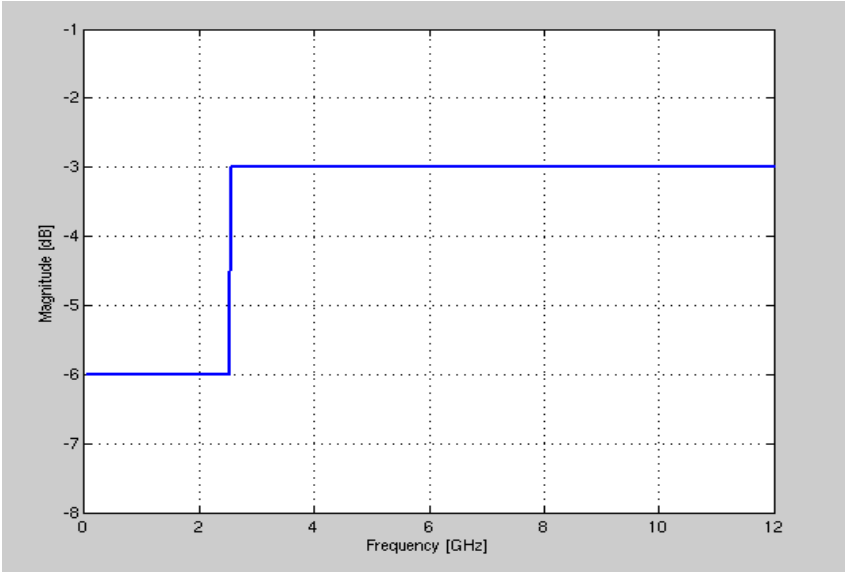
RX Differential Return-Loss Mask



$$\text{SDD11(f)} = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$

RX Common-Mode Return-Loss Mask



$$\text{SCC11(f)} = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$

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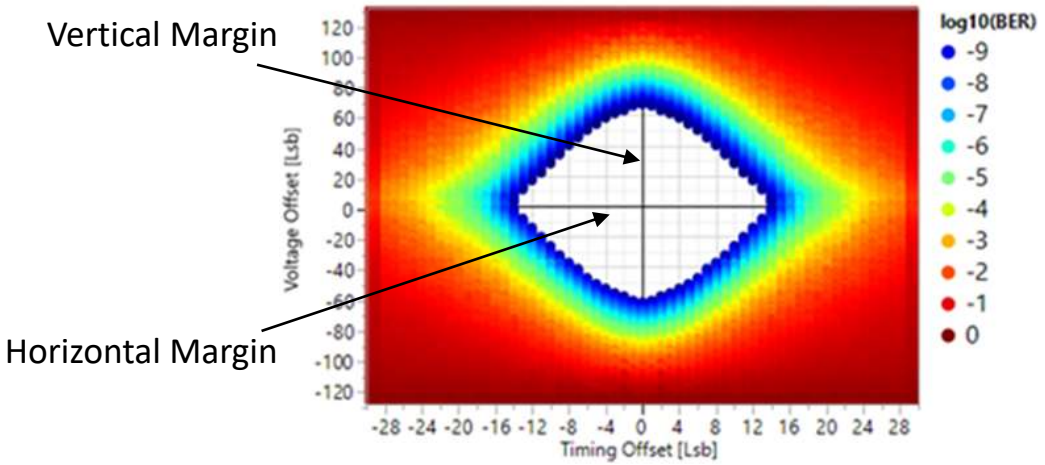
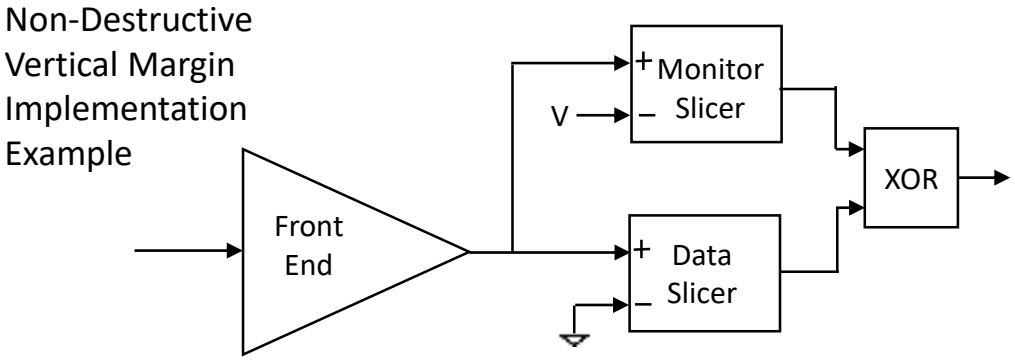
Receiver Margining

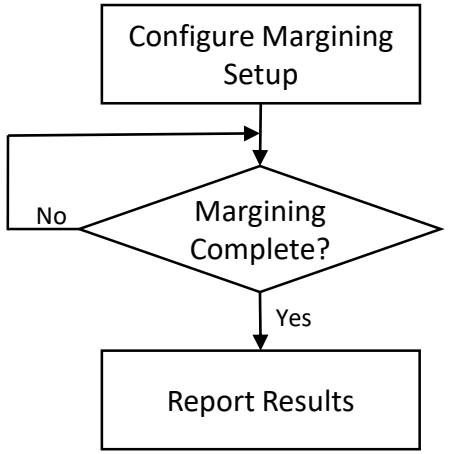
- USB4™ defines method for characterizing the RX margin per each of the link's instants
- The goal is to provide standard means for validating and debugging the link performance in production and in the field
  - The result is not used for determining compliancy but only for validation/debug
- All receivers need to support non-destructive voltage margining whereby a receiver sampler is offset from the nominal sampling position in the vertical axis
- Support for timing margining, whereby a receiver sampler is offset from the nominal sampling position in the horizontal dimension is optional





Receiver Margining Flow

- The Receiver Margining flow includes the following steps:
  - Configure the test parameters (lane, voltage/timing margin, BER target etc.)
  - Gradually decrease the vertical/horizontal margin and check for errors (monitor slicer errors in the non-destructive case, HEC/FEC errors in the destructive case)
  - Report margin result
- USB4™ port needs to support either “Software Margining Mode” or “Hardware Margining Mode” (may optionally support both):
  - Hardware Mode:
    The margining flow is mostly performed internally by the PHY hardware/firmware while external software is only triggering the test and reads the margin result
  - Software Mode:
    The margining flow is mostly conducted by external software controlling the PHY hardware which configures the vertical/horizontal offset



Time for Q&A