USB4™ Electricals Layer

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Agenda

- Background
- Transmitter Specifications
- Receiver Specifications
- Testability
**General Background**

- **USB4™** standard supports speeds of up to 40Gb/s per port, obtained by dual-lane operation with up to 20Gb/s per lane.

- New Forward Error Correction capabilities added for obtaining enhanced data integrity needed for supporting compressed display.

- **USB4™** Interconnect Configurations:

<table>
<thead>
<tr>
<th>Speed per Lane</th>
<th>Passive Cables</th>
<th>Active Cables</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gen2 (10Gb/s)</td>
<td>2m (1)</td>
<td>10’s of meters</td>
</tr>
<tr>
<td>Gen3 (20Gb/s)</td>
<td>0.8m (2)</td>
<td>10’s of meters</td>
</tr>
</tbody>
</table>

(1) Normative cable spec of 12dB at 5GHz
(2) Normative cable spec of 7.5dB at 10GHz
Electrical Layer Background

- The Electrical Layer specifications detail the requirements and testing methodologies required for achieving reliable communication over USB4™ channels.
  - Characterized in stand-alone manner, without depending on the upper layers of the protocol for obtaining simplicity.
Electrical Compliance Testing

• The electrical specifications are defined for a Router Assembly and measured at the USB Type-C® connector using compliance plug and receptacle fixtures

* Router Assembly is comprised of a Router and up to 2 Retimers placed between the Router and the USB Type-C connector

** Informative Insertion-Loss of the internal Router Assembly channel: 5.5dB @ 5GHz, 7.5dB @ 10GHz
Agenda

• Background
• **Transmitter Specifications**
• Receiver Specifications
• Testability
Transmitter Measurement Points

- The Transmitter compliance testing is defined at TP2 and TP3 measurement points:

![Diagram showing Transmitter Measurement Points]

- TP2: Passive Cable and USB Type-C Connector
- TP3: Active Retiming Cable

- PLL, RX, TX, DATA, CLK, Re-Timer, PLL
Transmitter Measurement Setup

- TP2 measurements are done using plug-fixture connected to the near receptacle
- TP3 measurements are done using receptacle fixture connected to cable output
Transmitter Equalization

• Tunable TX equalizer is supported, configured by the RX during the training period

<table>
<thead>
<tr>
<th>Preset Number</th>
<th>Pre-shoot [dB]</th>
<th>De-emphasis [dB]</th>
<th>Informative Filter Coefficients</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>$C_{-1}$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>-1.9</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>-3.6</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>-5.0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>-8.4</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0.9</td>
<td>0</td>
<td>-0.05</td>
</tr>
<tr>
<td>6</td>
<td>1.1</td>
<td>-1.9</td>
<td>-0.05</td>
</tr>
<tr>
<td>7</td>
<td>1.4</td>
<td>-3.8</td>
<td>-0.05</td>
</tr>
<tr>
<td>8</td>
<td>1.7</td>
<td>-5.8</td>
<td>-0.05</td>
</tr>
<tr>
<td>9</td>
<td>2.1</td>
<td>-8.0</td>
<td>-0.05</td>
</tr>
<tr>
<td>10</td>
<td>1.7</td>
<td>0</td>
<td>-0.09</td>
</tr>
<tr>
<td>11</td>
<td>2.2</td>
<td>-2.2</td>
<td>-0.09</td>
</tr>
<tr>
<td>12</td>
<td>2.5</td>
<td>-3.6</td>
<td>-0.09</td>
</tr>
<tr>
<td>13</td>
<td>3.4</td>
<td>-6.7</td>
<td>-0.09</td>
</tr>
<tr>
<td>14</td>
<td>3.8</td>
<td>-3.8</td>
<td>-0.13</td>
</tr>
<tr>
<td>15</td>
<td>1.7</td>
<td>-1.7</td>
<td>-0.05</td>
</tr>
</tbody>
</table>

\[
\text{Preshoot} = 20 \cdot \log \left( \frac{V_c}{V_b} \right) = 20 \log_{10} \left( \frac{-C_{-1} + C_0 + C_1}{C_{-1} + C_0 + C_1} \right)
\]

\[
\text{Deemphasis} = 20 \cdot \log \left( \frac{V_b}{V_a} \right) = 20 \log_{10} \left( \frac{C_{-1} + C_0 + C_1}{C_{-1} + C_0 + C_1} \right)
\]
Transmitter Eye Measurement

- The Transmitter eye measurements are performed using reference CDR and Receiver equalization functions
- The reference CDR is modeled by a 2nd order PLL response (type II)
- The reference RX equalizer is defined with CTLE and 1-tap DFE, applied on TP3 (post cable) measurements

Jitter Rejection Function (|1-CDR(s)|)
Transmitter Voltage Requirements

- Measured over $10^6$ UI
- Eye-Height at TP3 is measured after applying reference receiver equalizer
# Transmitter Jitter Requirement

<table>
<thead>
<tr>
<th></th>
<th>Gen2</th>
<th>Gen3</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TP2</td>
<td>TP3</td>
<td>TP2</td>
</tr>
<tr>
<td>Total Jitter (TJ)</td>
<td>0.38</td>
<td>0.60</td>
<td>0.46</td>
</tr>
<tr>
<td>Uncorrelated Jitter (UJ)</td>
<td>0.31</td>
<td>0.31</td>
<td>0.31</td>
</tr>
<tr>
<td>Uncorrelated Deterministic Jitter (UDJ)</td>
<td>0.17</td>
<td>0.17</td>
<td>0.17</td>
</tr>
<tr>
<td>Data-Dependent Jitter (DDJ)</td>
<td>0.15</td>
<td>NA</td>
<td>0.21</td>
</tr>
<tr>
<td>Duty-Cycle-Distortion (DCD)</td>
<td>0.03</td>
<td>NA</td>
<td>0.03</td>
</tr>
<tr>
<td>Low Frequency UDJ (UDJ_LF)</td>
<td>0.04</td>
<td>NA</td>
<td>0.07</td>
</tr>
</tbody>
</table>

* The TJ and UJ are referenced to 1E-13 statistics (adding some margin with respect to the 1E-12 target BER)
Transmitter SSC

• The transmitter is required to support Spread-Spectrum-Clocking (SSC) in its steady-state operation

Example Transmitter Frequency During Steady-State

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX Freq Range</td>
<td>-300</td>
<td>300</td>
<td>ppm</td>
</tr>
<tr>
<td>Down-Spread Range</td>
<td>0.4</td>
<td>0.5</td>
<td>%</td>
</tr>
<tr>
<td>SSC Rate</td>
<td>30</td>
<td>33</td>
<td>KHz</td>
</tr>
<tr>
<td>SSC df/dt (ppm/µs)</td>
<td>1250</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSC Phase Deviation</td>
<td>2.5</td>
<td>22</td>
<td>ns p-p</td>
</tr>
</tbody>
</table>
Transmitter Clocking During Training

- Router Assembly may include up to 2 Re-timers on top of the Router IC
- Link training flow:
  - Initially, all Re-timers transmit local training data using local clock (without SSC) for training the entire link segments in parallel
  - When the receivers are trained, the Re-timers sequentially switch to forward the incoming data using the recovered clock
- Specifications are defined for constraining the output frequency variations during the transition from initial training to steady state operation

![Diagram of Transmitter Clocking During Training](image-url)
TX Frequency Variations During Training

### Table: Frequency Variations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial frequency range</td>
<td>–300</td>
<td>300</td>
<td>ppm</td>
</tr>
<tr>
<td>Frequency variation over 200ns window</td>
<td>1400</td>
<td></td>
<td>ppm</td>
</tr>
<tr>
<td>Frequency variation over 1000ns window</td>
<td>2200</td>
<td></td>
<td>ppm</td>
</tr>
</tbody>
</table>
Transmitter Return-Loss

- The Router Assembly Transmitter Return-Loss is measured at the near connector in TP2 reference point (at the output of a compliance plug fixture) referenced to a single-ended impedance of 42.5 Ω

TX Differential Return-Loss Mask

\[
\text{SDD22}(f) = \begin{cases} 
-8.5 & 0.05 < f_{\text{GHz}} \leq 3 \\
-3.5 + 8.3 \cdot \log_{10} \left( \frac{f_{\text{GHz}}}{12} \right) & 3 < f_{\text{GHz}} \leq 12 
\end{cases}
\]

TX Common-Mode Return-Loss Mask

\[
\text{SCC22}(f) = \begin{cases} 
-6 & 0.05 < f_{\text{GHz}} \leq 2.5 \\
-3 & 2.5 < f_{\text{GHz}} \leq 12 
\end{cases}
\]
Agenda

• Background
• Transmitter Specifications
• **Receiver Specifications**
• Testability
Introduction

- USB4™ data path employs combination of Forward Error Correction (FEC) and Pre-Coding for obtaining enhanced data integrity
- The FEC is based on low-complexity/low-latency Reed-Solomon RS(198,194) over GF(2^8) with two correctable errors per block
- The Pre-Coder is designed for converting bursts of consecutive bit-errors into two errors at the beginning and end of the burst, supported by the RS FEC
- As a result, high level of protection is obtained for long bursts of errors, which might be introduced by Decision-Feedback-Equalizers (DFE)
- Therefore, the coded BER performance is not affected by long bursts of errors but mainly by the uncoded BER and by secondary DFE effect of multi error bursts
USB4 Data-Path Example

- Bursts of errors are converted by the pre-coding into 2 errors at the beginning and end of the burst, supported by the RS FEC

<table>
<thead>
<tr>
<th>fec_enc_out[n]</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>tx[n]</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>rx[n]</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>fec_dec_in[n]</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
The Electrical performance is tested in stand-alone mode without applying Pre-Coding nor Forward-Error-Correction.

- The testing is based on PRBS patterns driven by pattern-generator.

The coded BER performance cannot be measured directly due to the large measurement window needed (several years…) and therefore validated indirectly based on electrical layer indicators.
Receiver Uncoded BER

- The Receiver shall operate at uncoded BER of 1E-12 with stressed signal applied.
- Two test setups are used for evaluating the receiver tolerance:
  - “Case 1” addressing installations with low Insertion-Loss
  - “Case 2” addressing installations with maximum Insertion-Loss

**Case 1:**

**Case 2:**
Uncoded BER Test Setup

- The Receiver tolerance test is performed with PRBS31 pattern and calibrated as following:

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Gen2</td>
<td>Case1 (TP3')</td>
<td>350</td>
<td>0.14</td>
<td>0.17</td>
<td>0.35</td>
</tr>
<tr>
<td></td>
<td>Case2 (TP3)</td>
<td>47</td>
<td>0.14</td>
<td>0.17</td>
<td>0.60</td>
</tr>
<tr>
<td>Gen3</td>
<td>Case1 (TP3')</td>
<td>350</td>
<td>0.14</td>
<td>0.17</td>
<td>0.38</td>
</tr>
<tr>
<td></td>
<td>Case2 (TP3)</td>
<td>49</td>
<td>0.14</td>
<td>0.17</td>
<td>0.60</td>
</tr>
</tbody>
</table>

- Each test is repeated for several different PJ frequencies, calibrated to 0.17UI pk-pk at the output of the jitter rejection mask.
Multi Error Burst Probability

• When a Receiver employs DFE with more than 1-tap, it shall take steps to limit the probability that a burst of errors is restarted after receiving one or more correct bits
  • When error burst ends, the 1st DFE tap is fed with correct data but errors still exist in the DFE pipeline

• The Burst Restart probability is characterized as following:
  • Initialize the test setup to “Case 2” configuration, with PJ frequency of 100MHz (PRBS31 pattern, neither FEC nor Pre-Coding is applied)
  • Increase the PJ magnitude to the point where uncoded BER of 1E−8 is observed
  • The Receiver under test shall trigger on random bit-errors and capture errors that follow (referenced as Error Captures)
    • Error Capture shall start with bit-error that is preceded by at least 32 consecutive bits without errors
  • The probability for obtaining Burst Restart events shall not exceed 5E−7 (i.e., one error burst restart per 2 million error captures on average)
Input Phase Variations During Training

- The Receiver shall track incoming frequency variations during the link training created by far-end Re-timer’s transmitter clock switching
  - No need for meeting BER<1E-12 but only to maintain the CDR tracking

The CTS specifies equivalent test using PJ tones with similar df/dt characteristics

![Graph showing frequency variations and time](image-url)
Receiver Return-Loss

- The Router Assembly Receiver Return-Loss is measured at the near connector in TP3’ reference point (at the input of a compliance plug fixture) referenced to a single-ended impedance of 42.5 Ω.

RX Differential Return-Loss Mask

\[
SDD11(f) = \begin{cases} 
-8.5 & 0.05 < f_{GHz} \leq 3 \\
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RX Common-Mode Return-Loss Mask

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-3 & 2.5 < f_{GHz} \leq 12 
\end{cases}
\]
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• Testability
Receiver Margining

• USB4™ defines method for characterizing the RX margin per each of the link’s instants
• The goal is to provide standard means for validating and debugging the link performance in production and in the field
  • The result is not used for determining compliancy but only for validation/debug
• All receivers need to support non-destructive voltage margining whereby a receiver sampler is offset from the nominal sampling position in the vertical axis
• Support for timing margining, whereby a receiver sampler is offset from the nominal sampling position in the horizontal dimension is optional
Receiver Margining Flow

- The Receiver Margining flow includes the following steps:
  - Configure the test parameters (lane, voltage/timing margin, BER target etc.)
  - Gradually decrease the vertical/horizontal margin and check for errors (monitor slicer errors in the non-destructive case, HEC/FEC errors in the destructive case)
  - Report margin result
- USB4™ port needs to support either “Software Margining Mode” or “Hardware Margining Mode” (may optionally support both):
  - Hardware Mode:
    The margining flow is mostly performed internally by the PHY hardware/firmware while external software is only triggering the test and reads the margin result
  - Software Mode:
    The margining flow is mostly conducted by external software controlling the PHY hardware which configures the vertical/horizontal offset

![Diagram of Receiver Margining Flow](image-url)
Time for Q&A