USB4™ Host Interface
Compliance Test Specification

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1.0	June 2020	First Release
1.1	September 2020	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 4, 2020.
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Contents

Introduction 5
Terminology 6
Assertions 7
Test Requirements 27
Hardware 27
System 27
Test Setups 28
AN_HOST_DFP1 28
EX_HOST_DFP1 28
Subroutines 29
Router Enumeration Procedure 29
Lane Bonding Initiation Procedure 29
Router Reset Procedure 29
Router Connect Procedure 29
Router Disconnect Procedure 30
Loopback Path Setup 30
Loopback Teardown 31
Test Descriptions 32
TD 12.001 Ring 0 General Test 32
TD 12.002 Frame Mode Test 34
TD 12.003 Raw Mode Test 36
TD 12.004 Single Data Buffer Test 38
TD 12.005 Interrupt Disable Test 39
TD 12.006 Ring Disabled Test 40
TD 12.007 Low Power Test 41
TD 12.008 Dropped Packet Test (Exerciser Required) 42
TD 12.009 Padding Test 43
TD 12.010 Multi-Path Test 44
TD 12.011 E2E Flow Control Test 46
TD 12.012 PCIe Programming Interface Test 47

Introduction

The tests defined in this test specification verify that a Host Router is compliant with Chapter 12 of the USB4 Specification.

Terminology

The following table describes the terms used in this document.

Analyzer	Test tool that captures and parses packets, transactions, ordered sets, etc.
Exerciser	Test tool that implements a USB4 Port with added functionality needed for compliance testing.
UUT	Unit Under Test. The Router that is being tested for compliance.
USB4 CV	Test tool that implements a Connection Manager with additional functionality to implement compliance tests.

Assertions

Compliance criteria are provided as a list of assertions that describe specific characteristics or behaviors that must be met. Each assertion provides a reference to the USB4 specification or other documents from which the assertion was derived. In addition, each assertion provides a reference to the specific test description(s) where the assertion is tested.

Each test assertion is formatted as follows:

Assertion #	Test #	Assertion Description

Assertion#: Unique identifier for each spec requirement. The identifier is in the form USB4_SPEC_SECTION_NUMBER#X, where X is a unique integer for a requirement in that section.

Assertion Description: Specific requirement from the specification

Test #: A label for a specific test description in this specification that tests this requirement. Test # can have one of the following values:

NT	This item is not explicitly tested in a test description. Items can be labeled NT for several reasons – including items that are not testable, not important to test for interoperability, or are indirectly tested by other operations performed by the compliance test.
X.X	This item is covered by the test described in test description X.X in this specification.
IOP	This assertion is verified by the USB4 Interoperability Test Suite.

Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

The following Table presents the USB4 Specification Chapter 12 asserts.

Assertion #	Test Name	Assertion Description
12 Host Interface		
12#1	IOP	A Host Router shall implement a single Host Interface Adapter Layer as defined in Sections 12.1 through 12.4 and Section 12.7.
12#2	IOP	A PCIe Host Router shall also implement the PCIe-specific Host Interface Adapter Layer functionality defined in Sections 12.5 and 12.6.
12#3	IOP	A non-PCIe Host Router shall implement functionality equivalent to that defined in Sections 12.5 and 12.6.
12#4	TD 12.010	A Host Interface Adapter Layer shall implement N Transmit Descriptor Rings and N Receive Descriptor Rings, where N >= 2.

Assertion #	Test Name	Assertion Description
12#5	IOP	A Host Router shall support operation with a Connection Manager that interfaces to the Router via Transmit Ring 0 and Receive Ring 0.
12#5	IOP	If a Host Router has an embedded Connection Manager, it shall implement a mechanism to disable the embedded Connection Manager.
12#6	NT	A Device Router shall not contain a Host Interface Adapter.
12.1 Descriptor Ring Modes		
12.1#1	TD 12.001	Transmit Ring 0 and Receive Ring 0 shall operate in Raw Mode only.
12.1#2	TD 12.010	All other Descriptor Rings shall support operation in both Raw Mode and Frame Mode.
12.1.1 DW, Byte, and Bit Order		
12.1.1#1	NT	A PCIe Host Interface Adapter Layer shall map the payload of a PCIe TLP into a Transport Layer Packet payload, Transmit Descriptor, or a Receive Descriptor in the following manner: For a Transport Layer Packet: Data Byte 0 in the PCIe TLP payload, shall be mapped to bits [31:24] of the first payload DW depicted in Figure 5-1. Data Byte 1 in the PCIe TLP payload, shall be mapped to bits [23:16] of the first payload DW depicted in Figure 5-1, and so on.
12.1.1#2	NT	A PCIe Host Interface Adapter Layer shall map the payload of a PCIe TLP into a Transport Layer Packet payload, Transmit Descriptor, or a Receive Descriptor in the following manner: For a Transmit Descriptor: Data Byte 0 in the PCIe TLP payload shall be mapped to bits [7:0] of the first DW of the Transmit Descriptor depicted in Figure 12-4. Data Byte 1 in the PCIe TLP payload shall be mapped to bits [15:8] of the first DW of the Transmit Descriptor depicted in Figure 12-4, and so on.
12.1.1#3	NT	A PCIe Host Interface Adapter Layer shall map the payload of a PCIe TLP into a Transport Layer Packet payload, Transmit Descriptor, or a Receive Descriptor in the following manner: For a Receive Descriptor: Data Byte 0 in the PCIe TLP payload shall be mapped to bits [7:0] of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6. Data Byte 1 in the PCIe TLP payload shall be mapped to bits [15:8] of the first DW of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6, and so on.
12.1.1#4	NT	A PCIe Host Interface Adapter Layer shall map the payload of a PCIe TLP into a Transport Layer Packet payload, Transmit Descriptor, or a Receive Descriptor in the following manner: Within each byte, bit[i] in the PCIe TLP payload shall be mapped to bit[i] in the corresponding byte of the Transmit Descriptor, Receive Descriptor, or Transport Layer Packet payload.

Assertion #	Test Name	Assertion Description
12.1.1#5	NT	Data Buffers, Transmit Descriptors, and Receive Descriptors shall be stored in host memory in the following manner: For a Data Buffer: the lowest-addressed byte of data shall be mapped to bits [31:24] of the first payload DW depicted in Figure 5-1. The following addressed byte shall be mapped to bits [23:16] of the first payload DW depicted in Figure 5-1, and so on.
12.1.1#6	NT	Data Buffers, Transmit Descriptors, and Receive Descriptors shall be stored in host memory in the following manner: For a Transmit Descriptor: the lowest-addressed byte of descriptor data in memory shall be mapped to bits [7:0] of the first DW of the Transmit Descriptor depicted in Figure 12-4. The following addressed byte shall be mapped to bits [15:8] of the first DW of the Transmit Descriptor depicted in Figure 12-4, and so on.
12.1.1#7	NT	Data Buffers, Transmit Descriptors, and Receive Descriptors shall be stored in host memory in the following manner: For a Receive Descriptor: the lowest-addressed byte of descriptor data in memory shall be mapped to bits [7:0] of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6. The following addressed byte shall be mapped to bits [15:8] of the first DW of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6, and so on.
12.1.1#8	NT	Data Buffers, Transmit Descriptors, and Receive Descriptors shall be stored in host memory in the following manner: Within each byte, bit[i] in host memory shall be mapped to bit[i] in the corresponding byte of the Data Buffer, Transmit Descriptor, or Receive Descriptor.
12.1.2 Raw Mode		
12.1.3 Frame Mode		
12.1.3#1	NT	A Frame shall be between 1 byte and 4096 bytes in length.
12.1.3#2	TD 12.002	For a Start of Frame Packet, the payload shall contain the first segment of a Frame.
12.1.3#3	TD 12.002	A Start of Frame Packet shall only be used when the Frame is segmented into more than one Tunneled Packet.
12.1.3#4	TD 12.002	For a Start of Frame Packet, the PDF value shall be taken from the *SOF PDF* field in the first Transmit Descriptor of the Frame.
12.1.3#5	TD 12.002	For a Middle of Frame Packet, the payload shall contain an intermediate segment of a Frame.
12.1.3#6	TD 12.002	A Middle of Frame Packet shall only be used when the Frame is segmented into more than two Tunneled Packet.

Assertion #	Test Name	Assertion Description
12.1.3#7	TD 12.002	A Middle of Frame packet shall have the PDF field set to 0h.
12.1.3#8	TD 12.002	For an End of Frame Packet, the Payload shall contain the last segment of a Frame when the Frame is segmented into more than one Tunneled Packet.
12.1.3#9	TD 12.002	For an End of Frame Packet, the payload shall contain the full Frame when the Frame is not segmented into more than one Tunneled Packet.
12.1.3#10	TD 12.002	For an End of Frame Packet, the payload shall include the complete 32-bit CRC.
12.1.3#11	TD 12.002	For an End of Frame Packet, PDF value shall be taken from the EOF PDF field in the last Transmit Descriptor of the Frame
12.2 End-to-End (E2E) Flow Control		
12.2#1	TD 12.001	A Host Interface Layer shall not use E2E flow control for Transmit Ring 0 or Receive Ring 0.
12.2.1 E2E Flow Control Packets		
12.2.1.1 E2E Credit Grant Packets		
12.2.1.1#1	TD 12.002 TD 12.003	An E2E Credit Grant Packet shall include the header in Table 12-2 followed by the payload defined in Table 12-3.
12.2.1.1#2	TD 12.002 TD 12.003	For a PCIe Host Interface Adapter Layer, the inserted *HopID* value in an E2E Credit Grant Packet header, shall be the same value as in the *Transmit E2E HopID* field
12.2.1.1#3	TD 12.002 TD 12.003	The ECC field in an E2E Credit Grant Packet shall be computed the same way as the *HEC* field of the Transport Layer Packet header.
12.2.1.1#4	TD 12.002 TD 12.003	The Credit Sync field in an E2E Credit Grant Packet shall be set to 0b.
12.2.1.2 E2E Credit Sync Packets		
12.2.1.2#1	TD 12.002 TD 12.003	An E2E Credit Sync Packet shall include the header in Table 12-4 followed by payload defined in Table 12-5.
12.2.1.2#2	TD 12.002 TD 12.003	The ECC field in an E2E Credit Sync Packet shall be computed the same way as the *HEC* field of the Transport Layer Packet header.
12.2.1.2#3	TD 12.002 TD 12.003	The Credit Sync field in an E2E Credit Sync Packet shall be set to 1b.

Assertion #	Test Name	Assertion Description
12.2.2 Flow Control Rules		
12.2.2.1 Credit Update		
12.2.2.1#1	NT	Credits shall be given in units of Receive Descriptors where one credit corresponds to one Receive Descriptor.
12.2.2.2 Credit Counter Synchronization		
12.2.2.3 Transmitting Host Interface Rules		
12.2.2.3#1	NT	If E2E flow control is disabled for the Transmit Descriptor Ring, the Host Interface Adapter Layer shall not require any credits to be available before transmitting a Tunneled Packet from this Transmit Descriptor Ring
12.2.2.3#2	TD 12.011	If E2E flow control is enabled for the Transmit Descriptor Ring and the Ring is in Raw Mode, the Host Interface Adapter Layer shall not transmit a Tunneled Packet unless at least one credit for the corresponding Transmit Descriptor Ring is available
12.2.2.3#3	TD 12.011	If E2E flow control is enabled for the Transmit Descriptor Ring and the Ring is in Frame Mode, the Host Interface Adapter Layer shall not transmit a Tunneled Packet unless at least one credit for the corresponding Transmit Descriptor is available for the Frame
12.2.2.3#4	TD 12.006 TD 12.007	A Transmitting Host Interface Adapter Layer shall not send E2E Credit Sync Packets for a Transmit Descriptor Ring with E2E flow control disabled or when the egress Link is in a low-power state.
12.2.2.3#5	NT	When a Transmitting Host Interface Adapter Layer receives a Credit Grant Packet, it shall verify the ECC field value in the Credit Grant Record.
12.2.2.3#6	NT	The Adapter Layer shall correct any single-bit errors.
12.2.2.3#7	NT	After correcting an error, the Adapter Layer shall continue on as if the error had never occurred.
12.2.2.3#8	NT	If an uncorrectable error is detected, the Credit Grant Packet shall be dropped.
12.2.2.4 Receiving Host Interface Rules		
12.2.2.4#1	NT	A Receiving Host Interface Adapter Layer shall track credits individually for each Receive Descriptor Ring enabled with E2E flow control.
12.2.2.4#2	TD 12.002 TD 12.003	A Receiving Host Interface Adapter Layer shall send an E2E Credit Grant Packet every $T_{E2ERATE}$ for each Receive Descriptor Ring with E2E flow control enabled.

Assertion #	Test Name	Assertion Description
12.2.2.4#3	NT	It shall also send an E2E Credit Grant Packet each time additional Receive Descriptors are made available to the Receive Descriptor Ring in Host Memory.
12.2.2.4#4	NT	An E2E Credit Grant Packet shall carry the most recent credit count for the Descriptor Ring.
12.2.2.4#5	TD 12.006	A Host Interface Adapter Layer shall not send E2E Credit Grant Packets for a Receive Descriptor Ring with E2E flow control disabled.
12.2.2.4#6	TD 12.007	If the Adapter indicated by the *Transmit E2E HopID* field for a Receive Descriptor Ring is in a low power state, a Host Interface Adapter Layer shall only send an E2E Credit Grant Packet for the Receive Descriptor Ring when the credit count for the Receive Ring changes.
12.2.2.4#7	TD 12.002 TD 12.003	The number of available credits advertised for a Receive Descriptor Ring shall not exceed 8192.
12.2.2.4#8	NT	When a Receiving Host Interface Adapter Layer receives a Credit Sync Packet, it shall verify the ECC field value in the Credit Sync Packet payload.
12.2.2.4#9	NT	The Adapter Layer shall correct any single-bit errors.
12.2.2.4#10	NT	After correcting an error, the Adapter Layer shall continue on as if the error had never occurred.
12.2.2.4#11	NT	If an uncorrectable error is detected, the Credit Sync Packet shall be dropped.
12.3 Transmit Interface		
12.3#1	TD 12.010	A Host Interface Adapter Layer shall implement a Transmit Descriptor Ring for each supported Path.
12.3.1 Transmit Descriptor Structure		
12.3.1#1	NT	The Host Interface Adapter Layer shall fetch Transmit Descriptors from Host Memory.
12.3.1#2	NT	A Transmit Descriptor shall have the format depicted in Figure 12-4 and listed in Table 12-6.
12.3.1#3	NT	The least significant 2-bits of the *Address Low* field shall be 00b.
12.3.1#4	IOP	An Adapter Layer shall not modify the Address Low Field.
12.3.1#5	IOP	An Adapter Layer shall not modify the Address High Field.
12.3.1#6	NT	A value of 0 in the Data Length field indicates that 4096 bytes shall be fetched.

Assertion #	Test Name	Assertion Description
12.3.1#7	NT	An Adapter Layer shall not modify the Data Length Field.
12.3.1#8	NT	In Raw Mode, the EOF PDF field shall be set to a value between 0h and Eh.
12.3.1#9	NT	In Frame Mode, if the Transmit Descriptor is the last (or only) Transmit Descriptor for a Frame, the EOF PDF field shall be set to a value between 1h and Eh. Else, shall be set to 0h.
12.3.1#10	TD 12.001 TD 12.002 TD 12.003	An Adapter Layer shall not modify the EOF PDF field.
12.3.1#11	TD 12.003	In Raw Mode, a Router shall ignore the SOF PDF field.
12.3.1#12	NT	In Frame Mode, if the Transmit Descriptor is the first (or only) Transmit Descriptor for a Frame, the SOF PDF field shall be set to a value between 1h and Eh. Else, shall be set to 0h
12.3.1#13	NT	The SOF PDF shall be different than the EOF PDF for the Frame.
12.3.1#14	TD 12.001 TD 12.002 TD 12.003	An Adapter Layer shall not modify the SOF PDF field.
12.3.1#15	TD 12.001 TD 12.002 TD 12.003	If the *Request Status* bit in a Transmit Descriptor is set to 1b, the Host Interface Adapter Layer shall set the Descriptor Done bit to 1b after the last byte of the Data Buffer is sent to the Transport Layer.
12.3.1#16	NT	If the *Request Status* bit in a Transmit Descriptor is set to 0b, the Host Interface Adapter Layer shall not write to the Descriptor Done bit.
12.3.1#17	TD 12.001 TD 12.002 TD 12.003	An Adapter Layer shall not modify the Request Status field.
12.3.1#18	TD 12.001 TD 12.002 TD 12.003	If the Interrupt Enable bit is set to 1b, then the Host Interface Adapter Layer shall issue an interrupt indicating the completion of the Data Buffer after setting the *DD* bit to 1b.
12.3.1#19	TD 12.001 TD 12.002 TD 12.003	An Adapter Layer shall not modify the Interrupt Enable field.
12.3.1#20	IOP	An Adapter Layer shall not modify the Offset field.

Assertion #	Test Name	Assertion Description
12.3.2 Transmit Flow		
12.3.2#1	NT	A Host Interface Adapter Layer shall only process a Transmit Descriptor Ring when both the Transmit Descriptor Ring is enabled and at least one Transmit Descriptor is pending.
12.3.2.1 Frame Mode		
12.3.2.1#1	NT	A Frame shall reside in one or more Data Buffers.
12.3.2.1#2	TD 12.004	A Data Buffer shall not contain data from more than one Frame at a time.
12.3.2.1#3	IOP	A Host Interface Adapter Layer shall segment a Frame into one or more Tunneled Packets as follows: The Host Interface Adapter takes the Data Buffers of one or more Transmit Descriptors to form a Tunneled Packet payload. The Host Interface Adapter Layer prepends a Transport Layer Packet Header to the payload to generate a Tunneled Packet
12.3.2.1#4	NT	A Host Interface Adapter Layer shall segment a Frame into one or more Tunneled Packets as follows: If a Tunneled Packet contains multiple Data Buffers as payload, all Data Buffers shall contain data from the same Frame.
12.3.2.1#5	TD 12.002	A Host Interface Adapter Layer shall segment a Frame into one or more Tunneled Packets as follows: If a Frame is sent in a single Tunneled Packet, the Tunneled Packet shall be of type *End of Frame.*
12.3.2.1#6	TD 12.002	A Host Interface Adapter Layer shall segment a Frame into one or more Tunneled Packets as follows: If a Frame is sent in multiple Tunneled Packets: The Tunneled Packet containing the first segment of the Frame shall be of type Start of Frame and shall be sent first.
12.3.2.1#7	TD 12.002	A Host Interface Adapter Layer shall segment a Frame into one or more Tunneled Packets as follows: If a Frame is sent in multiple Tunneled Packets: Any following Tunneled Packets other than the last Tunneled Packet shall be of type Middle of Frame.
12.3.2.1#8	TD 12.002	A Host Interface Adapter Layer shall segment a Frame into one or more Tunneled Packets as follows: If a Frame is sent in multiple Tunneled Packets: The Tunneled Packet containing the last segment of the Frame shall be of type End of Frame and shall be sent last.
12.3.2.1#9	TD 12.002	The Router shall append a 32-bit CRC to each Frame.
12.3.2.1#10	NT	The CRC shall cover the entire Frame.
12.3.2.1#11	TD 12.002	The Router shall calculate the CRC as defined in Table 6-1.
12.3.2.1#12	TD 12.002	The CRC shall be calculated in increasing DW order. Within each DW, CRC shall be calculated from bit[31] to bit[0].

Assertion #	Test Name	Assertion Description
12.3.2.1#13	TD 12.002	The CRC shall be placed in the payload of an *End of Frame* Tunneled Packet immediately after the Frame bytes.
12.3.2.1#14	NT	Bits [7:0] of the calculated CRC shall be placed in bits [31:24] of the CRC field.
12.3.2.1#15	NT	Bits [15:8] of the calculated CRC shall be placed in bits [23:16] of the CRC field.
12.3.2.1#16	NT	Bits [23:16] of the calculated CRC shall be placed in bits [15:8] of the CRC field.
12.3.2.1#17	NT	Bits [31:24] of the calculated CRC shall be placed in bits [7:0] of the CRC field.
12.3.2.1#18	TD 12.009	If padding is added to any Tunneled Packets, it shall be added after the Frame CRC is calculated and the Frame and CRC are segmented into Tunneled Packet payload.
12.3.2.1#19	TD 12.002	The Router shall set the *HopID* value of each Tunneled Packet to n, where n is the HopID associated with the Transmit Descriptor Ring.
12.3.2.1#20	TD 12.002	If the *RS* bit in the Transmit Descriptor is set to 1b, a Host Interface Adapter Layer shall do the following after the last byte of the Data Buffer is sent to the Transport Layer: Set the DD bit to 1b in the Transmit Descriptor in Host Memory.
12.3.2.1#21	TD 12.002	If the *RS* bit in the Transmit Descriptor is set to 1b, a Host Interface Adapter Layer shall do the following after the last byte of the Data Buffer is sent to the Transport Layer: If the IE bit is set to 1b, issue an interrupt indicating the completion of the Data Buffer.
12.3.2.1#22	NT	After fetching a Data Buffer from Host Memory, a PCIe Host Interface Adapter Layer shall increment the Consumer Index for the Transmit Descriptor Ring by 1 (with wraparound to 0 when Consumer Index = Ring Size).
12.3.2.2 Raw Mode		
12.3.2.2#1	NT	A Host Interface Adapter Layer shall fetch the payload for a Transport Layer Packet from the Data Buffer referenced in the next available Transmit Descriptor.
12.3.2.2#2	NT	The Host Interface Adapter Layer shall prepend the Transport Layer Packet Header to the payload fetched from the Data Buffer.
12.3.2.2#3	TD 12.003	The *PDF* field in the Transport Layer Packet shall match the *EOF PDF* field in the Transmit Descriptor.

Assertion #	Test Name	Assertion Description
12.3.2.2#4	TD 12.001 TD 12.003	If the *RS* bit in the Transmit Descriptor is set to 1b, a Host Interface Adapter Layer shall do the following after the last byte of the Data Buffer is sent to the Transport Layer: Set the DD bit to 1b in the Transmit Descriptor in Host Memory.
12.3.2.2#5	TD 12.001 TD 12.003	If the *RS* bit in the Transmit Descriptor is set to 1b, a Host Interface Adapter Layer shall do the following after the last byte of the Data Buffer is sent to the Transport Layer: If the IE bit is set to 1b, issue an interrupt indicating the completion of the Data Buffer.
12.3.2.2#6	NT	After fetching a Data Buffer from Host Memory, a PCIe Host Interface Adapter Layer shall increment the *Consumer Index* for the Transmit Descriptor Ring by 1 (with wraparound to 0 when *Consumer Index = Ring Size*).
12.4 Receive Interface		
12.4#1	TD 12.010	A Host Interface Adapter Layer shall implement a Receive Descriptor Ring for each supported Path.
12.4#2	TD 12.010	Each Receive Descriptor Ring shall be allocated a different HopID value.
12.4.1 Receive Descriptor Structure		
12.4.1#1	NT	A Receive Descriptor that is fetched from Host Memory shall have the format depicted in Figure 12-5 and listed in Table 12-7.
12.4.1#2	NT	A Receive Descriptor that is posted to Host Memory shall have the format depicted in Figure 12-6 and listed in Table 12-8.
12.4.1#3	NT	The Address Low field shall contain the same value as posted by the Host.
12.4.1#4	NT	The Address High field shall contain the same value as posted by the Host.
12.4.1#5	TD 12.001 TD 12.003	When in Raw Mode, the EOF PDF field shall be set to the value in the *PDF* field of the Transport Layer Packet
12.4.1#6	TD 12.002	When in Frame Mode, the EOF PDF field shall be set to the value in the *PDF* field of the *End of Frame* Transport Layer Packet carrying the last (or only) segment of the Frame.
12.4.1#7	NT	When in Raw Mode, the SOF PDF field shall be set to 0h.
12.4.1#8	NT	When in Frame Mode, the SOF PDF field shall be set to 0h if Frame is sent in a single Tunneled Packet.

Assertion #	Test Name	Assertion Description
12.4.1#9	TD 12.002	Else, when in Frame Mode, the SOF PDF field shall be set to the value in the *PDF* field of the *Start of Frame* Transport Layer Packet carrying the first segment of the Frame.
12.4.1#10	TD 12.001 TD 12.003	When in Raw Mode, the CRC Error field shall be set to 0b.
12.4.1#11	TD 12.008	When in Frame Mode, the CRC Error field shall be set to 1b if the CRC check failed for the reassembled Frame. Otherwise, this bit shall be 0b.
12.4.1#12	TD 12.001 TD 12.002 TD 12.003	If the *RS* bit is set to 1b when the Receive Descriptor is read from Host Memory, the Descriptor Done bit shall be set to 1b after the last byte has been written to the Data Buffer.
12.4.1#13	NT	When in Raw Mode, the Buffer Overflow bit shall be set to 1b if the size of the received Tunneled Packet exceeds the available space in the Data Buffer.
12.4.1#14	TD 12.001 TD 12.003	When in Raw Mode, the Buffer Overflow bit shall be set to 0b if the size of the received Tunneled Packet does not exceed the available space in the Data Buffer.
12.4.1#15	NT	When in Frame Mode, the Buffer Overflow bit shall be set to 1b if the size of the reassembled Frame exceeds the available space in the Data Buffer.
12.4.1#16	TD 12.002	When in Frame Mode, the Buffer Overflow bit shall be set to 0b if the size of the reassembled Frame does not exceeds the available space in the Data Buffer.
12.4.1#17	TD 12.001 TD 12.002 TD 12.003	The Interrupt Enable field shall contain the same value as posted by the Host.
12.4.1#18	NT	The Offset field shall contain the same value as posted by the Host.
12.4.2 Receive Flow		
12.4.2#1	NT	When a Host Interface Adapter Layer receives a Transport Layer Packet from the Transport Layer it shall: 1. Select the Receive Descriptor Ring corresponding to the *HopID* field in the received Transport Layer Packet.
12.4.2#2	TD 12.006	When a Host Interface Adapter Layer receives a Transport Layer from the Transport Layer it shall: 2. If the *Valid* bit for the Receive Descriptor Ring is set to 0b, discard the Transport Layer Packet.

Assertion #	Test Name	Assertion Description
12.4.2#3	IOP	When a Host Interface Adapter Layer receives a Transport Layer from the Transport Layer it shall: 3. Else if the Receive Descriptor Ring operates in Frame Mode, process the Transport Layer according to Section 12.4.2.1.
12.4.2#4	IOP	When a Host Interface Adapter Layer receives a Transport Layer from the Transport Layer it shall: 4. Else if the Receive Descriptor Ring operates in Raw Mode, process the Transport Layer according to Section 12.4.2.2.
12.4.2.1 Frame Mode		
12.4.2.1#1	TD 12.002	A Host Interface Adapter Layer in Frame Mode shall process Tunneled Packets received for a Receive Descriptor Ring as follows: All Tunneled Packets for a Frame shall be posted into the same Data Buffer.
12.4.2.1#2	NT	A Host Interface Adapter Layer in Frame Mode shall process Tunneled Packets received for a Receive Descriptor Ring as follows: A Frame shall be posted using the next available Receive Descriptor.
12.4.2.1#3	NT	A Host Interface Adapter Layer in Frame Mode shall process Tunneled Packets received for a Receive Descriptor Ring as follows: If a Receive Descriptor is not available in Host Memory, discard the packet.
12.4.2.1#4	NT	A Host Interface Adapter Layer in Frame Mode shall process Tunneled Packets received for a Receive Descriptor Ring as follows: If the size of the packet payload exceeds the remaining available size of the Data Buffer: Optionally write to the Data Buffer the part of the packet that fits into the Data Buffer. Any further received Tunneled Packets that belong to the same Frame shall be dropped and shall not be written to Host Memory.
12.4.2.1#5	NT	A Host Interface Adapter Layer in Frame Mode shall process Tunneled Packets received for a Receive Descriptor Ring as follows: If the size of the packet payload exceeds the remaining available size of the Data Buffer: Set the Buffer Overflow bit in the Receive Descriptor to 1b.
12.4.2.1#6	NT	A Host Interface Adapter Layer in Frame Mode shall process Tunneled Packets received for a Receive Descriptor Ring as follows: If the size of the packet payload exceeds the remaining available size of the Data Buffer: The CRC Error bit, the SOF PDF field, and the EOF PDF field shall represent the Frame as received, including packets not written to Host Memory.
12.4.2.1#7	TD 12.008	A Host Interface Adapter Layer in Frame Mode shall process Tunneled Packets received for a Receive Descriptor Ring as follows: If a packet is a *Middle of Frame* packet and either no *Start of Frame* packet has been received for the Frame or an *End of Frame* packet was previously received for the Frame: Post packet payload to a Data Buffer using the next available Receive Descriptor.

Assertion #	Test Name	Assertion Description
12.4.2.1#8	TD 12.008	A Host Interface Adapter Layer in Frame Mode shall process Tunneled Packets received for a Receive Descriptor Ring as follows: If a packet is a *Middle of Frame* packet and either no *Start of Frame* packet has been received for the Frame or an *End of Frame* packet was previously received for the Frame: Set the *SOF PDF* field to 0b and the *CRC Error* bit to 1b in the Receive Descriptor once the Receive Descriptor is written back to Host Memory
12.4.2.1#9	TD 12.008	A Host Interface Adapter Layer in Frame Mode shall process Tunneled Packets received for a Receive Descriptor Ring as follows: If a packet is an *End of Frame* packet and either no *Start of Frame* packet has been received for the Frame or an *End of Frame* packet was previously received for the Frame: Post packet payload to a Data Buffer using the next available Receive Descriptor.
12.4.2.1#10	TD 12.008	A Host Interface Adapter Layer in Frame Mode shall process Tunneled Packets received for a Receive Descriptor Ring as follows: If a packet is an *End of Frame* packet and either no *Start of Frame* packet has been received for the Frame or an *End of Frame* packet was previously received for the Frame: Set the *SOF PDF* field to 0b.
12.4.2.1#11	TD 12.008	A Host Interface Adapter Layer in Frame Mode shall process Tunneled Packets received for a Receive Descriptor Ring as follows: If a packet is a Start of Frame packet and the previous packet received was a Start of Frame packet or a Middle of Frame packet, post the packet to the beginning of the Data Buffer (overwriting any previous packets).
12.4.2.1#12	TD 12.002	Packet payload for a Frame shall be posted in the order received.
12.4.2.1#13	TD 12.002	If the Packet payload is from a Start of Frame packet, it shall be posted at the offset in the Offset field of the Receive Descriptor.
12.4.2.1#14	TD 12.002	Otherwise, payload shall be posted immediately after the previously received payload for the Frame.
12.4.2.1#15	NT	The 32-bit CRC received with a Frame shall not be posted to the Data Buffer.
12.4.2.1#16	TD 12.002	If a packet is an *End of Frame* packet: If the RS bit in the Receive Descriptor is set to 1b: Write back the Receive Descriptor with the contents defined in Table 12-8.
12.4.2.1#17	TD 12.002	If a packet is an *End of Frame* packet: If the RS bit in the Receive Descriptor is set to 1b: If the IE bit is set to 1b, issue an interrupt indicating the completion of the Data Buffer.
12.4.2.1#18	NT	If a packet is an *End of Frame* packet: For a PCIe Host Interface Adapter Layer, increment the Producer Index by 1 with wraparound to 0 when Producer Index = Ring Size.

Assertion #	Test Name	Assertion Description
12.4.2.2 Raw Mode		
12.4.2.2#1	TD 12.004	A Host Interface Adapter Layer in Raw Mode shall process Transport Layer Packets received for a Receive Descriptor Ring as follows: Each Transport Layer Packet payload shall be posted into a separate, single, Data Buffer.
12.4.2.2#2	TD 12.003	A Host Interface Adapter Layer in Raw Mode shall process Transport Layer Packets received for a Receive Descriptor Ring as follows: A Transport Layer Packet shall be posted at the offset in the *Offset* field of the Receive Descriptor.
12.4.2.2#3	NT	A Host Interface Adapter Layer in Raw Mode shall process Transport Layer Packets received for a Receive Descriptor Ring as follows: A Transport Layer Packet shall be posted using the next available Receive Descriptor.
12.4.2.2#4	NT	A Host Interface Adapter Layer in Raw Mode shall process Transport Layer Packets received for a Receive Descriptor Ring as follows: If the size of payload of the received Transport Layer Packet exceeds the available size of the Data Buffer: Set the *Buffer Overflow* bit in the Receive Descriptor to 1b.
12.4.2.2#5	NT	A Host Interface Adapter Layer in Raw Mode shall process Transport Layer Packets received for a Receive Descriptor Ring as follows: If the size of payload of the received Transport Layer Packet exceeds the available size of the Data Buffer: If the *RS* bit in the Receive Descriptor is set to 1b, write back the Receive Descriptor with the contents defined in Table 12-8.
12.4.2.2#6	NT	A Host Interface Adapter Layer in Raw Mode shall process Transport Layer Packets received for a Receive Descriptor Ring as follows: If the size of payload of the received Transport Layer Packet exceeds the available size of the Data Buffer: If the *IE* bit is set to 1b, issue an interrupt indicating the completion of the Data Buffer.
12.4.2.2#7	NT	A Host Interface Adapter Layer in Raw Mode shall process Transport Layer Packets received for a Receive Descriptor Ring as follows: If the size of payload of the received Transport Layer Packet exceeds the available size of the Data Buffer: For a PCIe Host Interface Adapter Layer, increment the *Producer Index* by 1 with wraparound to 0 when *Producer Index = Ring Size.*
12.4.2.2#8	TD 12.001 TD 12.003	A Host Interface Adapter Layer in Raw Mode shall process Transport Layer Packets received for a Receive Descriptor Ring as follows: When posting packet payload to a Data Buffer: If the *RS* bit in the Receive Descriptor is set to 1b, write back the Receive Descriptor with the contents defined in Table 12-8.

Assertion #	Test Name	Assertion Description
12.4.2.2#9	TD 12.001 TD 12.003	A Host Interface Adapter Layer in Raw Mode shall process Transport Layer Packets received for a Receive Descriptor Ring as follows: When posting packet payload to a Data Buffer: If the *IE* bit is set to 1b, issue an interrupt indicating the completion of the Data Buffer.
12.4.2.2#10	NT	A Host Interface Adapter Layer in Raw Mode shall process Transport Layer Packets received for a Receive Descriptor Ring as follows: When posting packet payload to a Data Buffer: For a PCIe Host Interface Adapter Layer, increment the *Producer Index* by 1 with wraparound to 0 when *Producer Index = Ring Size*.
12.5 Interrupts		
12.5#1	NT	A PCIe Host Router shall support INTx Interrupt Signaling and Message Signaled Interrupt (MSI and MSI-X).
12.5.1 Interrupt Causes		
12.5.1#1	NT	If the *Interrupt Enable* bit is set to 1b in a Transmit Descriptor, then after the Host Interface Adapter Layer writes back to that Transmit Descriptor, it shall set to 1b the *Transmit Data Buffer Interrupt* bit in the Interrupt Status Registers that corresponds to this Transmit Descriptor Ring.
12.5.1#2	NT	If the *Interrupt Enable* bit is set to 1b in a Receive Descriptor, then after the Host Interface Adapter Layer has written back a Receive Descriptor, it shall set to 1b the *Receive Data Buffer Interrupt* bit in the Interrupt Status Registers that corresponds to this Receive Descriptor Ring.
12.5.1#3	NT	The Host Interface Adapter Layer shall monitor how many unused Receive Descriptors are in each Receive Descriptor Ring.
12.5.1#4	NT	For each Receive Descriptor Ring, a Host Interface Adapter Layer shall set to 1b the corresponding bit in the *Receive Ring Vacancy Status* register to 1b when: The *Receive Ring Vacancy Control* field for that Receive Descriptor Ring is zero and Receive Descriptor Ring has no unused Receive Descriptors.
12.5.1#5	NT	For each Receive Descriptor Ring, a Host Interface Adapter Layer shall set to 1b the corresponding bit in the *Receive Ring Vacancy Status* register to 1b when: or The number of unused Receive Descriptors for a Receive Descriptor Ring falls below the value indicated by the *Receive Ring Vacancy Control* field for that Receive Descriptor Ring.
12.5.1#6	NT	If a *Receive Ring Vacancy Status* bit is set to 1b, the Host Interface Adapter Layer shall set the corresponding bit to 1b in the Interrupt Status Registers.

Assertion #	Test Name	Assertion Description
12.5.2 Interrupt Masks		
12.5.2#1	NT	When the Host Interface Adapter Layer sets a bit in the *Interrupt Status* Registers to 1b, it shall initiate an interrupt request to the interrupt moderation function if the corresponding bit in the *Interrupt Mask* Registers is set to 1b.
12.5.2#2	TD 12.001 TD 12.005	It shall not initiate an interrupt if the corresponding bit in the *Interrupt Mask* Registers is set to 0b.
12.5.3 Interrupt Vectors		
12.5.3#1	NT	In MSI mode of operation, the Host Interface Adapter Layer shall request a single interrupt vector.
12.5.3#2	NT	In MSI-X mode of operation, the Host Interface Adapter Layer shall support 16 interrupt vectors.
12.5.3#3	NT	When a bit is set to 1b in the *Interrupt Status* Registers and the corresponding bit in the *Interrupt Mask* Registers is set to 1b, the Host Interface Adapter Layer shall issue the interrupt vector associated with the interrupt cause in the *Interrupt Vector Allocation* Registers (IVAR).
12.5.4 Interrupt Moderation		
12.5.4#1	NT	If the Interval field in the ITR[i] register (i=0,...,15) is set to 0, an interrupt of interrupt vector i shall not be moderated.
12.5.4#2	NT	An interrupt message shall be sent when the bit in the Interrupt Status Registers that is associated with interrupt vector i is set to 1b.
12.5.4#3	NT	If the Interval field in the ITR[i] register (i=0,...,15) is set to a non-zero value, an interrupt message shall be sent according to the flow defined in Figure 12-7.
12.6 Programming Interface		
12.6#1	NT	A PCIe Host Interface Adapter Layer shall support the programming interface defined in this section.
12.6#2	NT	The Host Interface Adapter Layer shall discard any write request to a non-implemented register within the memory BAR.
12.6#3	NT	The Host Interface Adapter Layer shall support aligned 32-bit accesses (with all Byte Enables set to 1b) to the Memory BAR.
12.6#4	NT	The Host Interface Adapter Layer shall expose a value of 0C 03 40h in the Class Code field of the PCI Configuration Space.

Assertion #	Test Name	Assertion Description
12.6.1 Access Types		
12.6.1#1	NT	**Read/Write.** A field with this access type shall be capable of both read and write operations. The value read from this field shall reflect the last value written to it unless the field was reset in the interim.
12.6.1#2	NT	**Read/Write Status.** A field with this access type shall be capable of both read and write operations.
12.6.1#3	NT	**Read Only.** A write to a field with this access type shall have no effect. A read shall return a meaningful value.
12.6.1#4	NT	**Read Clear.** A field with this access type shall be cleared to 0 after it is read. A write to a field with this attribute shall have no effect on its value.
12.6.1#5	NT	**Write Clear.** A field with this access type shall be cleared to 0 after it is written to. A read shall return a meaningful value.
12.6.1#6	NT	**Read/Write Self Clearing.** When set to 1b a field with this access type causes an action to be initiated. A field with this attribute shall read as 0b after the action is complete.
12.6.1#7	NT	**Reserved.** Reserved for future implementation. A write to this field shall have no effect. A read shall return 0.
12.6.1#8	NT	**Reserved and Zero.** Reserved for future implementation. A read shall return 0.
12.6.1#9	NT	**Write Only**. A field with this access type shall be capable of write operations. Reading the field returns a vendor-defined value.
12.6.2 Registers Summary		
12.6.3 Register Description		
12.6.3.1 Host Interface Control		
12.6.3.1.1 Host Interface Capabilities		
12.6.3.1.2 Host Interface Reset		
12.6.3.1.2#1	TD 12.012	When the RST bit in the Host Interface Capabilities Register is set to 1b, shall reset the Host Interface registers and the E2E flow control counters to their default values.
12.6.3.1.2#2	TD 12.012	The Host Interface Adapter Layer shall complete the reset within tHIReset time.

Assertion #	Test Name	Assertion Description
12.6.3.1.3 Host Interface Control		
12.6.3.1.4 Host Interface CL1 Enable		
12.6.3.1.5 Host Interface CL2 Enable		
12.6.3.2 Transmit Descriptor Rings		
12.6.3.2#1	NT	The Base Address is aligned to 16 bytes, so that the least significant 4-bits of the *Ring Base Address Low* field shall be 0h.
12.6.3.2.1 Base Address Low		
12.6.3.2.2 Base Address High		
12.6.3.2.3 Producer and Consumer Indexes		
12.6.3.2.4 Ring Size		
12.6.3.2.4#1	NT	Ring Size shall not exceed 4096 descriptors.
12.6.3.2.5 Ring Control		
12.6.3.2.5#1	NT	Raw Mode (RAW). When set to 0b, the Descriptor Ring shall operate in Frame Mode.
12.6.3.2.5#2	NT	Raw Mode (RAW). When set to 1b, the Descriptor Ring shall operate in Raw Mode.
12.6.3.3 Receive Descriptor Rings		
12.6.3.3.1 Base Address Low		
12.6.3.3.1#1	NT	The Base Address is aligned to 16 bytes, so that the least significant 4-bits of the *Ring Base Address Low* field shall be 0.
12.6.3.3.2 Base Address High		
12.6.3.3.3 Producer and Consumer Indexes		
12.6.3.3.4 Ring and Buffer Size		
12.6.3.3.4#1	NT	Ring Size shall not exceed 4096 descriptors.
12.6.3.3.4#2	NT	The Host Interface Adapter Layer shall not write to the *Data Length* field in a Receive Descriptor a value larger than *Data Buffer Size* minus the value of the *Offset* field provided by the Host in the Receive Descriptor.

Assertion #	Test Name	Assertion Description
12.6.3.3.5 Ring Control		
12.6.3.3.5#1	NT	Raw Mode (RAW). When set to 0b, the Descriptor Ring shall operate in Frame Mode.
12.6.3.3.5#2	NT	Raw Mode (RAW). When set to 1b, the Descriptor Ring shall operate in Raw Mode.
12.6.3.3.6 PDF Bit Masks		
12.6.3.3.6#1	NT	The EOF PDF Bitmask field specifies the *PDF* values that shall be interpreted as *End of Frame PDF*.
12.6.3.3.6#2	NT	If the *Raw Mode* bit is set to 0b, then the Host Interface Adapter Layer shall treat a received Transport Layer Packet as an *End of Frame* packet if bit i (i=1,...,14) in the EOF PDF Bitmask field is set to 1b, where i is the *PDF* value of the received Transport Layer Packet.
12.6.3.3.6#3	NT	If the *Raw Mode* bit is set to 1b, the EOF PDF Bitmask field shall have no effect.
12.6.3.3.6#4	NT	The SOF PDF Bitmask field specifies the *PDF* values that shall be interpreted as *Start of Frame PDF*.
12.6.3.3.6#5	NT	If the *Raw Mode* bit is set to 0b, then the Host Interface Adapter Layer shall treat a received Transport Layer Packet as a *Start of Frame* Packet if bit i (i=17,...,30) in the SOF PDF Bitmask field is set to 1b, where (i-16) is the *PDF* value of the received Transport Layer Packet.
12.6.3.3.6#6	NT	If the Raw Mode bit is set to 1b, the SOF PDF Bitmask field shall have no effect.
12.6.3.4 Interrupts		
12.6.3.4.1 Interrupt Status		
12.6.3.4.1#1	NT	When a bit is set to 1b in the Interrupt Status Clear Registers, the corresponding bit in the Interrupt Status Registers shall be set to 0b.
12.6.3.4.1#2	NT	When a bit is set to 1b in the Interrupt Status Set Registers, the corresponding bit in the Interrupt Status Registers shall be set to 1b.

Assertion #	Test Name	Assertion Description
12.6.3.4.2 Interrupt Status Clear		
12.6.3.4.3 Interrupt Status Set		
12.6.3.4.4 Interrupt Mask		
12.6.3.4.5 Interrupt Mask Clear		
12.6.3.4.6 Interrupt Mask Set		
12.6.3.4.7 Interrupt Throttling Rate (ITR)		
12.6.3.4.8 Interrupt Vector Allocation (IVAR)		
12.6.3.4.9 Receive Ring Vacancy Control		
12.6.3.4.10 Receive Ring Vacancy Status		
12.7 Timing Parameters		

Test Requirements

Hardware

Vendor provides Host Router in a reference system for testing:

- Reference System exposes one USB Type-C connector for each USB4 Port on the Host Router
- Host Router must be PCIe-based

System

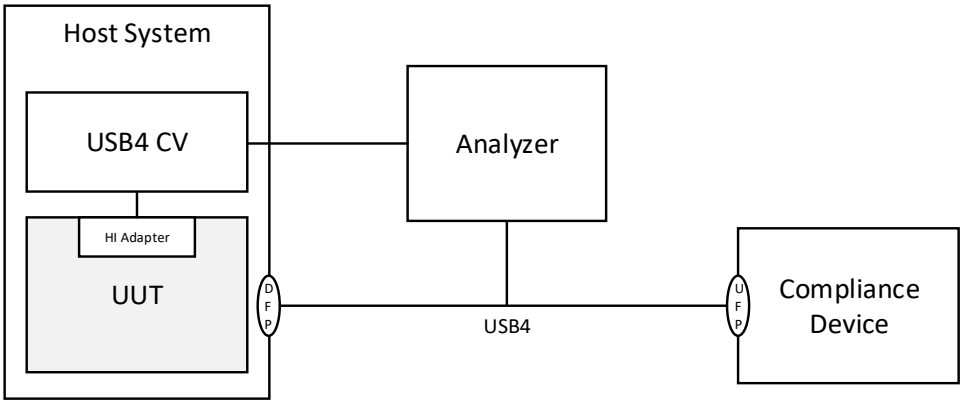
Reference system with Host Router must be x64-based and run Windows 10 with USB4 CV installed.

Test Setups

AN_HOST_DFP1

Description:

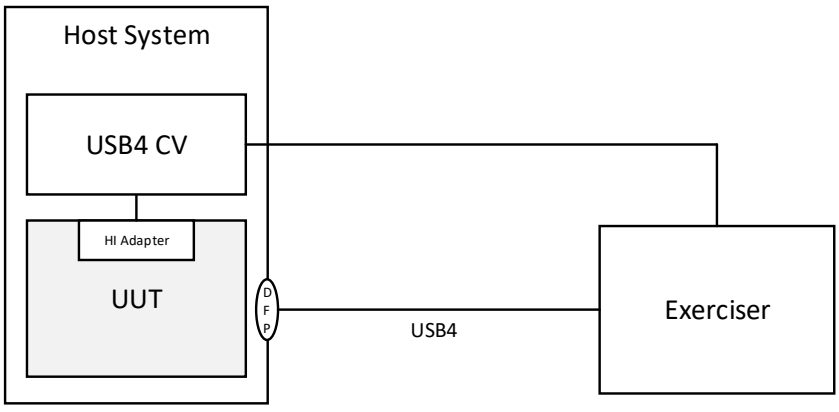
- The UFP of the Compliance Device is connected to the DFP of the UUT
- Unless specified otherwise, the Analyzer is connected between UUT and Compliance Device Router
- The Analyzer is invisible to UUT and Compliance Device



EX_HOST_DFP1

Description:

- The Exerciser is connected to the DFP of the UUT



Subroutines

Router Enumeration Procedure

The steps in this section are performed whenever a test step calls for a Router to be enumerated.

USB4 CV performs the following steps:

1. Wait for a Hot Plug Event Packet with UPG=0 for Lane 0 and Lane 1
2. Set the *Lock* bit in the Port that detected the connection to 0b
3. Send the UUT a Write Request that writes the following fields:
    a. *Connection Manager USB4 Version* = 1.0 (for a USB4 Connection Manager)
    b. *Connection Manager USB4 Version* = 0.0 (for a TBT3 Connection Manager)
    c. *Topology ID* = Router TopologyID (assigned per USB4 Specification)
    d. *Depth* = Router depth (0 for a Host Router, or 1 for a Device Router)
    e. *Valid* = 1b

Lane Bonding Initiation Procedure

The steps in this section are performed whenever a test step calls for Lane bonding to be initiated.

USB4 CV performs the following steps:

1. Send the UUT a Write Request that writes the following fields:
    a. *Target Link Width* = 1b
    b. *Lane Bonding* = 1b
2. Send the Link Partner of the UUT a Write Request that writes the following fields:
    a. *Target Link Width* = 1b
    b. *Lane Bonding* = 1b
3. Wait for a Hot Plug Packet with UPG=1 for Lane 1

Router Reset Procedure

The steps in this section are performed whenever a test calls for the UUT to be reset.

1. Teardown any Paths in the UUT
2. Disable, then enable all Transmit and Receive Rings
3. Perform a DFP Reset in each of the Downstream Facing Ports
4. Reset the Host Interface using the Host Interface Reset Register

Router Connect Procedure

The steps in this section are performed whenever a test calls for a USB4 device or the Exerciser to be connected to a UUT. The Adapters in the DFP being connected are enabled, which simulates a new connection.

USB4 CV performs the following steps in the DFP that is being connected:

1. Set the *Lane Disable* bit in the Lane 0 Adapter to 0b
2. Set the *Lane Disable* bit in the Lane 1 Adapter to 0b

Note: This step assumes that the Compliance Device/Exerciser is physically connected to the DFP and the DFP Adapters have been disabled using the Router Assembly Disconnect Procedure below.

Router Disconnect Procedure

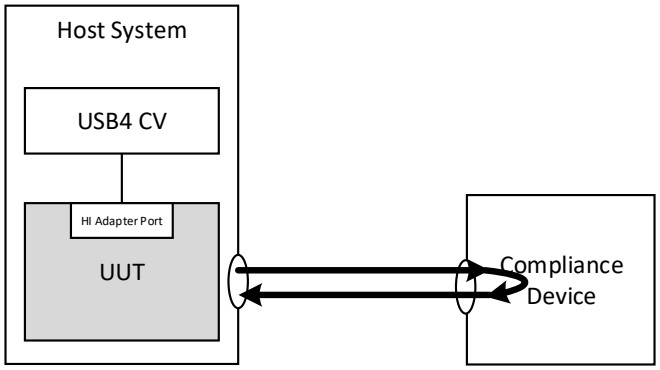
The steps in this section are performed whenever a test calls for a USB4 device or the Exerciser to be disconnected from a UUT. The Adapters in the DFP being disconnected are disabled, which simulates a disconnect.

USB4 CV performs the following steps in the DFP that is connected to the device being disconnected:

1. Set the *Lane Disable* bit in the Lane 1 Adapter to 1b
2. Wait for a Hot Plug Event Packet with UPG=1 for Lane 1
3. Set the *Lane Disable* bit in the Lane 0 Adapter to 1b
4. Wait for a Hot Plug Event Packet with UPG=1 for Lane 0

Loopback Path Setup

A Loopback Path allows USB4 CV to inject traffic into a USB4 fabric by sending itself USB4 Packets using Host-to-Host Tunneling. The USB4 Packets are generated by USB4 CV and routed through the UUT out to the Compliance Device and back through the UUT. The loopback Path uses Ring 1.



The steps in this section are performed whenever a test calls for a loopback path to be setup.

Note: When Lanes are bonded, only Lane 0 Path Configuration Space needs to be configured.

Part 1 – Configure the Path Segments

USB4 CV performs the following steps in each Adapter along the loopback Path starting with the Source Adapter and ending with the Destination Adapter:

1. For all Adapters, configure the HopID/routing table using the following fields in Path Configuration Space:
    a. *Output Adapter*
    b. *Output HopID*
    c. *Priority*
    d. *Weight*
2. If Adapter is Lane Adapter, set the Flow Control parameters using the following fields in Path Configuration Space:
    a. *Path Credits Allocated*
    b. *ESE*
    c. *ISE*
    d. *EFC*
    e. *IFC*
3. Set the *Valid* bit in Path Configuration Space to 1b

Part 2 – Enable Loopback

After all Path segments are configured, do the following in each Protocol Adapter along the loopback Path starting with the Source Adapter and ending with the Destination Adapter

4. Set the *Valid* bit in each of the Tx and Rx Rings to 1b

Loopback Teardown

The steps in this section are performed whenever a test calls for a loopback Path to be torn down.

Part 0 – Configure Adapters Credits fields

Upstream of the UUT, in each Lane Adapter along the loopback Path USB4 CV configures the following:

- If the Loopback Path is configured with Flow Control Disabled, set the *Non-Flow Controlled Buffers* field in the Adapter Configuration Space to: *Total Buffers – Path Credits Allocated* for Path 0.
- If the Loopback Path is configured with Restricted Shared or Shared flow control, set the *Link Credits Allocated* field in the Adapter Configuration Space to: MIN(*Total Buffers – Path Credits Allocated* for Path 0, 128).

Part 1 – Disable Loopback

USB4 CV performs the following steps in each Adapter along the loopback Path starting with the Destination Adapter and ending with the Source Adapter:

1. Set the *Enable* bit in Adapter Configuration Space to 0b

Part 2 – Teardown Path Segments

USB4 CV performs the following steps in each Adapter along the loopback Path starting with the Destination Adapter and ending with the Source Adapter:

2. Set the *Valid* bit in Path Configuration Space to 0b
3. Read the *Pending Requests* bit in Path Configuration Space
4. Poll the *Pending Requests* bit until it is 0b
5. Wait tTeardown time

Test Descriptions

~~Ring 0 Tests~~

~~The tests in this section only apply to Transmit Ring 0 and Receive Ring 0.~~Unless noted otherwise, repeat the tests in this section for the following:

- Transmit Ring 1 and Receive Ring 1 (if only 1 Transmit and 1 Receive Ring are implemented)
- Transmit Ring 1 and Receive Ring Max (if more than 1 Transmit and 1 Receive Ring are implemented)
- Transmit Ring Max and Receive Ring 1 (if more than 1 Transmit and 1 Receive Ring are implemented)
- Transmit Ring Max/2 and Receive Ring Max/2 (if more than 2 Transmit Rings and 2 Receive Rings are implemented). *Note: If Max is an odd number, round up to nearest whole number.*

Unless noted otherwise, repeat tests in this section with E2E flow control enabled (*E2E Flow Control Enable* bit = 1b) and disabled (*E2E Flow Control Enable* bit = 0b).

TD 12.001 Ring 0 General Test

Note: This test only applies to Transmit Ring 0 and Receive Ring 0.

Note: The Analyzer is not required for this test and may be omitted from the test setup. However, it may be used in the background for debugging purposes to capture a trace while the test is being performed.

A. Purpose:

- Verify that Ring 0 is in Raw Mode
- Verify that the UUT sets the *Descriptor Done* bit to 1b, when *Request Status* is 1b
- Verify that Transmit Ring 0 and Receive Ring 0 do not use E2E flow control
- Verify that the UUT reads from a Ring 0 transmit descriptor correctly
- Verify that the UUT writes back to a Ring 0 receive descriptor correctly

B. Asserts:

- 12.1#1
- 12.3.1#15
- 12.3.2.2#4, 12.3.2.2#5
- 12.3.1#10, 12.3.1#14-11, 12.3.1#17-15,
- 12.4.1#5, 12.4.1#10, 12.4.1#14, 12.4.1#17
- 12.4.2.2#8, 12.4.2.2#9
- 12.5.2#2

C. Setup:

- AN_HOST_DFP1

D. Repetitions:

- Repeat test with the following values in the Ring 0 Transmit Descriptor and corresponding Control Packet:
  - EOF PDF = 1h; SOF PDF = Eh (Read Request)
  - EOF PDF = 2h; SOF PDF = 9h (Write Request)
- Repeat test with:
  - *Interrupt Enable* = 0b in all Ring 0 Transmit Descriptors and *Interrupt Enable* = 1b in all Ring 0 Receive Descriptors
  - *Interrupt Enable* = 1b in all Ring 0 Transmit Descriptors and *Interrupt Enable* = 0b in all Ring 0 Receive Descriptors

E. Procedure:

USB4 CV performs the following test steps:

1. Reset UUT
2. Enumerate UUT
3. Read the Ring Control Register for Transmit Ring 0 and verify that the *Raw Mode* bit is set to 1b (12.1#1)
4. Read the Ring Control Register for Receive Ring 0 and verify that the *Raw Mode* bit is set to 1b (12.1#1)
5. Set the following in all Transmit Descriptors for Ring 0.
    a. Request Status = 1b
    b. Interrupt Enable = (see repetitions)
    c. *EOF PDF* = see repetitions
    d. *SOF PDF* = see repetitions
6. Set the following in all Receive Descriptors for Ring 0.
    a. Request Status = 1b
    b. Interrupt Enable = (see repetitions)
    c. *EOF PDF* = see repetitions
    d. *SOF PDF* = see repetitions
7. Send the UUT a Request using Transmit Ring 0.
8. If *Interrupt Enable* = 1b for a Transmit Descriptor, verify that the UUT issues an interrupt after Data Buffer completion in the Transmit Descriptor. (12.3.2.2#5, 12.3.1#18)
9. If *Interrupt Enable* = 0b for a Transmit Descriptor Ring, verify that the UUT does not send any interrupts for Transmit Descriptor completion. (12.5.2#2)
10. Read the Transmit Descriptor from the transfer and verify that:
    a. *EOF PDF* is the same as set in Step 5c (12.3.1#10)
    b. *SOF PDF* is the same as set in Step 5d (12.3.1#14)
    c. *Request Status* = 1b (12.3.1#17)
    d. *Interrupt Enable* = value set by USB4 CV (12.3.1#19)
    e. *Descriptor Done* bit in the Transmit Descriptor is 1b. (12.3.1#18, 12.3.2.2#4)
11. If *Interrupt Enable* = 0b for a Receive Descriptor Ring, verify that the UUT issues an interrupt. (12.4.2.2#9)
12. If *Interrupt Enable* = 0b for a Receive Descriptor Ring, verify that the UUT does not issue an interrupt. (12.5.2#2)
13. Verify that the Response is posted in a single Data Buffer. (12.1#1)
    a. Producer and Consumer Indexes indicate only one Packet is waiting to be consumed and the DD bit in the Receive Descriptor indicates that the Response is fully written.
14. Read the Receive Descriptor and verify the following: (12.4.2.2#8)
    a. *EOF PDF* field is same as in the corresponding Transmit Descriptor (12.4.1#5)
    b. *CRC Error* field = 0b (12.4.1#10)
    c. *Buffer Overflow* = 0b (12.4.1#14)
    d. *Descriptor Done* bit = 1b (12.4.1#12)
    e. *Interrupt Enable* bit = value set by USB4 CV (12.4.1#17)
15. Verify that the UUT did not send any E2E Flow Control Packets for Ring 0 (12.2#1)

Host-to-Host Tunneling Tests

Unless noted otherwise, repeat the tests in this section for the following:

- Transmit Ring 1 and Receive Ring 1 (if only 1 Transmit and 1 Receive Ring are implemented)
- Transmit Ring 1 and Receive Ring Max (if more than 1 Transmit and 1 Receive Ring are implemented)
- Transmit Ring Max and Receive Ring 1 (if more than 1 Transmit and 1 Receive Ring are implemented)
- Transmit Ring Max/2 and Receive Ring Max/2 (if more than 2 Transmit Rings and 2 Receive Rings are implemented). *Note: If Max is an odd number, round up to nearest whole number.*

Unless noted otherwise, repeat tests in this section with E2E flow control enabled (*E2E Flow Control Enable* bit = 1b) and disabled (*E2E Flow Control Enable* bit = 0b).

TD 12.002 Frame Mode Test

A. Purpose:

- Verify that the UUT sends E2E Flow Control Packets in Frame Mode
- Verify that the UUT reads from a transmit descriptor correctly in Frame Mode
- Verify that the UUT writes back to a receive descriptor correctly in Frame Mode
- Verify that the UUT completes Host-to-Host Tunneling transfer correctly in Frame Mode

B. Asserts:

- 12.1.3#2–11
- 12.2.1.1#1–4
- 12.2.1.2#1–3
- 12.2.2.4#2
- 12.2.2.4#7
- 12.3.1#10, 12.3.1#14, 12.3.1#17–15
- 12.3.2.1#5–9, 12.3.2.1#11–13, 12.3.2.1#19–20
- 12.4.1#6, 12.4.1#9, 12.4.1#12, 12.4.1#16, 12.4.1#17
- 12.4.2.1#1, 12.4.2.1#12–14

C. Setup:

- AN_HOST_DFP1

D. Repetitions:

- Repeat with Frame size of 4096 bytes where:
  - Frame is written to 1 Transmit Descriptor
  - Frame is written to 2 Transmit Descriptors
  - Frame is written to 4 Transmit Descriptors

E. Procedure:

USB4 CV performs the following test steps:

1. Reset UUT
2. Enumerate UUT
3. Set up a loopback Path
4. Configure the Transmit Descriptor Ring and Receive Descriptor Ring for the Source and Destination Host Interface Adapters:
   a. Set the *E2E Flow Control Enable* bit in the Ring Control Register
   b. Set the Raw Mode bit in the Ring Control Register to 0b for Frame Mode
5. In the first Transmit Descriptor for the Frame (if transfer has at least 2 Packets)
   a. Set the *SOF PDF* to 1h
   b. Set the *EOF PDF* to 0h

    c. Set *Request Status* bit to 1b
    d. Set Interrupt Enable bit to 1b
6. In the middle Transmit Descriptors for the Frame (if transfer has more than 2 Packets)
    a. Set the *EOF PDF* to 0h
    b. Set the *SOF PDF* to 0h
    c. Set *Request Status* bit to 1b
    d. Set Interrupt Enable bit to 1b
7. In the last Transmit Descriptor for the Frame:
    a. Set the *SOF PDF* to 0h
    b. Set the *EOF PDF* to Eh
    c. Set *Request Status* bit to 1b
    d. Set Interrupt Enable bit to 1b
8. In each Receive Descriptor:
    a. Set *Request Status* bit to 1b
    b. Set Interrupt Enable bit to 1b
9. Configure *Transmit E2E HopID* to equal to destination.
10. Start the Analyzer.
11. Wait 1 minute (to allow enough time to capture E2E Credit Sync Packets).
12. Initiate a transfer on the loopback Path (see repetitions).
13. Verify that the UUT issues an interrupt. (12.3.2.1#21)
14. For the Transmit Descriptor for the Frame verify that:
    a. *EOF PDF* = value set by USB4 CV (12.3.1#10)
    b. *SOF PDF* = value set by USB4 CV (12.3.1#14)
    c. *Request Status* = value set by USB4 CV (12.3.1#17)
    d. *Interrupt Enable* = value set by USB4 CV (12.3.1#19)
    e. The *Descriptor Done* bit is 1b. (12.3.1#18, 12.3.2.1#20)
15. Verify that the UUT issues an interrupt after the Data buffer in the Receive Descriptor for the transfer is completed. (12.4.2.1#17)
16. After UUT writes back to the Receive Descriptor, verify the following: (12.4.2.1#16)
    a. *EOF PDF* is Eh (12.4.1#6)
    b. *SOF PDF* is 1h in the first Receive Descriptor (12.4.1#9)
    c. *Descriptor Done* bit is 1b (12.4.1#12)
    d. *Buffer Overflow* bit is 0b (12.4.1#16)
    e. *Interrupt Enable* field is 1b (12.4.1#17)
17. Compare the transmitted data with the data in the Data Buffer for the Receive Descriptor.
18. Verify that all data transmitted in the loopback transfer is received back. (12.4.2.1#1)
19. Verify that all data from transfer is in the correct order. (12.1.3#2, 12.1.3#5, 12.1.3#8, 12.1.3#9, 12.4.2.1#12, 12.4.2.1#13, 12.4.2.1#14)
20. Stop the Analyzer.

Parse the Trace from the Analyzer and verify the following:

21. For all E2E Credit Sync Packets from the UUT:
    a. *Length* is 04h (12.2.1.2#1)
    b. *ECC* is valid (12.2.1.2#2)
    c. Bits 30:21 are 0 (Rsvd) (12.2.1.2#1)
    d. *Credit Sync* field is 1b (12.2.1.2#3)
22. Verify that the UUT sent an E2E Credit Grant Packet every $T_{E2ERATE}$ (12.2.2.4#2)
23. Verify the following for any E2E Credit Grant Packets from the UUT
    a. *Length* is 04h (12.2.1.1#1)
    b. *ECC* field is valid (12.2.1.1#3)
    c. *HopID* field is equal to Transmit E2E HopID (12.2.1.1#2)
    d. *Credits* field does not exceed 8192 (12.2.2.4#7)
    e. Bits 30:21 are 0 (Rsvd) (12.2.1.1#1)
    f. *Credit Sync* field is 0b (12.2.1.1#4)

24. For an SOF Packet, PDF = 1h (12.1.3#4)
25. For a MOF Packet, PDF = 0h (12.1.3#7)
26. For a EOF Packet:
    a. PDF = Eh (12.1.3#11)
    b. Packet contains a complete 32-bit CRC (12.1.3#10, 12.3.2.1#9)
    c. CRC is immediately after the last byte of payload (12.3.2.1#13)
    d. CRC matches the calculated value (12.3.2.1#11, 12.3.2.1#12)
27. A SOF Packet is always followed by a MOF Packet or an EOF Packet. (12.1.3#3, 12.3.2.1#6)
28. A MOF Packet always comes after a EOF Packet or another MOF Packet. (12.1.3#6, 12.3.2.1#7)
29. The HopID in a Tunneled Packet matches the HopID associated with the Transmit Descriptor Ring being tested. (12.3.2.1#19)

TD 12.003 Raw Mode Test

A. Purpose:

- Verify that the UUT sends E2E Flow Control Packets in Raw Mode
- Verify that the UUT writes back to a receive descriptor correctly in Raw Mode
- Verify that the UUT reads from a transmit descriptor correctly in Raw Mode
- Verify that the UUT completes Host-to-Host Tunneling transfer correctly in Raw Mode

B. Asserts:

- 12.2.1.1#1–4
- 12.2.1.2#1–3
- 12.2.2.4#2
- 12.2.2.4#7
- 12.3.1#10, 12.3.1#14, 12.3.1#17-15
- 12.3.2.2#3–5
- 12.4.1#5, 12.4.1#10, 12.4.1#12, 12.4.1#14, 12.4.1#17
- 12.4.2.2#2, 12.4.2.2#8, 12.4.2.2#9
- 12.3.1#11

C. Setup:

- AN_HOST_DFP1

D. Repetitions:

- Repeat for transfers with length = 1 byte, 100 bytes, and 256 bytes

E. Procedure:

USB4 CV performs the following test steps:

1. Reset UUT
2. Enumerate UUT
3. Set up a loopback Path
    a. Path uses Raw Mode
    b. Flow control is enabled
4. Configure the Transmit Descriptor Ring and Receive Descriptor Ring for the Source and Destination Host Interface Adapters:
    a. Set the E2E Flow Control Enable bit in the Ring Control Register
    b. Set the Raw Mode bit in the Ring Control Register to 1b for Raw Mode
5. In each Transmit Descriptor:
    a. Set *Request Status* bit to 1b
    b. Set Interrupt Enable bit to 1b
    c. Set *EOF PDF* to 1h

    d. Set *SOF PDF* to Eh
6. In each Receive Descriptor:
    a. Set *Request Status* bit to 1b
    b. Set Interrupt Enable bit to 1b
7. Configure *Transmit E2E HopID* to equal to target.
8. Start the Analyzer.
9. Wait 1 minute (to allow enough time to capture E2E Credit Sync Packets)
10. Initiate a transfer on the loopback Path.
11. Verify that the UUT issues an interrupt. (12.3.2.2#5)
12. For each Transmit Descriptor verify that:
    a. *EOF PDF* is 1h (12.3.1#10)
    b. *SOF PDF* is Eh (12.3.1#14)
    c. Request Status 1b (12.3.1#17)
    d. *Interrupt Enable* 1b (12.3.1#19)
    e. The *Descriptor Done* bit is 1b. (12.3.1#18, 12.3.2.1#20)
    f. *Descriptor Done* bit is 1b. (12.3.1#18, 12.3.2.2#4)
13. Verify that the UUT issues an interrupt after writing to the Receive Data Buffer. (12.4.2.2#9)
14. After UUT writes back to a receive descriptor, verify the following: (12.4.2.2#8)
    a. *EOF PDF* is 1h (12.4.1#5)
    b. *CRC Error* field is 0b (12.4.1#10)
    c. *Buffer Overflow* is 0b (12.4.1#14)
    d. *Descriptor Done* bit is 1b (12.4.1#12)
    e. *Interrupt Enable* bit is 1b (12.4.1#17)
15. Verify that all data from transfer is received back on the loopback Path and is in the correct order. (12.4.2.2#2)
16. Stop the Analyzer.

Parse the Trace from the Analyzer and verify the following:

17. For all E2E Credit Sync Packets from the UUT:
    a. *Length* is 04h (12.2.1.2#1)
    b. *ECC* is valid (12.2.1.2#2)
    c. Bits 30:21 are 0 (Rsvd) (12.2.1.2#1)
    d. *Credit Sync* field is 1b (12.2.1.2#3)
18. Verify that the UUT sent an E2E Credit Grant Packet every $T_{E2ERATE}$ (12.2.2.4#2)
19. Verify the following for any E2E Credit Grant Packets from the UUT
    a. *Length* is 04h (12.2.1.1#1)
    b. *ECC* field is valid (12.2.1.1#3)
    c. *HopID* field is equal to 1 (Transmit E2E HopID from Step 8) (12.2.1.1#2)
    d. *Credits* field does not exceed 8192 (12.2.2.4#7)
    e. Bits 30:21 are 0 (Rsvd) (12.2.1.1#1)
    f. *Credit Sync* field is 0b (12.2.1.1#4)
20. The PDF in the Tunneled Packet matches the *EOF PDF* field in the Transmit Descriptor (12.3.2.2#3, 12.3.1#11)

TD 12.004 Single Data Buffer Test

Note: The Analyzer is not required for this test and may be omitted from the test setup. However, it may be used in the background for debugging purposes to capture a trace while the test is being performed.

A. Purpose:

- Verify that the UUT posts each Tunneled Packet payload into a separate Data Buffer when in Raw Mode
- Verify that the UUT does not post more than one Frame into a Data buffer when in Frame Mode

B. Asserts:

- 12.4.2.2#1
- 12.3.2.1#2

C. Setup:

- AN_HOST_DFP1

D. Repetitions:

- Repeat in Raw Mode (*Raw Mode* bit = 1b) and in Frame Mode (*Raw Mode* bit = 0b)

E. Procedure:

USB4 CV performs the following test steps:

1. Reset UUT
2. Enumerate UUT
3. Set up a loopback Path
    a. Flow control is enabled
4. Configure the Transmit Descriptor Ring and Receive Descriptor Ring for the Source and Destination Host Interface Adapters:
    a. Set the E2E Flow Control Enable bit in the Ring Control Register
    b. Set the Raw Mode bit in the Ring Control Register (see repetitions)
5. Send the UUT a series of 10 loopback transfers that are each 100-bytes in length.
6. When the UUT completes a transfer:
    a. Look at the Data Length field in the posted Receive Descriptor
    b. Verify that the Data Length field in the Receive Descriptor is 1. (12.4.2.2#1, 12.3.2.1#2)
7. After the last transfer completes, verify that a total of 10 Receive Descriptors were written back to (12.4.2.2#1, 12.3.2.1#2)

TD 12.005 Interrupt Disable Test

Note: The Analyzer is not required for this test and may be omitted from the test setup. However, it may be used in the background for debugging purposes to capture a trace while the test is being performed.

A. Purpose:

- Verify that the UUT does not issue interrupts when interrupts are disabled

B. Asserts:

- 12.5.2#2

C. Setup:

- AN_HOST_DFP1

D. Repetitions:

- Repeat in Raw Mode (Raw Mode bit = 1b) and in Frame Mode (Raw Mode bit = 0b)
- Repeat with:
  - *Interrupt Enable* = 0b in all Transmit Descriptors and *Interrupt Enable* =1b in all Receive Descriptors
  - *Interrupt Enable* = 1b in all Transmit Descriptors and *Interrupt Enable* = 0b in all Receive Descriptors

E. Procedure:

USB4 CV performs the following test steps:

1. Reset UUT
2. Enumerate UUT
3. Set up a loopback Path
4. Configure the Transmit Descriptor Ring and Receive Descriptor Ring for the Source and Destination Host Interface Adapters:
   a. Set the *E2E Flow Control Enable* bit in the Ring Control Register
   b. Set the Raw Mode bit in the Ring Control Register (see repetitions)
5. Set *Interrupt Enable* bits (see repetitions)
6. Initiate a series of ten loopback transfers
   a. If the Descriptors are configured in Frame Mode, each transfer is 4096 bytes
   b. if the Descriptors are configured for Raw Mode, each transfer is 256 bytes
7. If *Interrupt Enable* = 0b for a Transmit Descriptor Ring, verify that the UUT does not send any interrupts for Transmit Descriptor completion. (12.5.2#2)
8. If *Interrupt Enable* = 0b for a Receive Descriptor Ring, verify that the UUT does not send any interrupts for Receive Descriptor completion. (12.5.2#2)

TD 12.006 Ring Disabled Test

Note: Do not perform this test with E2E flow control enabled.

A. Purpose:

- Verify that descriptors are not processed when a ring is disabled
- Verify that E2E flow control packets are not sent when E2E Flow Control is disabled

B. Asserts:

- 12.2.2.3#4
- 12.2.2.4#5
- 12.4.2#2

C. Setup:

- AN_HOST_DFP1

D. Repetitions:

- Repeat in Raw Mode (Raw Mode bit = 1b) and in Frame Mode (Raw Mode bit = 0b)

E. Procedure:

USB4 CV performs the following test steps:

1. Reset UUT
2. Enumerate UUT
3. Set up a loopback Path
4. Configure the Transmit Descriptor Ring and Receive Descriptor Ring for the Source and Destination Host Interface Adapters:
    a. Set the E2E Flow Control Enable bit in the Ring Control Register to 0b to disable E2E flow control
    b. Set the Raw Mode bit in the Ring Control Register (see repetitions)
5. Start the Analyzer
6. Initiate a loopback transfer by increasing the Producer Index of the Tx Ring
7. Wait for transfer to complete
8. Set the *Valid* bit in the Receive Descriptor Ring to 0b
9. Initiate a loopback transfer
10. Wait 1 minute (transfer should fail)
11. Teardown the loopback Path
12. Set up the same loopback Path as in Step 5
13. Initiate a loopback transfer
14. Verify that loopback transfer completes successfully
    a. All data transmitted in the transfer is received back
    b. All data from transfer is in the correct order
15. Stop the Analyzer

Parse the Trace from the Analyzer and verify the following:

16. UUT did not send any E2E Credit Sync Packets (12.2.2.3#4)
17. UUT did not send any E2E Credit Grant Packets (12.2.2.4#5)
18. UUT did not send any Host Interface Tunneled Packets while *Valid* bit was 0b in Receive Descriptor Ring (i.e. between Control Packet setting Valid bit to 0b and Control Packet setting Valid bit to 1b) (12.4.2#2)

TD 12.007 Low Power Test

Note: This test is only performed if the UUT supports low power (CLx) states.

Note: Do not perform this test with E2E flow control disabled.

Note: The Analyzer is not required for this test and may be omitted from the test setup. However, it may be used in the background for debugging purposes to capture a trace while the test is being performed.

A. Purpose:

- Verify that E2E flow control packets are not sent when Link is in low power state

B. Asserts:

- 12.2.2.3#4
- 12.2.2.4#6

C. Setup:

- AN_HOST_DFP1

D. Repetitions:

- Repeat in Raw Mode and in Frame Mode
- Repeat for each supported CLx state

E. Procedure:

USB4 CV performs the following test steps:

1. Reset UUT
2. Enumerate UUT
3. Set up a loopback Path
4. Configure the Transmit Descriptor Ring and Receive Descriptor Ring for the Source and Destination Host Interface Adapters:
    a. Set the E2E Flow Control Enable bit in the Ring Control Register to 1b to enable E2E flow control
    b. Set the Raw Mode bit in the Ring Control Register (see repetitions)
5. Transition the Link to low power state (CLx)
6. Wait 1 minute
7. Verify that:
    a. UUT did not send any E2E Credit Sync Packets (12.2.2.3#4)
    b. UUT did not send any E2E Credit Grant Packets (12.2.2.4#6)

TD 12.008 Dropped Packet Test (Exerciser Required)

A. Purpose:

- Verify that the UUT handles transfers with dropped packet correctly

B. Asserts:

- 12.4.1#11
- 12.4.2.1#7-11

C. Setup:

- EX_HOST_DFP1

D. Repetitions:

- Repeat with transfers missing the SOF packet, a MOF packet, and the EOF packet
- Repeat with a Frame Size of:
  - 140 Bytes (*Note: Will only have EOF packet*)
  - 300 Bytes (*Note: Will only have SOF and EOF packets*)
  - 600 Bytes
  - 4096 Bytes

E. Procedure:

USB4 CV performs the following test steps:

1. Reset UUT
2. Enumerate UUT
3. Set up a Path from the Exerciser to the UUT
4. Configure the Transmit Descriptor Ring and Receive Descriptor Ring for the Source and Destination Host Interface Adapters:
   a. Set the *E2E Flow Control Enable* bit in the Ring Control Register
   b. Set the Raw Mode bit in the Ring Control Register to 0b for Frame Mode
5. Tell Exerciser to send a transfer with a missing packet (see repetitions).
6. Wait for transfer to complete.
7. If SOF was dropped, verify that:
   a. The *SOF PDF* field in the Receive Descriptor is 0b (12.4.2.1#8, 12.4.2.1#10)
   b. The next packet payload is posted to a Data Buffer using the next available Receive Descriptor (12.4.2.1#7, 12.4.2.1#9)
8. If MOF was dropped, verify that the CRC Error field in the Receive Descriptor is 1b (12.4.1#11).
9. If EOF was dropped, verify that the next packet payload is posted to the beginning of the Data Buffer (overwriting any previous packets) (12.4.2.1#11)
10. Tell Exerciser to send a transfer (no missing packets)
11. Query Exerciser to verify that flow control credits counts are correct

TD 12.009 Padding Test

Note: The Analyzer is not required for this test and may be omitted from the test setup. However, it may be used in the background for debugging purposes to capture a trace while the test is being performed.

A. Purpose:

- Verify that the UUT inserts and removes packet padding correctly

B. Asserts:

- 12.3.2.1#18

C. Setup:

- AN_HOST_DFP1

D. Repetitions:

- Repeat with transfer sizes of:
  - 53 bytes (%4 = 1)
  - 50 bytes (%4 = 2)
  - 51 bytes (%4 = 3)
  - 52 bytes (%4 = 0)

E. Procedure:

USB4 CV performs the following test steps:

1. Reset UUT
2. Enumerate UUT
3. Set up a loopback Path
4. Configure the Transmit Descriptor Ring and Receive Descriptor Ring for the Source and Destination Host Interface Adapters:
   a. Set the E2E Flow Control Enable bit in the Ring Control Register
   b. Set the Raw Mode bit in the Ring Control Register to 0b for Frame Mode
5. Initiate a loopback transfer (see repetitions).
6. Wait for transfer to complete.
7. Verify that transfer completes successfully. (12.3.2.1#18)
   a. All data transmitted in the transfer is received back
   b. All data from transfer is in the correct order

TD 12.010 Multi-Path Test

Note: This test is only performed once per UUT.

Note: Do not perform this test with E2E flow control disabled.

Note: Ring 0 is used for the Control Path only, therefore it is not tested in this test.

Note: The Analyzer is not required for this test and may be omitted from the test setup. However, it may be used in the background for debugging purposes to capture a trace while the test is being performed.

A. Purpose:

- Verify that the UUT can operate with multiple H2H Paths

B. Asserts:

- 12#4
- 12.1#2
- 12.3#1
- 12.4#1, 12.4#2

C. Setup:

- AN_HOST_DFP1

D. Repetitions:

- Repeat with:
  - Odd numbered Rings, operates in Raw Mode and even numbered Rings, operate in Frame Mode (e.g. Ring 1 operates in Raw mode, Ring 2 operates in Frame mode, etc…)
  - Even numbered Rings, operates in Raw Mode and odd numbered Rings, operates in Frame Mode

    Note: In the above repetitions the Rings are aligned (e.g. Transmit Ring 1 and Receive Ring 1 are part of same Path, etc.).

- Repeat in Frame Mode with loopback Paths that have:
  - Transmit and Receive Rings aligned (e.g. Transmit Ring 1 and Receive Ring 1 are part of same Path, Transmit Ring 2 and Transmit Ring 2 are on same Path, etc.)
  - Transmit and Receive Rings skewed (e.g. Transmit Ring 1 and Transmit Ring N are part of same Path, Transmit Ring 2 and Transmit Ring N-1 are part of same Path, etc.)

E. Procedure:

USB4 CV performs the following test steps:

1. Reset UUT
2. Enumerate UUT
3. Verify that the UUT advertises support for at least 2 Transmit Descriptor Rings and at least 2 Receive Descriptor Rings (including Ring 0). (12#4)
4. If UUT only supports 2 Transmit/Receive Descriptor Rings, end test here and do not perform any repetitions. Otherwise, continue to next step.
5. Configure a loopback Path for each Ring that the UUT supports

6. Configure the Transmit Descriptor Rings and Receive Descriptor Rings for all of the Source and Destination Host Interface Adapters:
    a. Set the *E2E Flow Control Enable* bit in the Ring Control Register to 1b to enable E2E flow control
    b. Set the *Raw Mode* bit in the Ring Control Register (see repetitions)
7. Initiate 300 loopback transfers simultaneously on all Paths.
    a. In Raw Mode, the transfer size is 200 bytes.
    b. In Frame Mode, the transfer size is 2000 bytes.
8. For each Path:
    a. Verify that the number of packets sent equals the number of packets received. (12.1#2, 12.3#1, 12.4#1)
    b. Verify that the data sent is the same as the data received. (12.1#2, 12.3#1, 12.4#1)

TD 12.011 E2E Flow Control Test

Note: This test is only performed with E2E flow control enabled.

Note: The Analyzer is not required for this test and may be omitted from the test setup. However, it may be used in the background for debugging purposes to capture a trace while the test is being performed.

A. Purpose:

- Verify that the UUT does not lose packets when receive buffer space is not available

B. Asserts:

- 12.2.2.3#2, 12.2.2.3#3

C. Setup:

- AN_HOST_DFP1

D. Repetitions:

- Repeat in Raw Mode (Raw Mode bit = 1b) and Frame Mode (Raw Mode bit = 0b)

  Note: In the above repetitions, the Rings are aligned (e.g. Transmit Ring 1 and Receive Ring 1 are part of same Path, etc.).

- Repeat in Frame Mode with loopback Paths that have:
  - Transmit and Receive Rings aligned (e.g. Transmit Ring 1 and Receive Ring 1 are part of same Path, Transmit Ring 2 and Transmit Ring 2 are on same Path, etc.)
  - Transmit and Receive Rings skewed (e.g. Transmit Ring 1 and Transmit Ring N are part of same Path, Transmit Ring 2 and Transmit Ring N-1 are part of same Path, etc.)

E. Procedure:

USB4 CV performs the following test steps:

1. Reset UUT
2. Enumerate UUT
3. Set up a loopback Path
   a. Set the Receive Ring size to 100
   b. Do not empty the Receive Descriptors when they fill up
4. Configure the Transmit Descriptor Ring and Receive Descriptor Ring for the Source and Destination Host Interface Adapters:
   a. Set the *E2E Flow Control Enable* bit in the Ring Control Register to 1b
   b. Set the Raw Mode bit in the Ring Control Register (see repetitions)
5. Send 200 Tunneled Packets
6. Wait 10 seconds
7. Empty 50 Tunneled Packets from the Receive Descriptors
8. Wait 10 seconds
9. Empty the remaining Tunneled Packets from the Receive Descriptors
10. Verify that all 200 Tunneled Packets are received back (12.2.2.3#2, 12.2.2.3#3)

TD 12.012 PCIe Programming Interface Test

Note: This test is only performed once per UUT.

Note: This test is only performed with E2E flow control enabled.

Note: The Analyzer is not required for this test and may be omitted from the test setup. However, it may be used in the background for debugging purposes to capture a trace while the test is being performed.

A. Purpose:

- Verify that the PCIe interface is implemented correctly

B. Asserts:

- 12.6.3.1.2#1, 12.6.3.1.2#2

C. Setup:

- AN_HOST_DFP1

D. Procedure:

USB4 CV performs the following test steps:

1. Reset UUT
2. Enumerate UUT
3. Setup a loopback Path
    a. Disable ISR Auto-Clear = 1b
    b. Host Interface CL1 Enable = 1b
    c. Host Interface CL2 Enable = 1b
    d. E2E Flow Control Enable = 1b
    e. No-Snoop Flag = 1b
    f. Raw Mode = 1b
4. Write to the Base Address Registers (Base Address Low and Base Address High)
5. Read the Producer and Consumer Indexes Register and verify that:
    a. Producer Index = 0
    b. Consumer Index = 0
6. Perform a large loopback transfer
7. Set the RST bit in the Host Interface Reset Register to 1b
8. Wait tHIReset time (10ms)
9. Read the RST bit in the Host Interface Reset Register
10. Verify that the RST bit is 0b (12.6.3.1.2#2)
11. Read the following fields in the Host Interface Registers and verify default values: (12.6.3.1.2#1)
    a. Disable ISR Auto-Clear = 0b
    b. Host Interface CL1 Enable = 0b
    c. Host Interface CL2 Enable = 0b
    d. E2E Flow Control Enable = 0b
    e. No-Snoop Flag = 0b
    f. Raw Mode = 0b