USB4™ PCIe Tunneling Compliance Test Specification

Date: October 2021

Revision: 1.2

Revision History:

Revision	Issue Date	Comments
1.0	June 2020	First Release
1.1	January 2021	With clarifications and corrections
1.2	June 2021	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through October 15, 2020.
1.3	October 2021	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.

Contents

Introduction

The tests in this test specification verify that the Router in a USB4 Host, Hub, or Peripheral Device is compliant with Chapter 11 of the USB4™ Specification.

Terminology

The following table describes the terms used in this document.

Analyzer	Test tool that captures and parses packets, transactions, ordered sets, etc.
Compliance Device	A KG USB4 Device that is capable of performing Transport Layer Packet loopback.
DFP	Downstream Facing Port.
Exerciser	The compliance test tool (hardware and software) that implements USB4 Port functionality and the behavior required for compliance testing.
IOP	Interop Testing. See USB4™ Interop Test Specification.
KG USB4 Device	“Known Good” USB4 Device. A USB4 Device that is known to be compliant with the USB4 Specification.
KG USB4 Host	“Known Good” USB4 Host. A USB4 Host that is known to be compliant with the USB4 Specification.
KG TBT3 Device	A Certified Thunderbolt 3 Device.
KG TBT3 Host	A Certified Thunderbolt 3 Host.
PUT	Port Under Test. The Port on a UUT that is being tested for compliance. Only Ports that support PCIe Tunneling are tested.
UFP	Upstream Facing Port.
USB4 CV	USB4 Command Verifier software. The software that runs compliance tests and analyzes the results.
USB4 Product	Refers to a USB4 host, USB4 hub, and/or USB4 device. Includes silicon, reference platforms, and end product.
UUT	The Router being tested for compliance.
VIF	Vendor Information File. File provided by UUT vendor that provides information about the characteristics and capabilities of the UUT.

Assertions

Compliance criteria are provided as a list of assertions that describe specific characteristics or behaviors that must be met. Each assertion provides a reference to the USB4 specification or other documents from which the assertion was derived. In addition, each assertion provides a reference to the specific test description(s) where the assertion is tested.

Each test assertion is formatted as follows:

Assertion #	Test #	Assertion Description

Assertion#: Unique identifier for each spec requirement. The identifier is in the form USB4_SPEC_SECTION_NUMBER#X, where X is a unique integer for a requirement in that section.

Assertion Description: Specific requirement from the specification

Test #: A label for a specific test description in this specification that tests this requirement. Test # can have one of the following values:

NT	This item is not explicitly tested in a test description. Items can be labeled NT for several reasons – including items that are not testable, not important to test for interoperability, or are indirectly tested by other operations performed by the compliance test.
X.X	This item is covered by the test described in test description X.X in this specification.
BCP	This assertion is verified by the Background Check Procedure.

Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

The following Table presents the Chapter 11 assertions.

Assertion #	Test Name	Assertion Description
11 PCI Express Tunneling		
11#1	TD 11.1	A USB4 host that tunnels PCIe traffic shall do one of the following: Incorporate an internal PCIe Switch; Connect to a Root Complex via Root Ports; Connect to a Root Complex via other means that meet the PCIe Specification.
11#2	NT	The Host Router in a USB4 host that supports PCIe Tunneling shall have one Downstream PCIe Adapter per Downstream Facing Port. Each Downstream PCIe Adapter shall interface to a downstream port of the internal PCIe Switch or Root Complex.

11#3	TD 11.1	A USB4 hub shall support PCIe Tunneling. A USB4 hub shall contain an internal PCIe Switch.
11#4	NT	The Device Router in a USB4 hub shall have: An Upstream PCIe Adapter that interfaces to the internal PCIe Switch; For each Downstream Facing Port, a Downstream PCIe Adapter that interfaces to a downstream port of the internal PCIe Switch.
11#5	TD 11.1	A USB4 device that tunnels PCIe traffic shall contain either an internal PCIe Switch or an internal PCIe Endpoint.
11#6	NT	The Device Router in a USB4 device that supports PCIe tunneling shall have an Upstream PCIe Adapter that interfaces to the internal PCIe Switch or Endpoint.
11.2 Internal PCIe Ports		
11.2#1	TD 11.4 TD 11.5 TD 11.6 TD 11.7 TD 11.9 TD 11.11	Each internal PCIe port that interfaces to a PCIe Adapter shall implement a Physical Layer Logical sub-block, a Data Link Layer, and a Transaction Layer as defined in the PCIe Specification.
11.2.1 PCIe Physical Layer Logical Sub-block		
11.2.1#1	TD 11.2	The Logical sub-block shall update the PCIe configuration registers with the following characteristics: PCIe Gen 1 protocol behavior; Max Link Speed field in the Link Capabilities Register set to 0001b (data rate of 2.5 GT/s only).
11.2.1.1 Encoding		
11.2.1.1#1	NT	The Physical Layer Logical sub-block shall: Not scramble the bits it delivers to the PCIe Adapter Layer; Not de-scramble the bits it receives from the PCIe Adapter Layer, regardless of the Disable Scrambling bit received in the TS Ordered Set.
11.2.1.2 Link Training and Status State Machine (LTSSM)		
11.2.1.2#1	TD 11.7	The LTSSM shall support the L1 state.
11.2.1.2#2	TD 11.3 (partially)	The LTSSM shall not support the following: Loopback state; L0s state; L1 PM substates; Changes in PCIe link speed; Lane-to-Lane de-skew; Inferring Electrical Idle in states other than L0.

11.2.1.2#3	NT	A PCIe Upstream port in Recovery.idle shall transition to L0 state when it receives a TLP or DLLP. If the port does not receive any TLP or DLLP, it shall transition to the L0 state tRecovery time after it entered the Recovery.idle state.
11.2.1.2#4	NT	A PCIe Downstream Port, shall immediately send UpdateFC after transitioning from L1 to L0.
11.2.1.3 ASPM L1 Entry		
11.2.1.3#1	TD 11.8	The PCIe Upstream Port shall send no more than 10 additional PM_Active_State_Request DLLPs after sending an ACK DLLP for the received PM_Active_State_Nak message.
11.2.1.3#2	NT	After receiving the ACK DLLP for the PM_Active_State_Nak message, the PCIe Downstream Port shall wait 9.5 microseconds as described in the PCIe Specification and shall drop the first 10 PM_Active_State_Request DLLPs it receives. If it receives a TLP or DLLP which is not a PM_Active_State_Request DLLP, it may not drop the next PM_Active_State_Request DLLPs.
11.2.1.4 Clock Tolerance Compensation		
11.2.1.4#1	NT	Clock tolerance compensation shall not be performed.
11.2.1.5 Compliance Mode		
11.2.1.5#1	NT	Compliance Mode shall not be supported.
11.1.1.6 Clock Power Management		
11.2.1.6#1	NT	Clock Power Management shall not be supported.
11.2.2 PCIe Data Link Layer		
11.2.2#1	NT	An internal PCIe Port shall implement a PCIe Data Link Layer as defined in the PCIe Specification.
11.2.3 PCIe Transaction Layer		
11.2.3#1	TD 11.10	Max Payload Size of 128B
11.2.3#2	TD 11.6	Support the PCIe Latency Tolerance Reporting (LTR) mechanism. The Latency Tolerance Reporting LTR Capability shall be implemented in the PCIe Upstream Port.
11.2.3#3	TD 11.7	Support PCIe hot-add and hot-removal (“hot-plug”).
11.2.3#4	TD 11.8	In a USB4 Hub, the Transaction Layer shall additionally support Access Control Services (ACS).

11.2.3#5	TD 11.9	In a USB4 Hub, the Transaction Layer shall additionally support Flattening Portal Bridge (FPB).
11.2.5 Precision Time Management (PTM) Mechanism		
11.2.5#1	TD 11.12	A USB4 Hub shall support PTM as defined in the PCIe Specification with the modifications in this section.
11.2.5.1 Parameter Generator		
11.2.5.1#1	TD 11.12	The following Routers shall act as a Parameter Generator: A Host Router with its PTM function enabled; A Device Router with its PTM function enabled and the Root Select bit in its PTM Control Register set to 1b.
11.2.5.1#2	NT	A Parameter Generator shall calculate the TMU_to_PTM Parameters as defined in Section 11.1.5.3.1.
11.2.5.1#3	NT	Instead of the PTM Master Time and Propagation Delay fields defined in the PCIe Specification, a Parameter Generator shall include the most recent TMU_to_PTM Parameters in the PTM ResponseD Message as depicted in Figure 11-2.
11.2.5.2 Parameter Consumer		
11.2.5.2#1	NT	A Device Router shall act as Parameter Consumer if its PTM function is enabled and the Root Select bit in its PTM Control Register is set to 0b.
11.2.5.2#2	TD 11.12	When sending a PTM ResponseD Message through a Downstream PCIe Adapter Port, a Parameter Consumer shall use the PTM ResponseD Message format defined in Figure 11-2.
11.2.5.2#3	NT	The TMU_to_PTM Parameters in the ResponseD Message shall be the same as the last TMU_to_PTM Parameters received on the Upstream PCIe Adapter Port.
11.2.5.2#4	TD 11.12	When sending a PTM ResponseD Message to a Native Downstream PCIe Port, a Parameter Consumer shall use the PTM ResponseD Message format defined in the PCIe Specification.
11.2.5.2#5	NT	The Parameter Consumer shall calculate the PTM Master Time for the PTM ResponseD Message as defined in Section 11.2.5.3.2.
11.1 PCIe Adapter Layer		
11.1.1 Encapsulation		
11.1.1#1	TD 11.13 BCP	The PCIe Adapter Layer shall encapsulate the following PCIe constructs in Tunneled Packets: Transaction Layer Packets (TLP); Data Link Layer Packets (DLLP); Ordered Sets; Out-of-band events.

11.1.1#2	TBD	A PCIe Adapter Layer shall not encapsulate Idle data Symbols into Tunneled Packets.
11.1.1#3	TD 11.13 BCP	A TLP or a DLLP shall fit into a single Tunneled Packet
11.1.1#4	TD 11.13 BCP	A Tunneled Packet may contain a single TLP or DLLP, or it may contain a DLLP followed by a TLP or DLLP. It shall not contain any other TLP/DLLP combinations.
11.1.1#5	TD 11.13 BCP	Each Ordered Set shall be encapsulated into a separate Tunneled Packet.
11.1.1#6	TD 11.13 BCP	Each PCIe out-of-band event shall be encapsulated into a separate Tunneled Packet.
11.1.1#7	TD 11.13 BCP	The order of bytes and bits in the Tunneled Packet shall be identical to the original PCIe construct. The least-significant byte of the encapsulated construct is mapped to B0 in the Tunneled Packet Payload (see Figure 4-17). Bit 7 in each byte of the encapsulated construct is mapped to bit 7 in respective byte of the Tunneled Packet Payload.
11.1.1#8	TD 11.13 BCP	Table 11-2 defines the PDF values that shall be used for each type of PCIe construct.
11.1.1#9	TD 11.13	If a PCIe Adapter Port receives a Tunneled Packet with a Rsvd PDF value, it shall discard the Tunneled Packet and shall not send any Packets in response.
11.1.1.1 PCIe TLP and DLLP		
11.1.1.1#1	NT	A PCIe Adapter Port shall not discard a PCIe TLP or DLLP due to lack of credits in the USB4 fabric. When credits are not available, the Router shall queue the PCIe TLP and shall transport it once sufficient credits become available.
11.1.1.1#2	TD 11.13	When a PCIe Adapter Layer receives a Tunneled Packet with a pre-header that does not match any of the pre-headers defined in this section, it shall discard the packet and report the mismatch as a PCIe Receiver Error to the internal PCIe Port.
11.1.1.1.1 TLP Encapsulation		
11.1.1.1.1#1	NT	A PCIe Adapter Port shall not send a Tunneled Packet for the following: A Nullified TLP; A Truncated TLP; A Truncated DLLP.

11.1.1.1.1#2	TD 11.13 BCP	As shown in Figure 11-4, before encapsulation into a Tunneled Packet, a PCIe Adapter Layer shall: 1. Truncate a TLP by removing the STP Symbol, four leading Reserved bits, and the END Symbol; 2. Add the TLP pre-header defined in Table 11-3.
11.1.1.1.2 DLLP Encapsulation		
11.1.1.1.2#1	TD 11.13 BCP	Before encapsulating a DLLP into a Tunneled Packet, a PCIe Adapter Layer shall: 1. Truncate a DLLP by removing the SDP Symbol and the END Symbol; 2. Add a DLLP pre-header of 0FACh to a DLLP as shown in Figure 11-6.
11.1.1.1.3 Mixed TLP/DLLP Encapsulation		
11.1.1.1.3#1	TD 11.13 BCP	When a Tunneled Packet contains a DLLP followed by a TLP or DLLP, each DLLP or TLP shall contain its own pre-header.
11.1.1.2 PCIe Ordered Sets		
11.1.1.2.1 Training Sequence (TS) Ordered Sets		
11.1.1.2.1#1	TD 11.5 TD 11.6	When a PCIe Adapter Layer receives one or more identical TS1 Ordered sets in a row from the internal PCIe Port, it shall transmit 16 copies of the TS1 Ordered set before it transmits another Tunneled PCIe Packet. The PCIe Adapter Layer may transmit more than 16 TS1 Ordered sets before transmitting a Tunneled PCIe Packet.
11.1.1.2.1#2	TD 11.5 TD 11.6	When a PCIe Adapter Layer receives one or more identical TS2 Ordered sets in a row from the internal PCIe Port, it shall transmit 16 copies of the TS2 Ordered set before it transmits another Tunneled PCIe Packet. The PCIe Adapter Layer may transmit more than 16 TS2 Ordered sets before transmitting a Tunneled PCIe Packet.
11.1.1.2.1#3	TD 11.5 TD 11.6	A PCIe Adapter Layer shall only transmit TS Ordered Sets that target Lane 0. TS Ordered Sets that target a non-zero Lane shall be discarded and shall not be send over the USB4 fabric.
11.1.1.2.1#4	TD 11.5 TD 11.6	A PCIe Adapter Layer shall modify a TS Ordered Set as defined in Table 11-4.
11.1.1.2.1#5	NT	Upon receiving a TS Ordered Set from the Transport Layer, a PCIe Adapter Layer shall transfer the TS Ordered Set to the internal PCIe Port.
11.1.1.2.2 Electrical Idle Ordered Sets (EIOS)		
11.1.1.2.2#1	TD 11.5 TD 11.7	When a PCIe Adapter Layer receives an Electrical Idle Ordered Set (EIOS) from the internal PCIe Port, it shall send two consecutive EIOS Tunneled Packets over the USB4 fabric.

11.1.1.2.2#2	TD 11.5 TD 11.7	An EIOS shall be encapsulated in a Tunneled Packet with payload as defined in Table 11-5.
11.1.1.2.2#3	NT	A PCIe Adapter Layer that receives an EIOS Tunneled Packet shall: 1. Transfer the EIOS to the internal PCIe Port; 2. Indicate Rx Electrical Idle to the internal PCIe Port.
11.1.1.3 Electrical Idle State		
11.1.1.3#1	TD 11.7	Upon detecting that a PCIe Physical Layer Logical sub-block is in Electrical Idle state, a PCIe Adapter Layer shall send at least 3 Electrical Idle State Tunneled Packets.
11.1.1.3#2	TD 11.7	The payload for an Electrical Idle State Tunneled Packet shall consist of one DW that contains a value of 0000 0000h.
11.1.1.3#3	NT	A PCIe Adapter Layer that receives an Electrical Idle State Tunneled Packet shall indicate Rx Electrical Idle to the internal PCIe Port.
11.1.1.3#4	NT	When a PCIe Adapter Layer receives a Tunneled Packet that is not an Electrical Idle State Tunneled Packet or an EIOS Tunneled Packet, it shall stop indicating Rx Electrical Idle to the internal PCIe Port.
11.1.1.4 PERST		
11.1.1.4.1 PERST Tunneled Packets		
11.1.1.4.1#1	NT	A Router shall send PERST Active and PERST Inactive packets only from a Downstream PCIe Adapter Port.
11.1.1.4.1#2	TD 11.14	The payload for a PERST Active Tunneled Packet and a PERST Inactive Tunneled Packet shall consist of one DW that contains a value of 0000 0000h.
11.1.1.4.2 PERST Propagation		
11.1.1.4.2.1 PERST Activation		
11.1.1.4.2.1#1	TD 11.14	Upon detecting an assertion of PERST#, a Host Router shall: 1. Discard any queued Tunneled Packet in the PCIe Adapter Layer; 2. Send at least three PERST Active Tunneled Packets on all Downstream PCIe Adapter Ports that have the Path Enable bit set to 1b.
11.1.1.4.2.1#2	TD 11.14	When a Device Router receives a PERST Active Tunneled Packet it shall: 1. Discard any Tunneled Packets that are queued in a PCIe Adapter Layer; 2. Send at least 3 PERST Active Tunneled Packets on all Downstream PCIe Adapter Ports that have the Path Enable bit set to 1b. The Router shall also assert PERST# on all physical PCIe ports and to the internal PCIe Port.

11.1.1.4.2.1#3	NT	While PERST# is asserted, a Downstream PCIe Adapter Layer shall discard any PCIe Tunneled Packets it receives.
11.1.1.4.2.2 PERST Inactivation		
11.1.1.4.2.2#1	TD 11.14	Upon detecting a de-assertion of PERST#, a Host Router shall send at least 3 PERST Inactive Tunneled Packets on all Downstream PCIe Adapter Ports that have the Path Enable bit set to 1b.
11.1.1.4.2.2#2	TD 11.14	After receiving a PERST Active Tunneled Packet, if a Device Router receives any PCIe Tunneled Packet other than a PERST Active Tunneled Packet on its Upstream PCIe Adapter Port, it shall: Send at least 3 PERST Inactive Tunneled Packets on all Downstream PCIe Adapter Ports that have the Path Enable bit set to 1b; De-assert PERST# on all PCIe physical ports and to the internal PCIe Port.
11.1.1.4.2.2#3	NT	After PERST# is de-asserted, a Downstream PCIe Adapter Layer shall not forward to the internal PCIe Port any Ordered Sets, packets, or events that were received before or during PERST# assertion.
11.1.2 USB4 Hot-Plug		
11.1.2#1	TD 11.14	When a Device Router is hot-plugged, the Upstream Adapter Port in the hot-plugged Router shall maintain the internal PCIe Port in PCIe Warm Reset.
11.1.2#2	TD 11.17	The Device Router shall maintain the Warm Reset until either a PERST Inactive Tunneled Packet or a PCIe TS Ordered Set is received by the Upstream Adapter Port.
11.3 Paths		
11.3#1	NT	A PCIe Adapter Layer shall put HopID = 8 in the header of an outgoing Tunneled Packet before handing it off to the Transport Layer for routing
11.3.1 Path Set-Up		
11.3.1#1	TBD	Before setting up a Path, the Router does not indicate in-band presence to the Internal PCIe Port. The internal PCIe Port LTSSM is in the Detect state.
11.3.1#2		Deprecated.
11.3.1#3	TBD	When the Path Enable bit is set to 1b, a Router shall indicate in-band presence to the internal PCIe Port.
11.3.1#4	TBD	The PCIe Adapter Layer shall also enable sending of PCIe Tunneled Packets to the Transport Layer.

11.3.1#5	NT	When an internal PCIe Port detects an in-band presence, it shall: Transition its LTSSM to the Polling state; Generate a PCIe interrupt to indicate a hot plug event to software.
11.3.2 Path Tear-Down		
11.3.2#1	TD 11.20	When a Router detects a disconnect event on a Downstream Facing USB4 Port, it shall: Set the Path Enable bit to 0b in the PCIe Adapter Port Configuration Capability of the PCIe Adapter Port associated with the USB4 Port via the Router's Routing Tables.
11.3.2#2	TD 11.20	When the Path Enable bit is set to 0b in its PCIe Adapter Configuration Capability, a PCIe Adapter shall: Disable sending of PCIe Tunneled Packets from the PCIe Adapter Layer to the Transport Layer; If the PCIe Adapter is a Downstream PCIe Adapter, clear the In-band Presence 1 indication to the internal PCIe port; If the PCIe Adapter is an Upstream PCIe Adapter, drive PERST# to default as defined in Section 11.1.1.4.2.
11.3.2#3	NT	When an internal PCIe Port detects that the in-band presence indicator is cleared, it shall: Transition its LTSSM to the Recovery state followed by transition to the Detect state. It is recommended that the LTSSM not wait the full amount of time defined in the PCIe Specification before transitioning to the Detect state; Generate a PCIe interrupt to indicate a hot removal event to software.

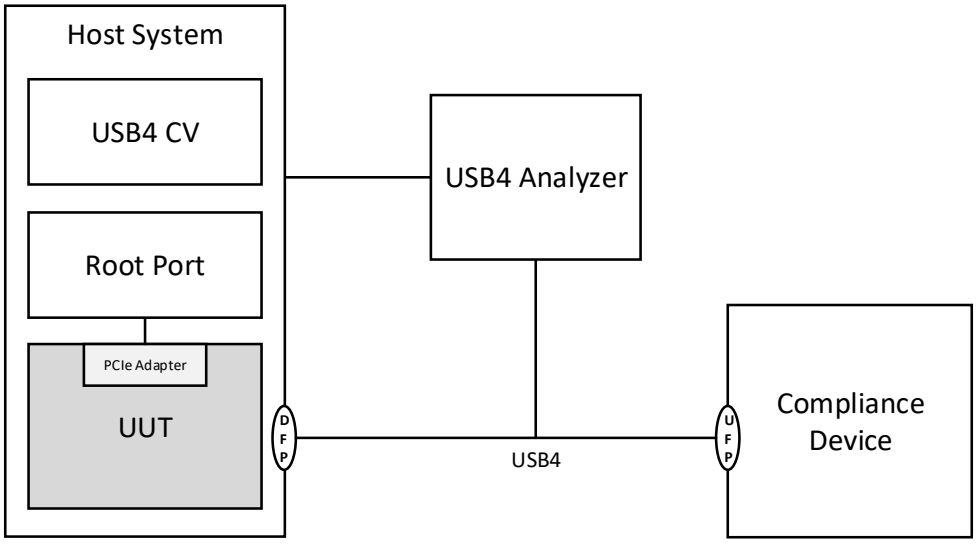
Test Setups

Host

This section describes the test setup for a Host Router.

AN_HOST_DFP1—PCIE_01

- Vendor provides the host system for the UUT with:
  - USB4 CV installed
  - The relevant PCIe-related capabilities (PTM, ASPM, etc.) enabled in the BIOS/OS as required for testing
- A KG USB4 Device with a known PCIe endpoint is connected downstream.
- A USB4 Analyzer is connected between the UUT an KG USB4 Device.

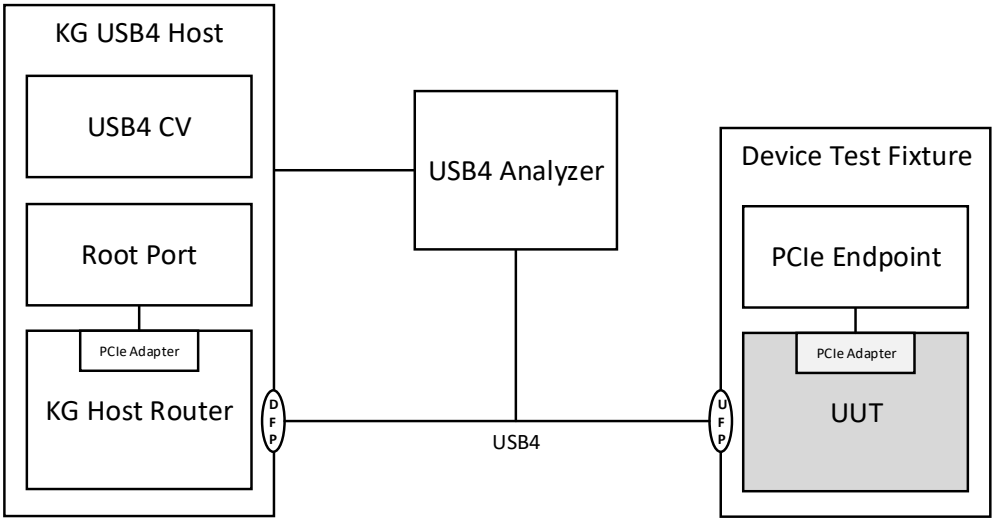


Hub

This section describes the test setups for a Hub Router (i.e. a Device Router with one or more DFP).

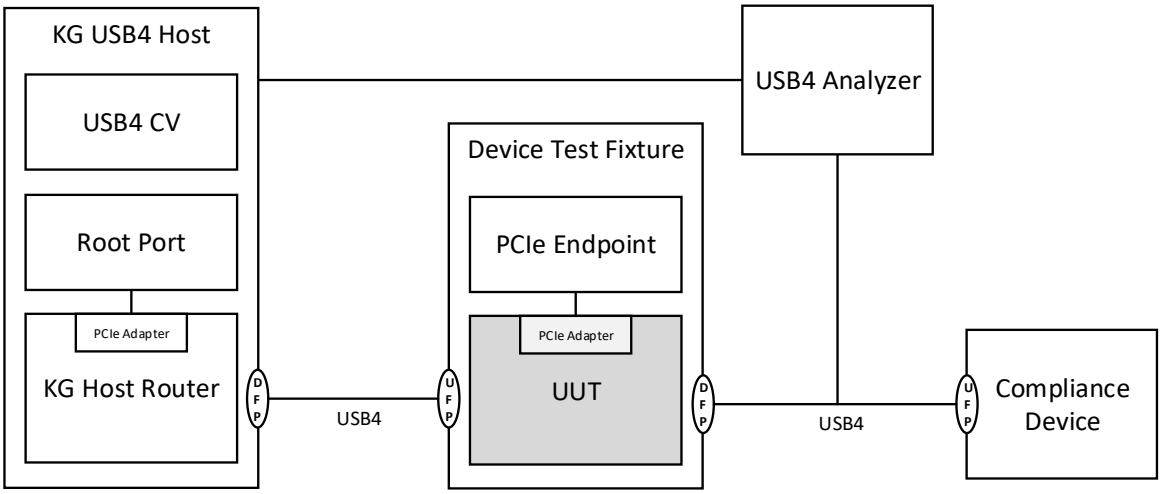
AN_HUB_UFP1—PCIE_01

- Vendor provides device test fixture for the UUT with a x8 PCIe slot.
- For an embedded PCIe endpoint, the vendor provides a Windows driver/utility capable of running controlled Tx/Rx traffic on the device.
- A KG USB4 Host is connected to the UUT.
- A USB4 Analyzer is connected between the KG USB4 Host and UUT.



AN_HUB_DFP1—PCIE_02

- Vendor provides device test fixture for the UUT with a x8 PCIe slot.
- In case of an embedded PCIe endpoint the vendor provides a Windows driver/utility capable of running controlled Tx/Rx traffic on the device.
- A known host system running Windows OS with a KG USB4 Host will connect to the UUT.

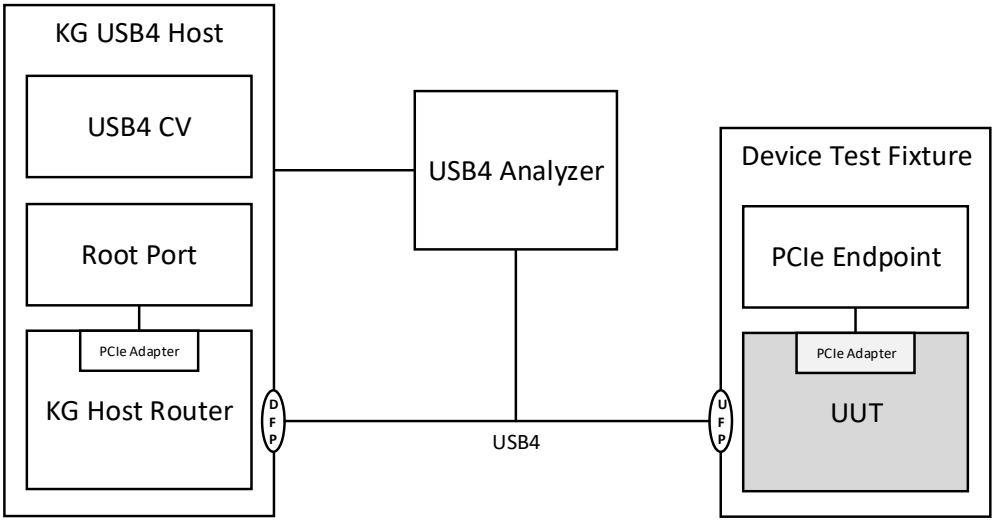


Peripheral Device

This section describes the test setup for a Peripheral Device Router (i.e. a Device Router that does not have DFP).

AN_DEV_UFP1—PCIE_01

- Vendor provides device test fixture for the UUT with a x8 PCIe slot.
- For an embedded PCIe endpoint, the vendor provides a Windows driver/utility capable of running controlled Tx/Rx traffic on the device.
- A KG USB4 Host is connected to the UUT.
- A USB4 Analyzer is connected between the KG USB4 Host and UUT.



Traffic Generation Control

Note: This section only applies to USB4 hubs and devices that contain an embedded PCIe endpoint.

In order to test the USB4 PCIe Tunnel with PCIe traffic, a Vendor shall supply the following Batch file (.bat), which can control the PCIe traffic generation from the Vendor DUT:

File name:

Vendor's choice. On relevant tests, pop-up windows will be used to choose the file location.

Parameters:

1. -start : To start traffic generation.
2. -direction <0 / 1> : To start traffic in Tx OR Rx direction. Mandatory in case of start.
3. -dump : Dump file location, Created by USB4CV software. Used by the batch file to write errors.
4. -interval : Time[ms] interval between each packet.
5. -stop : To stop traffic generation.

Format:

1. To start traffic in Tx direction:
   gen.bat -start -type 0 -dump "C:\\Users\\Public\\USB4\\Traffic\\trafficDump.txt"
2. To start traffic in Rx direction:
   gen.bat -start -type 1 -dump "C:\\Users\\Public\\USB4\\Traffic\\trafficDump.txt"
3. To start traffic in Tx direction with 1ms intervals:
   gen.bat -start -type 0 -interval 1 -dump "C:\\Users\\Public\\USB4\\Traffic\\trafficDump.txt"
4. To stop traffic:
   gen.bat -stop

Status:

If the dump file remains empty, the traffic generation is assumed to be without errors. If the dump file is not empty, the traffic generation is assumed to have errors, which are described in the dump file.

Test Descriptions

Unless specified otherwise, the tests in this section are performed in USB4 mode where all connected USB4 Ports negotiate and enter USB4 operation as described in the USB Type-C Specification and the USB PD Specification. USB4 CV enumerates the Router as a USB4 Connection Manager.

Tests are performed at the highest signaling speed that the UUT supports. Lanes are bonded unless specified otherwise. When Lanes are bonded, the configuration Space of the Lane 0 Adapter is used to perform the tests.

Unless otherwise noted, a test will timeout if it takes more than 500ms to go from one step to the next step. It is a test failure if a test times out.

Background Check Procedure

The test steps in this section are performed by the Analyzer in the background while the rest of the tests in this document are performed.

1. Parse each USB4 Transaction – Check for correct header and identify PCIe Tunneled Packets
2. Parse each PCIe Transaction:
    a. For TLP Check Type, LEN, CHK fields and END symbol
    b. For DLLP check SDP and END symbol
    c. For OS check TS fields – Link Number, Lane Number, N_FTS, Data rate identifier, Training control
    d. For EIOS, check for correct symbols
    e. Identify PERST#
3. For TLP's DLLP's – check correctness at the PCIe level as defined by the PCIe 4.0 specification

PCIe Tunneling Tests

TD 11.1 Product Structure Test

A. Purpose:

- Verify that the UUT includes a PCIe switch or endpoint

B. Asserts:

- 11#1, 11#3, 11#5

C. Equipment:

- USB4 CV

D. Procedure:

Case 1 – USB4 Host

1. Power on the UUT
2. Enumerate the UUT on the host system
3. Verify that the UUT contains either a PCIe switch or a root port

Case 2 – USB4 Peripheral Device

1. Connect the UUT to the host system
2. Enumerate the UUT on the PCIe bus through the Host Router
3. Verify that the UUT contains a PCIe switch and/or a PCIe endpoint

Case 3 – USB4 Hub

1. Connect the UUT to the host system
2. Enumerate the UUT on the PCIe bus through the Host Router
3. Verify that the UUT contains a PCIe switch

TD 11.2 Supported Tunnel Speed Test

A. Purpose:
   - Verify that the UUT only supports GEN1 speed when tunneling PCIe

B. Asserts:
   - 11.2.1#1

C. Equipment:
   - USB4 CV

D. Procedure:
   1. Connect the UUT
   2. Enumerate the UUT
   3. For each PCIe Port on the UUT:
      a. Read the Link Capabilities register from PCIe configuration space
      b. Verify that the max link speed field is GEN1

TD 11.3 Unsupported LTSSM States Test

Note: This test is only performed once on the UUT.

A. Purpose:
   - Verify that the UUT does not support non-required LTSSM states when tunneling PCIe

B. Asserts:
   - 11.2.1.2#2

C. Equipment
   - USB4 CV

D. Procedure:
   1. Connect the UUT
   2. Enumerate the UUT
   3. For each PCIe Port on the UUT:
      a. Read the ASPM support bits from the Link Capabilities register
      b. Verify that L0s is not supported
      c. Verify that L1 PM sub-states capability does not exist on the PCIe port

TD 11.4 Hot Reset Test

A. Purpose:
   - Verify that the UUT handles Hot Reset (secondary bus reset) correctly over a PCIe tunnel

B. Asserts:
   - 11.2#1

C. Equipment:
   - Analyzer
   - USB4 CV
   - PCIe access SW

D. Procedure:
   1. Connect the UUT
   2. Enumerate the UUT
   3. Disable hot plug interrupts on the PCIe Downstream port above the UUT:
      a. Hot plug interrupts are disabled by zeroing the Presence Detect Changed Enable, Hot-Plug Interrupt Enable and Data Link Layer State Changed Enable bits on the slot control register
   4. From the PCIe Downstream port above the UUT, perform a secondary bus reset from the bridge control register
   5. Verify that the UUT is in the reset state and not responding to accesses
   6. Exit hot reset
   7. Verify that the UUT PCIe Upstream port is responding to accesses
   8. Verify that the configuration space was reset by checking the Command (CMD offset 0x4) MMIO and BME bits and the Bus register (offset 0x18) primary, secondary, and subordinate fields
   9. Reconfigure the PCIe port bus range through the PCIe access SW
   10. Verify the hot reset propagation – that the ports below were also reset
   11. For every PCIe downstream port in the UUT:
      a. Connect and enumerate an endpoint below the port
      b. Disable hot plug interrupts as specified above
      c. Perform hot reset from the port's bridge control register
      d. Verify that the upstream port below was reset
      e. Check the TS1/TS2 structure with the Analyzer

TD 11.5 Link Retrain Test

A. Purpose:
- Verify that the UUT handles link retrain correctly over a PCIe tunnel.

B. Asserts:
- 11.2#1, 11.1.1.2.1#1, 11.1.1.2.1#2, 11.1.1.2.1#3, 11.1.1.2.1#4, 11.1.1.2.2#1, 11.1.1.2.2#2

C. Equipment:
- Analyzer
- USB4 CV

D. Procedure:
1. Connect the UUT
2. Enumerate the UUT
3. Disable hot plug interrupts on the PCIe Downstream port above the UUT
    a. Hot plug interrupts are disabled by zeroing the Presence Detect Changed Enable, Hot-Plug Interrupt Enable and Data Link Layer State Changed Enable bits on the slot control register
4. For an upstream port, perform link retrain from the PCIe Downstream port above the UUT
5. Note: This is done by setting the retrain link bit in the link control register
6. Verify that the PCIe link goes down and trains back up to L0
7. Check TS1/TS2 structure with the analyzer
8. Verify that at least 16 replicas of TS1 and TS2 are generated by the UUT
9. Verify that the port is accessible on the PCIe bus
10. For every PCIe downstream port in the UUT:
    a. Connect and enumerate an endpoint below the port
    b. Disable hot plug interrupts as specified above
    c. Perform link retraining from the port's link control register
    d. Verify that the link goes down and trains back up to L0
    e. Check TS1/TS2 structure with the analyzer
    f. Verify that at least 16 replicas of TS1 and TS2 are generated by the UUT
    g. Verify that the upstream port below is accessible
    h. Verify EIOS (Electrical Idle Ordered Set) structure
11. Verify that two consecutive EIOS are sent over the tunnel

TD 11.6 Link Disable Test

A. Purpose:
   - Verify that the UUT handles link disable correctly over a PCIe tunnel

B. Asserts:
   - 11.2#1, 11.1.1.2.1#1, 11.1.1.2.1#2, 11.1.1.2.1#3, 11.1.1.2.1#4

C. Equipment:
   - Analyzer
   - USB4 CV

D. Procedure:
   1. Connect the UUT
   2. Enumerate the UUT
   3. Disable hot plug interrupts on the PCIe Downstream port above the UUT
      a. Hot plug interrupts are disabled by zeroing the Presence Detect Changed Enable, Hot-Plug Interrupt Enable and Data Link Layer State Changed Enable bits on the slot control register
   4. For an upstream port, perform link disable from the PCIe Downstream port above the UUT
   5. Note: This is done by setting the link disable bit in the link control register
   6. Verify that the link went to disabled state and the UUT is not responding to access
   7. Set the link disable bit to 0
   8. Verify that the PCIe link trains back up to L0
   9. Check TS1/TS2 structure with the analyzer
   10. Verify that at least 16 replicas of TS1 and TS2 are generated by the UUT (upstream port)
   11. Verify that the UUT is accessible on the PCIe bus
   12. For every downstream PCIe port in the UUT:
      a. Connect and enumerate an endpoint below the port
      b. Disable hot plug interrupts as specified above
      c. Perform link disable from the port's link control register
      d. Verify that the link went to disabled state by reading the LTSSM
      e. Verify that the link goes down and trains back up to L0
      f. Check TS1/TS2 structure with the analyzer
      g. Verify that at least 16 replicas of TS1 and TS2 are generated by the UUT (downstream port)
      h. Verify that the upstream port below is accessible

TD 11.7 ASPM L1 Traffic Test

A. Purpose:
- Verify that the UUT PCIe link is correctly entering and exiting ASPM L1 on a supporting tunnel

B. Asserts:
- 11.2#1, 11.2.1.2#1, 11.1.1.2.2#1, 11.1.1.2.2#2, 11.1.1.3#1, 11.1.1.3#2

C. Equipment
- Analyzer
- USB4 CV
- SW capable of running controlled Tx/Rx traffic over the device

D. Repetitions
- Repeat for each USB4 Port that supports PCIe Tunneling

E. Procedure:
1. Connect the UUT
2. Enumerate the UUT
3. Read the link capabilities register and make sure that ASPM L1 is supported
4. Configure ASPM L1 in the link control register over all the supporting tunneled PCIe links
5. Verify entry to L1 state in the LTSSM field in the adapter register
6. Verify by analyzer:
    a. DLLP L1 entry handshake is as defined by the PCIe 4.0 specification
    b. Verify EIOS (Electrical Idle Ordered Set)
        i. EIOS structure
        ii. Two consecutive EIOS are sent over the tunnel
    c. Verify EIDLE (Electrical Idle Event)
        i. EIDLE structure is as defined in the USB4 specification
        ii. At least three consecutive EIDLE events are sent over the tunnel
7. Start burst traffic to the device for 1 minute
    a. For a host Router or device/hub Router with a PCIe slot, connect a NIC with L1 support and use file transfer or PINGs to create the burst traffic
    b. For a device Routers with an embedded PCIe endpoint, use the Traffic Generation Control batch file provided by the device Router vendor to generate traffic with 1ms intervals.
8. Check entry to L1 and exit from L1 during the traffic
9. Stop the traffic
10. Verify that the link has entered L1
11. Repeat for Tx and Rx traffic (Tx is egress traffic and Rx is ingress traffic)

12. For a Host Router or a Device Router that provides an open PCIe slot – connect a PCIe device capable of initiating traffic to the host and repeat with traffic from device to host
13. For a Device Router that supports TBT3-Compatibility mode:
    a. Connect the UUT to a TBT3 Router with USB4 Sideband Channel Support enabled
    b. Verify that TBT3 mode was established
    c. Enable ASPM L1 in the link control registers
    d. Verify entry to L1 in the LTSSM registers as above
    e. Connect the UUT to a TBT3 Router with USB4 Sideband Channel Support disabled
    f. Verify that TBT3 mode was established
    g. Enable ASPM L1 in the link control registers
    h. Verify that the link did not enter L1

TD 11.8 PM L1 Nak Response Test

A. Purpose:
- Verify correct behavior of the PCIe port when sending/receiving PM_Active_State_Nak DLLP

B. Asserts:
- 11.2.1.3#1

C. Equipment
- Analyzer
- USB4 CV

D. Repetitions:
- Repeat for each USB4 Port that supports PCIe Tunneling

E. Procedure:
1. Connect the UUT
2. Enumerate the UUT
3. Enable L1 on the UUT PCIe upstream port (but not on the opposite downstream port)
4. Check via analyzer trace that PM_Active_State_Request are generated by the upstream port and answered by PM_Active_State_Nak DLLP
5. Make sure that no more than 10 PM_Active_State_Request DLLP are sent by the upstream port after receiving the first Nak
6. Enable L1 on the downstream port
7. Verify that L1 is reached in the LTSSM field in the adapter register and by analyzer
8. Access the PCIe endpoint over the link 10 times every 1ms
9. Verify that L1 state is reached after each access
10. Verify by analyzer:
    a. DLLP L1 entry handshake as defined by the PCIe 4.0 specification
    b. Verify EIOS (Electrical Idle Ordered Set) structure
11. Verify that two consecutive EIOS are sent over the tunnel

Link Initialization Tests

TD 11.9 L2 link State Test

A. Purpose:
   - Verify that the UUT enters and exits L2 properly

B. Asserts:
   - 11.2#1

C. Equipment:
   - USB4 analyzer
   - USB4 CV
   - PCIe access SW

D. Procedure:
   1. Connect UUT
   2. Enumerate UUT
   3. Initiate L2 entry process from the chipset by using the PCIe access SW
   4. Verify correct entry to L2 by checking the chipset L2 control register and verifying:
      a. PME_TO and PME_TO_ACK messages captured by the USB4 analyzer
      b. L23 link entry handshake as defined by the PCIe 4.0 specification
   5. Exit L2
   6. Verify that the PCIe link reaches L0
   7. Run some traffic over the link through the PCIe access SW tool

TD 11.10 Max Payload Size Support Test

A. Purpose:
   - Verify that the UUT ports support only 128B max payload size

B. Asserts:
   - 11.2.3#1

C. Equipment:
   - USB4 CV

D. Procedure:
   1. Connect UUT
   2. Enumerate the UUT
   3. For each embedded PCIe device in the UUT:
      a. Read the device capabilities register
      b. Verify that the Max_Payload_Size supported field declares 128B support

TD 11.11 PCIe Stress Traffic Test

A. Purpose:
- Verify that the UUT can pass high BW PCIe traffic without recoveries and errors

B. Asserts:
- 11.2#1

C. Equipment
- USB4 CV
- Traffic utility – Iometer or vendor provided (in case the UUT is a device)
- USB4 analyzer

D. Procedure:

Case 1 – Host Router

1. Connect UUT to a KG USB4 Device
2. Enumerate the UUT
3. Pass traffic Tx/Rx traffic over the endpoint through the utility for 1 minute
4. Verify no hangs – system freeze or traffic stops
5. Verify no PCIe link recoveries on the tunnel through the USB4 analyzer
6. Repeat with a full depth Re-timer channel

Case 2 – Device Router

1. Connect UUT to a KG USB4 Host and let it be enumerated by the system
2. Pass traffic Tx/Rx traffic over the endpoint through the utility for 1 minute
3. Verify no hangs
4. Verify no recoveries
5. Verify no errors on the following bits of the advanced error reporting capability of the routers:
    a. Uncorrectable error register – all error bits
    b. Correctable error register – Bad TLP, Bad DLLP, Replay_Num Rollover
6. Repeat with a full depth Re-timer channel

Lane State Tests

TD 11.12 PTM Test

A. Purpose:
   - Verify the UUT PTM functionality. Mandatory for a USB4 hub. Optional otherwise

B. Asserts:
   - 11.2.5#1, 11.2.5.1#1, 11.2.5.2#2, 11.2.5.2#4

C. Equipment:
   - USB4 CV
   - USB4 analyzer

D. Procedure:
   1. Connect the UUT
   2. Enumerate the UUT
   3. Read the PTM capability structure and make sure it complies with the PCIe 4.0 specification
   4. Enable PTM by setting the PTM enable bit to 1 from the top of the tree to the bottom
   5. Verify through the USB4 analyzer that the PTM Msg and MsgD packet exchange occurs as described in the PCIe 4.0 specification

TD 11.13 PCIe Transactions Encapsulation Test

A. Purpose:

- Verify that the various PCIe TLP and DLLP packets are encapsulated correctly into USB4 packets

B. Asserts:

- 11.1.1#1, 11.1.1#3, 11.1.1#4, 11.1.1#5, 11.1.1#6, 11.1.1#7, 11.1.1#8, 11.1.1#9, 11.1.1.1#2, 11.1.1.1.1#2, 11.1.1.1.2#1, 11.1.1.1.3#1

C. Equipment:

- Exerciser
- USB4 CV
- SW for running controlled Tx/Rx traffic over the device
- USB4 Analyzer

D. Procedure:

Part 0 – Setup

1. Connect the UUT
2. Enumerate the UUT

Part 1 – TLP Encapsulation

3. Generate MRd, Mwr, CFGrd, CFGwr TLP's through the PCIe access and traffic SW
4. Check each TLP type structure with the analyzer as in the Background Check Procedure
5. Generate error TLP packets through the exerciser:
    a. Reserved PDF
    b. Type error
    c. Length error
    d. CHK error
6. Check for each that the receiver error bit in the correctable error status register is set

Part 2 – DLLP Encapsulation

7. Correct generation of DLLP's is tested by performing the Background Check Procedure
8. Generate error DLLP prefix through the exerciser
9. Verify that the receiver error bit in the correctable error status register is set

Part 3 – Mixed encapsulation

10. Generate MRd, Mwr, CFGrd, CFGwr TLP's through the PCIe access and traffic SW. Verify the following combinations in the analyzer trace:
    a. DLLP followed by DLLP in the same USB4 packet
    b. DLLP followed by TLP in the same USB4 packet

TD 11.14 PCIe Reset (PERST) Event Test

A. Purpose:

- Verify that the PERST event is being tunneled correctly over the PCIe tunnel

B. Asserts:

- 11.1.1.4.1#2, 11.1.1.4.2.1#1, 11.1.1.4.2.1#2, 11.1.1.4.2.2#1, 11.1.1.4.2.2#2, 11.1.2#1

C. Equipment

- USB4 Analyzer
- USB4 CV
- Scope\ Voltage meter\ GPIO monitor

D. Procedure:

Case 1 – Host Router

1. Connect UUT
2. Enumerate the UUT
3. Cause PERST# assertion event
4. Check PERST active message structure as defined by the USB4 specification
5. Check at least 3 consecutive PERST active packets
6. Repeat for PERST# de-assertion event

Case 2 – Device Router

1. Connect UUT and let it be enumerated by the system
2. Cause PERST# event
3. Check PERST structure
4. Check at least 3 consecutive PERST packets
5. Check PERST propagation on physical ports
6. Verify that the RST bit on the relevant PCIe adapter (ADP_PCIE_CS_0[19]) is set
7. Repeat for PERST# de-assertion event
8. Verify that the RST bit on the relevant PCIe adapter (ADP_PCIE_CS_0[19]) is cleared

TD 11.15 PCIe Traffic with CLx Test

A. Purpose:
   - Verify that the UUT PCIe link is correctly entering and exiting ASPM L1 when the USB4 link is entering and exiting CLx states

B. Asserts:
   - TBD

C. Equipment
   - Analyzer
   - USB4 CV
   - SW for running controlled Tx/Rx traffic over the device

D. Procedure:
   1. Connect the UUT to a USB4 Router with a cable that supports CLx
   2. Enumerate the UUT
   3. Verify that the LCL bit is set
   4. Check the CLx support bits on the LANE_ADP_CS_1 register for the lowest supported CLx state
   5. Configure ASPM L1 in the link control register over all the supporting tunneled PCIe links
   6. Make sure that LTR is disabled
   7. Verify entry to L1 state in the LTSSM field in the adapter register
   8. Verify by analyzer:
      a. DLLP L1 entry handshake as defined by the PCIe 4.0 specification
      b. Verify EIOS (Electrical Idle Ordered Set):
         i. EIOS structure
         ii. Two consecutive EIOS sent over the tunnel
      c. Verify EIDLE (Electrical Idle Event):
         i. EIDLE structure as defined in the USB4 specification
         ii. At least three consecutive EIDLE events sent over the tunnel
   9. Start burst traffic with 1ms intervals to the device for 1 minute
   10. Check entry to L1 and exit from L1 during the traffic
   11. Check entry to CLx on the USB4 link
   12. Stop the traffic
   13. Verify that the PCIe link has entered L1
   14. Verify that the USB4 link has entered CL2
   15. Repeat for Tx and Rx traffic

16. For a UUT with a PCIe slot:
    a. Connect a device with a low LTR value (few µs)
    b. Make sure LTR is enabled
    c. Verify that the LTR message is transmitted by the device
    d. Verify that the USB4 link does not enter CLx
    e. Connect a device with a high LTR (few ms)
    f. Verify that the LTR message is transmitted by the device
    g. Check CLx link entry on the USB4 link

TD 11.16 LTR Test

A. Purpose:
   - Verify that the UUT supports the LTR capability

B. Asserts:
   - 11.2.3#2

C. Equipment:
   - USB4 CV

D. Procedure:
   1. Connect the UUT
   2. Enumerate the UUT
   3. Perform Secondary Bus Reset from the Downstream port above the tested Upstream port on the bridge control register
   4. Read the LTR capability structure from every upstream port in the UUT and make sure it complies with the PCIe 4.0 specification

TD 11.17 Hot-Plug Support Test

A. Purpose:
   - Verify that the UUT supports hot-plug

B. Asserts:
   - 11.2.3#3, 11.1.2#2

C. Equipment:
   - USB4 CV

D. Procedure:
   1. Connect the UUT
   2. Enumerate the UUT
   3. Do not configure a PCIe tunnel
   4. Read the slot capabilities register of each USB4 link PCIe downstream port in the UUT
   5. Verify that the Hot-plug surprise and hot-plug capable bits are set
   6. Set the Presence Detect Change Enable and the Hot-Plug Interrupt Enable bits in the slot control register. Read back and Verify that these bits were written
   7. For a Device Router Verify that the upstream adapter is in a warm reset state – read the RST bit ADP_PCIE_CS_0[19]

TD 11.18 ACS Support (Hubs Only) Test

A. Purpose:
   - Verify that the UUT supports the ACS capability

B. Asserts:
   - 11.2.3#4

C. Equipment:
   - USB4 CV

D. Procedure:
   1. Connect the UUT
   2. Enumerate the UUT
   3. Read the ACS capability structure from every Downstream port in the UUT and make sure it complies with the PCIe 4.0 specification

TD 11.19 FPB Support (Hub Only) Test

A. Purpose:

- Verify that the UUT supports the FPB capability

B. Asserts:

- 11.2.3#5

C. Equipment:

- USB4 CV

D. Procedure:

1. Connect the UUT
2. Enumerate the UUT
3. Read the FPB capability structure from every PCIe port in the UUT and make sure it complies with the PCIe 4.0 specification

TD 11.20 Path Teardown Test

A. Purpose:
   - Verify that the UUT tears down the PCIe Path upon a disconnect event

B. Asserts:
   - 11.3.2#1, 11.3.2#2

C. Equipment:
   - USB4 CV

D. Procedure:
   1. Connect the UUT
   2. Enumerate the UUT
   3. Disable ASPM (ASPM Control bits on the Link Control register are zeroed on all ports)
   4. Connect a USB4 Device Router under every USB4 DFP in the UUT and let it be enumerated on the PCIe bus
   5. Disconnect the USB4 device
   6. Read the path enable bit from the relevant PCIe adapter and verify that it's cleared
   7. Verify that the LTSSM is in DETECT through the LTSSM field on ADP_PCIE_CS_0
   8. In case of a USB4 device or hub disconnect the UPF
   9. Read the path enable bit from the relevant PCIe adapter and Verify that it's cleared
   10. Verify that the LTSSM is in DETECT state
   11. Verify that the RST bit on the relevant PCIe adapter (ADP_PCIE_CS_0[19]) is cleared
   12. Tear down the PCIe path to the device from the UUT path configuration space
   13. Connect the USB4 device
   14. Set the PCIe path back up
   15. Verify that the PCIe link trains to L0