USB4™ Logical Layer
Compliance Test Specification for Router Assemblies

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Revision: 1.2

Revision History:

Revision	Issue Date	Comments
1.0	June 2020	First Release
1.1	September 2020	With corrections and clarifications.
1.2	January 2021	With corrections and clarifications.

Contents

Introduction

The tests in this specification verify that the Logical Layer of Router in a Router Assembly is compliant with the USB4™ Specification. If the Router Assembly contains one or more On-Board Re-timers, additional tests verify that the Logical Layer of the Re-timer(s) in the Router Assembly are compliant the USB4 Re-timer Specification.

Reference Documents

- Universal Serial Bus 4 (USB4™) Specification Version 1.0 with Errata and ECN through May 4, 2020 (USB4 Specification)
- USB4 Re-Timer Specification, Version 0.96, June 2020 (USB4 Re-Timer Specification)
- USB4 Connection Manager (CM) Guide, Revision 1.0, [to be published] (Connection Manager Guide)
- USB Type-C® Cable and Connector Specification, Release 2.0 (USB Type-C Specification)
- Universal Serial Bus Power Delivery Specification, Release 3.0, Version 2.0, August 2019 (USB PD Specification)

Terminology

The following table describes the terms used in this document.

Compliance Device	A KG USB4 Device that is capable of performing Transport Layer Packet loopback. The KG USB4 Device is configured by USB4 CV (when USB4 CV is upstream of the UUT) or the Exerciser (when the Exerciser is upstream of the UUT). Unless specified otherwise, the Compliance Device is configured as an ordinary KG USB4 Device. See the USB4 Connection Manager Guide for more information on how a USB4 Device is configured.
DFP	Downstream Facing Port.
Exerciser	The compliance test tool (hardware and software) that implements USB4 Port functionality and the behavior required for compliance testing.
IOP	Interop Testing. See USB4™ Interop Test Specification.
KG USB4 Device	“Known Good” USB4 Device. A USB4 Device that is known to be compliant with the USB4 Specification.
KG USB4 Host	“Known Good” USB4 Host. A USB4 Host that is known to be compliant with the USB4 Specification.
KG TBT3 Device	A Certified Thunderbolt 3 Device.
KG TBT3 Host	A Certified Thunderbolt 3 Host.
PUT	Port Under Test. The USB4 Port on a UUT that is the test point for compliance testing.
UFP	Upstream Facing Port.
USB4 CV	USB4 Command Verifier software. The software that runs compliance tests and analyzes the results.
USB4 Product	Refers to a USB4 host, USB4 hub, and/or USB4 device. Includes silicon, reference platforms, and end product.
UUT	Unit Under Test. The Router Assembly that is being tested for compliance.
VIF	Vendor Information File. File provided by UUT vendor that provides information about the characteristics and capabilities of the UUT.

Assertions

Compliance criteria are provided as a list of assertions that describe specific characteristics or behaviors that must be met. Each assertion provides a reference to the USB4™ specification or other documents from which the assertion was derived. In addition, each assertion provides a reference to the specific test description(s) where the assertion is tested.

Each test assertion is formatted as follows:

Assertion #	Test #	Assertion Description

Assertion#: Unique identifier for each spec requirement. The identifier is in the form USB4_SPEC_SECTION_NUMBER#X, where X is a unique integer for a requirement in that section.

Assertion Description: Specific requirement from the specification

Test #: A label for a specific test description in this specification that tests this requirement. Test # can have one of the following values:

NT	This item is not explicitly tested in a test description. Items can be labeled NT for several reasons – including items that are not testable, not important to test for interoperability, or are indirectly tested by other operations performed by the compliance test.
X.X	This item is covered by the test described in test description X.X in this specification.
IOP	This assertion is verified by the USB4 Interoperability Test Suite.
BC	This assertion is verified as part of a background check.

Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

Reserved Fields and Values

Chapter 1

The following Table presents the USB4 Specification Chapter 1 asserts regarding reserved fields and values.

Assertion #	Test Name	Assertion Description
1.7 Reserved Fields and Values		
1.7#1	BC	A transmitter shall not use a value in this specification that is marked as "Rsvd".
1.7#2	TBD	The target of a Transaction shall ignore a Transaction that has any of its defined fields set to an Rsvd value and proceed as if the Transaction was never received.
1.7#3	TBD	A transmitter shall not use a value in this specification that is marked as "Rsvd".
1.7#4	TBD	The target of an Ordered Set shall ignore an Ordered Set that has any of its defined fields set to an Rsvd value and proceed as if the Ordered Set was never received.
1.7#5	BC TD 4.5	A transmitter shall set a field that is marked "Rsvd" to zero.
1.7#6	TBD	A receiver shall ignore any fields that are marked "Rsvd".

Router Assertions

Chapter 4

The following Table presents the USB4 Specification Chapter 4 asserts.

Assertion #	Test Name	Assertion Description
4 Logical Layer		
4.1 Sideband Channel		
4.1.1 Transactions		
4.1.1.1 Symbols		
4.1.1.1#1	IOP	A Sideband Channel shall encode all transmitted Symbols using the 10-bit Start/Stop encoding scheme as follows: A Start bit (logical 0b), Eight bits of payload, and A Stop bit (logical 1b).
4.1.1.2 Transactions		
4.1.1.2#1	IOP	The symbols within a transaction shall be sent in ascending order.
4.1.1.2#2	IOP	The bits within a symbol shall be sent in the order from bit 0 to bit 7.
4.1.1.2.1 LT Transactions		
4.1.1.2.1#1	BC	An LT Transaction shall consist of the three Symbols described in Table 4-1.
4.1.1.2.1#2	NT	Within a LSE Symbol: Bit 5 (LSELane) shall be 0b (for Lane 0) or 1b (for Lane 1).
4.1.1.2.1#3	BC	Within a LSE Symbol: Bit 5 (LSELane) shall be set to 0b when issuing an LT_LRoff Transaction.
4.1.1.2.1#4	BC	Within a LSE Symbol: Bits [7:6] (StartLT) shall be set to 10b.
4.1.1.2.1#5	TD 4.27	The recipient of an LT Transaction shall verify that the CLSE Symbol payload is a bitwise complement of the LSE Symbol payload.
4.1.1.2.1#6	TD 4.27	An LT Transaction that fails this check shall be dropped and no further action shall be taken on its behalf.
4.1.1.2.2 AT Transactions		
4.1.1.2.2#1	BC	An AT Transaction shall consist of the Symbols in Table 4-3.
4.1.1.2.2#2	BC	The number of Data Symbols (n) in an AT Transaction shall not exceed 66.

4.1.1.2.2#3	NT	Within a STX Symbol for an AT Transaction: Bit 0 (*CmdNotResp*) shall be set to 0b for an AT Response or 1b for an AT Command.
4.1.1.2.2#4	BC	Within a STX Symbol: Bit 1 (*ReturnBounce*) shall be set to 0b.
4.1.1.2.2#5	BC	Within a STX Symbol for an AT Transaction: Bit 2 (*Recipient*) shall be set to 1b.
4.1.1.2.2#6	BC	Within a STX Symbol for an AT Transaction: Bit 3 (*Bounce*) shall be set to 0b.
4.1.1.2.2#7	BC	Within a STX Symbol for an AT Transaction: Bit 4 (*Responder*) shall be set to 0b.
4.1.1.2.2#8	BC	Within a STX Symbol for an AT Transaction: Bits [7:6] (*StartAT*) shall be set to 00b.
4.1.1.2.2#9	BC	A Router that receives an AT Command with the Recipient bit set to 1b shall respond with an AT Response.
4.1.1.2.3 RT Transactions		
4.1.1.2.3.1 Broadcast RT Transaction		
4.1.1.2.3.1#1	BC	A Broadcast RT Transaction shall have the format shown in Table 4-5.
4.1.1.2.3.1#2	NT	Within a STX Symbol for a Broadcast RT Transaction: Bits [7:6] (*StartRT*) shall be set to 01b.
4.1.1.2.3.1#3	NT	Within a STX Symbol for a Broadcast RT Transaction: Bit 5 (*Broadcast*) shall be set to 1b.
4.1.1.2.3.1#4	BC TD 4.5	Within a STX Symbol for a Broadcast RT Transaction: Bits [4:1] (*Index*) shall be set to 0.
4.1.1.2.3.1#5	BC	Within a STX Symbol for a Broadcast RT Transaction: Bit 0 (*CmdNotResp*) shall be set to 1b.
4.1.1.2.3.1#6	BC	Within Byte 2 of a Broadcast RT Transaction: Bit 4 (*TBT3-Compatible Speed*) is set to 0b.
4.1.1.2.3.1#7	BC	Within Byte 2 of a Broadcast RT Transaction: Bit 0 (*USB4*) is set to 1b.
4.1.1.2.3.1#8	TD 4.5	Within Byte 3 of a Broadcast RT Transaction: Bit 1 (*Lane1Enabled*) shall equal the value of the Enabling Decision (Lane 1) bit in the Link Configuration register of the SB Register Space.
4.1.1.2.3.1#9	TD 4.5	Within Byte 3 of a Broadcast RT Transaction: Bit 0 (*Lane0Enabled*) shall equal the value of the Enabling Decision (Lane 0) bit in the Link Configuration register of the SB Register Space.

4.1.1.2.3.2 Addressed RT Transaction		
4.1.1.2.3.2#1	BC	An Addressed RT Transaction shall have the format shown in Table 4-9.
4.1.1.2.3.2#2	BC	The number of Data Symbols shall not exceed 66.
4.1.1.2.3.2#3	NT	Within a STX Symbol for an Addressed RT Transaction: Bits [7:6] (*StartRT*) shall be set to 01b.
4.1.1.2.3.2#4	NT	Within a STX Symbol for an Addressed RT Transaction: Bit 5 (*Broadcast*) shall be set to 0b.
4.1.1.2.3.2#5	NT	Within a STX Symbol for an Addressed RT Transaction: Bits [4:1] (*Index*) in an Addressed RT Command shall be set to 0 if the target of the Transaction is the first Router or Re-timer that receives the Transaction.
4.1.1.2.3.2#6	NT	Else, shall be set to the Re-timer Index of the Re-timer that is the target of the Command.
4.1.1.2.3.2#7	NT	Within a STX Symbol for an Addressed RT Transaction: Bit 0 (*CmdNotResp*) shall be set to 0b for an Addressed RT Response or 1b for an Addressed RT Command.
4.1.1.2.3.2#8	NT	A Router that receives an Addressed RT Command with the Index field set to 0 shall respond with an Addressed RT Response.
4.1.1.2.3.2#9	TD 4.1	A Router shall not respond to Addressed RT Commands with a non-zero Index field.
4.1.1.2.4 AT and RT Transaction Rules		
4.1.1.2.4#1	NT	A transmitter shall not abort an AT Transaction or an RT Transaction after the STX Symbol is sent.
4.1.1.2.4#2	TD 4.28	When a receiver receives two or more leading DLE symbols it shall discard the extra leading DLE symbols and process the received LT Transaction as if only one leading DLE symbol was received
4.1.1.2.4#3	TD 4.2	If any Data Symbol or a CRC Symbol in an AT Transaction or an RT Transaction contains the same payload as a DLE Symbol, the transmitter of the AT Transaction or RT Transaction shall insert a Symbol with payload of FEh in front of that Data Symbol.
4.1.1.2.4#4	TD 4.2	The recipient of an AT Transaction or an RT Transaction shall strip all duplicating FEh Symbols that immediately precede a Data Symbol or a CRC Symbol.
4.1.1.2.4#5	BC	Each AT Transaction or RT Transaction shall include a 16-bit CRC.
4.1.1.2.4#6	BC	Only the STX and Data Symbols shall be used in CRC calculation.

4.1.1.2.4#7	BC	The CRC shall be calculated in increasing Symbol order, starting with the STX Symbol.
4.1.1.2.4#8	BC	Within each Symbol, CRC shall be calculated from bit[7] to bit[0].
4.1.1.2.4#9	BC	The CRC shall be calculated using the following rules: Width: 16; Poly: 8005h; Init: FFFFh; RefIn: True; RefOut: True; XorOut: 0000h.
4.1.1.2.5 AT and RT Command Rules		
4.1.1.2.5#1	IOP	A Router shall process AT Commands and AT Responses arriving from the Link Partner or Re-timer in the order received.
4.1.1.2.5#2	IOP	A Router shall process Addressed RT Commands and Addressed RT Responses arriving from a Re-timer in the order received.
4.1.1.2.5#3	TD 4.4	A Router shall not send an AT Command or Addressed RT Command while it is waiting for a response for either a previously sent AT Command or a previously sent Addressed RT Command.
4.1.1.2.5.1 AT Commands		
4.1.1.2.5.1#1	BC	The recipient of an AT Command shall send an AT Response within tCmdResponse of receiving the AT Command.
4.1.1.2.5.1#2	NT	If a Router sends an AT Command, then receives at least two AT Commands from the target of the outstanding AT Command within tATTimeout, it shall stop waiting for an AT Response and shall immediately reissue the outstanding AT Command.
4.1.1.2.5.1#3	TD 4.4	Otherwise, a Router shall wait tATTimeout for an AT Response.
4.1.1.2.5.2 Addressed RT Commands		
4.1.1.2.5.2#1	BC	The recipient of an Addressed RT Command shall send an Addressed RT Response within tCmdResponse of receiving the Addressed RT Command.
4.1.1.2.5.2#2	TD 4.4	A Router shall wait tRTTimeout for an Addressed RT Response.
4.1.1.2.6 Receiver Decoding of LT, AT, and RT Transactions		
4.1.1.2.6#1	TD 4.29	A Router shall ignore and discard an AT Transaction or an Addressed RT Transaction if any of the following are true: The CRC in the Transaction is invalid.
4.1.1.2.6#2	TD 4.29	A Router shall ignore and discard an AT Transaction or an Addressed RT Transaction if any of the following are true: The Transaction has no data and no CRC field.
4.1.1.2.6#3	TD 4.29	Any sequence of Symbols not handled as an LT Transaction, an AT Transaction, or an RT Transaction shall be discarded.

4.1.1.2.6#4	TD 4.29	An AT Response or an RT Response shall not be sent in response to such a sequence.
4.1.1.3 SB Register Space		
4.1.1.3#1	NT	A Router shall maintain one SB Register Space per USB4 Port.
4.1.1.3.1 Router Access		
4.1.1.3.1#1	BC	An AT Command or RT Command shall consist of the Symbols described in Table 4-12.
4.1.1.3.1#2	BC	In an AT or RT Command, LEN shall not be greater than 64.
4.1.1.3.1#3	IOP	For a Write Command, COMMAND_DATA register Contents shall appear least significant byte first.
4.1.1.3.1#4	BC	An AT Response or RT Response shall consist of the Symbols described in Table 4-13.
4.1.1.3.1#5	IOP	For a Read Response, RESPONSE_DATA register contents shall appear low-ordered byte first.
4.1.1.3.1#6	TD 4.30	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Operation with a single Data Symbol, send a Response with no RESPONSE_DATA and LEN set to 0.
4.1.1.3.1#7	TD 4.30	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Read operation to an unsupported vendor defined register or to an undefined register, send a Response with no RESPONSE_DATA and LEN set to 0.
4.1.1.3.1#8	TD 4.30	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Read operation with more than two Data Symbols, send a Response with no RESPONSE_DATA and LEN set to 0.
4.1.1.3.1#9	TD 4.30	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Read operation of more bytes than the target register length, send a Response with the entire register contents in the RESPONSE_DATA and LEN set to the number of bytes in the RESPONSE_DATA field.
4.1.1.3.1#10	TD 4.30	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Read operation of fewer bytes than the target register length, send a Response with the number of bytes requested in the RESPONSE_DATA and LEN set to the number of bytes in the RESPONSE_DATA field.

4.1.1.3.1#11	IOP	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: All other read operations, perform the Read Command and send a Read Response with the contents of the register being accessed in the RESPONSE_DATA field.
4.1.1.3.1#12	TD 4.3	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation to an unsupported vendor defined register or to an undefined register, do not perform the Write Command, send a Response with the LEN field = 0 and the Result Code = 01h (ERROR) in the RESPONSE_DATA field.
4.1.1.3.1#13	TD 4.3	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation with LEN field that does not match the Transaction size, do not perform the Write Command, send a Response with the LEN field = 0 and the Result Code = 01h (ERROR) in the RESPONSE_DATA field.
4.1.1.3.1#14	TD 4.3	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation to a Read-only (RO) register, do not perform the Write Command, a send a Response with the LEN field = 0 and the Result Code = 01h (ERROR) in the RESPONSE_DATA field.
4.1.1.3.1#15	TD 4.3	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation of more bytes than the target register length, do not perform the Write Command, send a Response with the LEN field = 0 and the Result Code = 01h (ERROR) in the RESPONSE_DATA field.
4.1.1.3.1#16	TD 4.3	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: Write operation of less bytes than the target register length, perform the write operation only on the requested bytes, send a Response with the LEN field equal to the size in bytes of the register being accessed and the Result Code = 00h (SUCCESS) in the RESPONSE_DATA field.
4.1.1.3.1#17	IOP	When a Router receives an AT Command or an RT Command, it shall process the AT or RT Command according to Table 4-14 and in the order listed: All other write operations, perform the Write Command and send a Response with the LEN field equal to the size in bytes of the register being accessed and the Result Code = 00h (SUCCESS) in the RESPONSE_DATA field.
4.1.1.3.2 Connection Manager Access		
4.1.1.3.2#1	NT	When the *Pending* bit in a USB4 Port Capability is set to 1b, a Router shall: If the *Target* field in the USB4 Port Capability is set to 000b, the Router shall issue an access to the SB Register Space of the Port.
4.1.1.3.2#2	NT	The Router shall access the register identified in the *Address* field in the USB4 Port Capability.

4.1.1.3.2#3	NT	The Router shall access the number of bytes indicated in the *Length* field.
4.1.1.3.2#4	NT	If the *WnR* field is set to 0b, the Router shall read from the SB Register Space.
4.1.1.3.2#5	NT	If the *WnR* field is set to 1b, the Router shall write to the SB Register Space.
4.1.1.3.2#6	NT	The Router shall write the contents from the *Data* DWs in the USB4 Port Capability.
4.1.1.3.2#7	NT	Register contents shall be written least significant byte first.
4.1.1.3.2#8	NT	When the *Pending* bit in a USB4 Port Capability is set to 1b, a Router shall: If the *Target* field in the USB4 Port Capability is set to 001b, the Router shall send an AT Command on the Sideband Channel of the Port to access the SB Register Space of the Link Partner.
4.1.1.3.2#9	NT	The AT Command shall have the following contents: The *REG* field shall be set to the contents of the *Address* field in the USB4 Port Capability.
4.1.1.3.2#10	NT	The AT Command shall have the following contents: The *LEN* field shall be set to the contents of the Length field in the USB4 Port Capability.
4.1.1.3.2#11	NT	The AT Command shall have the following contents: The *WnR* field shall be set to the contents of the WnR field in the USB4 Port Capability.
4.1.1.3.2#12	NT	The AT Command shall have the following contents: If the *WnR* field is set to 1b, the COMMAND_DATA Symbols shall contain the contents from the *Data* DWs in the USB4 Port Capability. Register contents shall appear least significant byte first.
4.1.1.3.2#13	NT	When the *Pending* bit in a USB4 Port Capability is set to 1b, a Router shall: If the *Target* field in the USB4 Port Capability is set to 010b, the Router shall send an Addressed RT Command on the Sideband Channel of the Port to access the SB Register Space of a Re-timer on the Link.
4.1.1.3.2#14	NT	The Addressed RT Command shall have the following contents: The *Index* field in an Addressed RT Command shall be set to the contents of the Re-timer Index in the USB4 Port Capability.
4.1.1.3.2#15	NT	The Addressed RT Command shall have the following contents: The *REG* field in an Addressed RT Command shall be set to the contents of the Address field in the USB4 Port Capability.
4.1.1.3.2#16	NT	The Addressed RT Command shall have the following contents: The *LEN* field in an Addressed RT Command shall be set to the contents of the Length field in the USB4 Port Capability.
4.1.1.3.2#17	NT	The Addressed RT Command shall have the following contents: The *WnR* field in an Addressed RT Command shall be set to the contents of the WnR field in the USB4 Port Capability.

4.1.1.3.2#18	NT	The Addressed RT Command shall have the following contents: If the *WnR* field in an Addressed RT Command is set to 1b, the COMMAND_DATA Symbols shall contain the contents from the *Data* DWs in the USB4 Port Capability. Register contents shall appear least significant byte first.
4.1.1.3.2#19	NT	A Router shall process an AT Command as described in Table 4-14.
4.1.1.3.2#20	TD 4.4	When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows: The *LEN* field in the AT Response, the RT Response, or the local access is copied to the *Length* field in the USB4 Port Capability.
4.1.1.3.2#21	TD 4.4	When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows: The *No Response* bit is updated.
4.1.1.3.2#22	TD 4.4	When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows: The *Result Code* bit in the USB4 Port Capability is updated.
4.1.1.3.2#23	NT	When a response to a local access is ready or when a Response Transaction is received, the Router shall update the USB4 Port Capability as follows: For a read, the *Data* DWs in the USB4 Port Capability are updated.
4.1.1.3.2#24	TD 4.4	The Router shall then set the *Pending* bit in the USB4 Port Capability to 0b.
4.1.1.3.3 SB Register Definitions		
4.1.1.3.3#1	TD 4.3	A Write operation to a field with the RO access type shall have no effect.
4.1.1.3.3#2	NT	A Read operation to a field with the RO access type shall return a meaningful value.
4.1.1.3.3#3	NT	A field with the RW access type shall be capable of both Read operation and Write operation.
4.1.1.3.3#4	NT	The value read from a field with RW access type shall reflect the last value written to it unless the field was reset in the interim.
4.1.1.3.3#5	NT	A Write operation to a Rsvd field shall have no effect.
4.1.1.3.3#6	TD 4.5	The SB Register Space registers shall have the structure and fields described in Table 4-17.
4.1.1.3.3#7	NT	Registers not listed in Table 4-17 are undefined and shall not be used.
4.1.1.3.3#8	TD 4.5	The Vendor ID Low field shall contain the same value as the lower byte of the Vendor ID field in Router Configuration Space.
4.1.1.3.3#9	TD 4.5	The Vendor ID High field shall contain the same value as the higher byte of the Vendor ID field in Router Configuration Space.

4.1.1.3.3#10	TD 4.5	The Product ID Low field shall contain the same value as the lower byte of the Device ID field in Router Configuration Space.
4.1.1.3.3#11	TD 4.5	The Product ID High field shall contain the same value as the higher byte of the Device ID field in Router Configuration Space.
4.1.1.3.3#12	CH8	A Router shall write the Completion Metadata (if any) to the Metadata field after executing a Port Operation.
4.1.1.3.3#13	TD 4.5	The Enabling Decision (Lane 0) field shall indicate whether or not Lane 0 is enabled during Lane Initialization: 0b = Adapter is in CLd state and 1b = Lane is Enabled.
4.1.1.3.3#14	TD 4.5	The Enabling Decision (Lane 1) field shall indicate whether or not Lane 1 is enabled during Lane Initialization: 0b = Adapter is in CLd state and 1b = Lane is Enabled.
4.1.1.3.3#15	TD 4.5	A Router shall set the Enabling Request (Lane 0) bit to 0b when the Lane Disable bit in the USB4 Adapter Configuration Capability for Lane 0 is 1b.
4.1.1.3.3#16	NT	A Lane 1 Adapter shall not request enabling unless the Lane 0 Adapter requests enabling.
4.1.1.3.3#17	NT	A USB4 Port shall only set the Enabling Request (Lane 1) bit to 1b if all On-Board Re-timers connected between the Router and the cable support dual Lanes.
4.1.1.3.3#18	TD 4.5	A Router shall set the Enabling Request (Lane 1) bit to 0b when the Lane Disable bit in the USB4 Adapter Configuration Capability for Lane 1 is 1b.
4.1.1.3.3#19	TD 4.5	A USB4 Port shall only set the *Gen 3 Support* bit to 1b if all of the following are true: The Port supports Gen 3 speeds; All On-Board Re-timers connected between the Port and the cable support Gen 3 speeds; The Port implements both a Lane 0 Adapter and a Lane 1 Adapter; The Target Link Speed field in the Lane Adapter Configuration Capability is 1100b.
4.1.1.3.3#20	TD 4.5	Otherwise the *Gen 3 Support* bit shall be 0b.
4.1.1.3.3#21	TD 4.5	A USB4 Port shall set the RS-FEC Request (Gen 2) bit to the same value as the Request RS-FEC Gen 2 bit in the USB4 Port Capability.
4.1.1.3.3#22	TD 4.5	A USB4 Port shall set the RS-FEC Request (Gen 3) bit to the same value as the Request RS-FEC Gen 3 bit in the USB4 Port Capability.
4.1.1.3.3#23	TD 4.5	The USB4 Sideband Channel field shall be set to 1b.
4.1.1.3.3#24	TD 4.5	A USB4 Port shall only set the TBT3-Compatible Speeds Supported bit to 1b if all On-Board Re-timers connected between the Router and the cable support TBT3-compatible speeds.
4.1.1.3.3#25	TD 4.5	Bit 2 through 7 of byte 2 in the Link Configuration register are 0 (reserved).

4.1.1.3.3#26	TD 4.5	The *Clock Switch Done (Lane 0)* bit shall be set to the value of the Rx Locked (Lane 0) bit.
4.1.1.3.3#27	TD 4.5	The *Clock Switch Done (Lane 1)* bit shall be set to the value of the Rx Locked (Lane 1) bit.
4.1.1.3.3#28	CH8	A Router shall write the Completion Data (if any) to the *Data* field after executing a Port Operation.
4.1.2 Lane Initialization		
4.1.2#1	IOP	The Sideband Channel shall initialize each Lane independently.
4.1.2#2	IOP	Initialization shall occur for all enabled USB4 Ports on a Router.
4.1.2.1 Phase 1 – Determination of Initial Conditions		
4.1.2.1#1	NT	A Router shall not continue on to Phase 2 until it has obtained the connection information described in this section.
4.1.2.1#2	NT	A Router shall not proceed to Phase 2 if the Link is not USB4.
4.1.2.1#3	NT	A Router shall drive SBTX to logic low on all of its USB4 Ports by default.
4.1.2.1.1 Lane Reversal		
4.1.2.1.1#1	IOP	When a Router detects a reverse insertion on a USB Type-C connector, it shall perform Lane Reversal in the USB4 Port that faces the reversed connector.
4.1.2.1.1#2	IOP	Lane Reversal shall be performed during phase 1.
4.1.2.1.1#3	IOP	The Router shall swap the designation of Lane 0 and Lane 1 and shall associate the Lane 0 Adapter with the updated Lane 0 and the Lane 1 Adapter with the updated Lane 1.
4.1.2.1.1#4	IOP	If there are no On-Board Re-timers between Router and the USB Type-C connector, the Router shall swap its SBTX and SBRX lines facing the connector.
4.1.2.1.2 Polarity Inversion		
4.1.2.2 Phase 2 – Router Detection		
4.1.2.2#1	IOP	After completion of phase 1, a Host Router shall initiate Router detection by driving SBTX to logic high on all of its Downstream Facing Ports.
4.1.2.2#2	TD 4.5	When a Device Router detects a logic high on SBRX of any USB4 Port for tConnectRx time, it shall drive SBTX to logic high on all of its USB4 Ports.
4.1.2.2#3	NT	After a USB4 Port drives its SBTX to logic high and detects a logic high on its SBRX for tConnectRx time, it shall set its *Link Initialization in Progress* bit to 1b, then transition to Phase 3 of Lane Initialization.

4.1.2.3 Phase 3 – Determination of USB4 Port Characteristics		
4.1.2.3#1	TD 4.5	During phase 3, Router A shall read the Link Configuration Register (register 12) of Router B using AT Transactions.
4.1.2.3#2	TD 4.5	Router A shall issue at least one more register read to Router B in order to avoid a tATTimeout delay at the Link Partner.
4.1.2.3#3	NT	(Enabling) If Enabling Request = 1b in the SB Register Space of the Ports of both Router A and Router B, Router A shall: proceed to initialize the Lane.
4.1.2.3#4	TD 4.5	(Enabling) If Enabling Request = 1b in the SB Register Space of the Ports of both Router A and Router B, Router A shall: set the local Enabling Decision bit for the Lane to 1b.
4.1.2.3#5	TD 4.5	(Enabling) Else, Router A shall not initialize the Lane. The Lane shall remain in CLd state.
4.1.2.3#6	TD 4.5	(Enabling) Else, Router A shall set the local Enabling Decision bit for the Lane to 0b.
4.1.2.3#7	TD 4.5	(Dual-Lane) Router A shall set the Bonding Enabled bit in the USB4 Port Capability to 1b if all of the following are true: The USB4 Ports of Router A and Router B both have the Enabling Request bit set to 1b for both Lanes of the USB4 Port; The USB4 Ports of Router A and Router B both support Lane bonding (i.e. the Bonding Support bit is 1b in the SB Register Space of the Ports on both sides of the Lane).
4.1.2.3#8	TD 4.5	(Dual-Lane) Otherwise, Router A shall set Bonding Enabled bit to 0b.
4.1.2.3#9	IOP	(Speed) Router A shall operate at Gen 3 Lane speed if all of the following are true: The Ports on both sides of the Lane support Gen 3 (*Gen 3 Support* is set to 1b); The cable over which Router A and Router B are communicating supports Gen 3.
4.1.2.3#10	IOP	(Speed) Otherwise, Router A shall operate at Gen 2 Lane Speed.
4.1.2.3#11	TD 4.5	(Speed) Router A shall set the Current Link Speed field in the USB4 Adapter Configuration Capability to reflect whether it is operating at Gen 2 or Gen 3 Lane speed.
4.1.2.3#12	IOP	(RS-FEC) At Gen 2 speed, Router A shall enable RS-FEC if both sides of the Link request it (i.e. the *RS-FEC Request (Gen 2)* bit is set to 1b in the SB Register Space of both the local USB4 Port and its Link Partner).
4.1.2.3#13	IOP	(RS-FEC) Otherwise, RS-FEC shall not be enabled.
4.1.2.3#14	TD 4.5	(RS-FEC) For Gen 2 speed, Router A shall set the RS-FEC Enabled (Gen 2) bit in the USB4 Port Capability to reflect whether it is operating with RS-FEC.

4.1.2.3#15	IOP	(RS-FEC) For Gen 3 speed, shall enable RS-FEC if both sides of the Link request it (i.e. the *RS-FEC Request (Gen 3)* bit is set to 1b in the SB Register Space of both the local USB4 Port and its Link Partner).
4.1.2.3#16	IOP	(RS-FEC) Otherwise, RS-FEC shall not be enabled.
4.1.2.3#17	TD 4.5	(RS-FEC) For Gen 3 speed, Router A shall set the RS-FEC Enabled (Gen 3) bit in the USB4 Port Capability to reflect whether it is operating with RS-FEC.
4.1.2.4 Phase 4 – Lane Parameters Synchronization and Transmit Start		
4.1.2.4#1	TD 4.5 TD 4.31	(Step 1) Router A shall send a Broadcast RT Transaction every tLaneParams with the parameter values in Table 4-18.
4.1.2.4#2	TD 4.5 TD 4.31	(Step 1) Router A shall continue sending Broadcast RT Transactions until all of the following conditions are true, then continue to step 2): At least tLTPhase4 time has passed from completion of Phase 2; Router A has sent Broadcast RT Transactions at least twice; Router A has received a Broadcast RT Transaction from Router B.
4.1.2.4#3	TD 4.5	(Step 2) Router A shall activate the transmitter on each enabled Lane at the selected speed and shall send SLOS1.
4.1.2.4#4	TD 4.5	(Step 3) After its transmitter is transmitting a valid signal, Router A shall then send an LT_Resume Transaction for each enabled Lane in the USB4 Port and shall set to 1b the Tx Active bit in the Tx Status byte of the TxFFE Register in the SB Register Space to indicate that it has started transmission on the target Lane.
4.1.2.4#5	TD 4.5	(Step 3) The LSELane field in the LT_Resume Transaction shall equal the Lane number associated with the transmitter.
4.1.2.5 Phase 5 – Link Equalization		
4.1.2.5#1	TD 4.5	Router A's transmitter shall perform the transmitter flow in the symmetric equalization flow defined in Section 4.1.2.5.1.1.
4.1.2.5#2	TD 4.5	A Router shall use Addressed RT Transactions with the *Index* field set to 0 to access the SB Register Space of the adjacent component, which can be either an On-Board Re-timer, a Cable Re-timer, or Router B.
4.1.2.5#3	TD 4.5	Router B's receiver shall perform the receiver flow in the symmetric equalization flow defined in Section 4.1.2.5.1.2.
4.1.2.5#4	TD 4.5	The Router shall use Addressed RT Transactions with the *Index* field set to 0b to access the SB Register Space of the adjacent component, which can be either an On-Board Re-timer, a Cable Re-timer, or Router A.
4.1.2.5#5	TD 4.5	A Router shall set the Clock Switch Done bit to 1b in the SB Register space of the Ports of a USB4 Port after all of the USB4 Port's receivers complete the equalization flow.

4.1.2.5.1 Phase 5 – Symmetric TxFFE Negotiation		
4.1.2.5.1.1 Phase 5 – Transmitter Flow		
4.1.2.5.1.1#1	NT	(Step 1) The transmitter shall start with the following default values in the Tx Status byte of the TxFFE register: Tx Active bit = 1b; Request Done bit = 0b.
4.1.2.5.1.1#2	TD 4.5	(Step 2) The transmitter shall read the Rx Status & TxFFE Request byte of the receiver.
4.1.2.5.1.1#3	TD 4.5	(Step 3) On reception of a Response from the receiver, The transmitter shall do the following: If Rx Locked = 1, then negotiation is complete and no further TxFFE negotiation steps are taken; Else, if New Request = 0, the receiver has not provided a new request yet. The transmitter shall retry step 2 within tPollTXFFE of receiving the Response; Else, this is a new request to update TxFFE parameters. Continue on to step 4.
4.1.2.5.1.1#4	TD 4.5	(Step 4) The transmitter shall update its transmitter parameters based on the new parameters in the received Response.
4.1.2.5.1.1#5	TD 4.5	(Step 4) The transmitter shall update its Tx Status byte with the following values: TxFFE Setting = the index (from 16 possible values) loaded above to the TxFFE configuration configured at the transmitter; Request Done = 1b.
4.1.2.5.1.1#6	TD 4.5	(Step 5) The transmitter shall read the Rx Status & TxFFE Request byte of the receiver.
4.1.2.5.1.1#7	TD 4.5	(Step 6) On reception of a Response from the receiver, the transmitter shall do the following: If New Request = 1, the receiver is still trying to lock on a previous request. The transmitter shall retry step 5 within tPollTXFFE of receiving the Response; Else, the transmitter shall set the Request Done bit in the Tx Status byte to 0b, and return to step 2.
4.1.2.5.1.2 Phase 5 – Receiver Flow		
4.1.2.5.1.2#1	NT	(Step 1) The receiver shall start with the following default values in the Rx Status & TxFFE Request byte of the TxFFE register: Rx Locked bit = 0b; New Request bit = 1b; Rx Active bit = 0b.
4.1.2.5.1.2#2	TD 4.5	(Step 2) The receiver shall read the transmitter's Tx Status byte.
4.1.2.5.1.2#3	TD 4.5	(Step 3) On reception of a Response from the transmitter, the receiver shall do the following: If Tx Active = 1b, then enable the receiver, set Rx Active to 1b, and continue on to Step 4; Else, repeat step 2 within tPollTXFFE of receiving the Response.
4.1.2.5.1.2#4	TD 4.5	(Step 4) The receiver shall evaluate its receiver behavior and shall set the Rx Locked bit to 1b if equalization is complete.
4.1.2.5.1.2#5	TD 4.5	(Step 5) The receiver shall do the following: If Rx Locked = 1, then TXFFE negotiation is complete and no further negotiation steps are taken.

4.1.2.5.1.2#6	TD 4.5	(Step 5) The receiver shall do the following: If Rx Locked = 0, the receiver shall: Select a new set of TxFFE parameters and set the TxFFE Request field to the index of the selected set of TXFFE parameters; Set the New Request bit to 1b; Continue with the steps below.
4.1.2.5.1.2#7	TD 4.5	(Step 6) The receiver shall read the transmitter's Tx Status byte.
4.1.2.5.1.2#8	TD 4.5	(Step 7) On reception of a Response from the transmitter, the receiver shall do the following: If (Tx Active = 1b) AND (Request Done = 1b) AND (TxFFE Setting = value of TxFFE request in the local Rx Status & TxFFE Request byte), then continue on to Step 8.
4.1.2.5.1.2#9	TD 4.5	(Step 7) On reception of a Response from the transmitter, the receiver shall do the following: If (Tx Active = 0b) OR (Request Done = 0b) OR (TxFFE Setting != value of TxFFE request in the local Rx Status & TxFFE Request byte), repeat step 5 within tPollTXFFE of receiving the Response.
4.1.2.5.1.2#10	TD 4.5	(Step 8) The receiver shall evaluate its receiver behavior and set the Rx Locked bit to 1b if equalization is complete.
4.1.2.5.1.2#11	TD 4.5	(Step 9) The receiver shall set the New Request bit to 0b.
4.1.2.5.1.2#12	TD 4.5	(Step 10) The receiver shall read the transmitter's Tx Status byte by sending a read Command to the transmitter that targets its TxFFE register.
4.1.2.5.1.2#13	TD 4.5	(Step 11) On reception of a Response from the transmitter, the receiver shall do the following: If (Tx Active = 1b) and (Request Done = 0b), then go to Step 4.
4.1.2.5.1.2#14	TD 4.5	(Step 11) On reception of a Response from the transmitter, the receiver shall do the following: If (Tx Active = 0b) or (Request Done = 1b), repeat Step 9 within tPollTXFFE of receiving the Response.
4.2 Logical Layer State Machine		
4.2.1 Lane Adapter State Machine		
4.2.1.1 Disabled		
4.2.1.1.1 Entry to State		
4.2.1.1.1#1	TD 4.6	An Adapter shall enter this state from Training state or CL0 state when the *Lane Disable* bit in the Lane Adapter Configuration Capability is set to 1b.
4.2.1.1.1#2	TD 4.6	A Lane Adapter shall set the *Plugged* bit to 0b upon transitioning to Disabled state.

4.2.1.1.2 Behavior in State		
4.2.1.1.1.3 Exit from State		
4.2.1.1.3#1	NT	An Adapter shall exit this state when the *Lane Disable* bit in the Lane Adapter Configuration Capability is set to 0b
4.2.1.1.3#2	NT	A disabled Adapter shall stay in the Disabled state for a minimum of tDisabled.
4.2.1.1.3#3	NT	If the *Lane Disable* bit is set to 0b less than tDisabled after sending the LT_Fall Transaction, the Adapter shall not transition to the CLd state until tDisabled has elapsed.
4.2.1.2 CLd		
4.2.1.2.1 Entry to State		
4.2.1.2.1#1	NT	An Adapter shall enter this state on any of the following events: Router power on.
4.2.1.2.1#2	NT	An Adapter shall enter this state on any of the following events: The USB4 Port is disconnected.
4.2.1.2.1#3	NT	An Adapter shall enter this state on any of the following events: Router enters Sleep state.
4.2.1.2.1#4	NT	In addition to the events listed above, a Lane Adapter that is not the Upstream Adapter shall enter this state on any of the following events: Adapter exits from the Disabled state.
4.2.1.2.1#5	TD 4.8	In addition to the events listed above, a Lane Adapter that is not the Upstream Adapter shall enter this state on any of the following events: Adapter receives an LT_Fall Transaction.
4.2.1.2.2 Behavior in State		
4.2.1.2.2#1	NT	A Lane Adapter that enters this state due to a disconnect shall enter Lane Initialization starting from Phase 1.
4.2.1.2.2#2	NT	A Lane Adapter that enters this state from the Disabled State performs Lane Initialization after the Lane is enabled. The Lane Adapter shall start Lane Initialization from Phase 4. The USB4 Port shall maintain any state acquired in Phases 1 through 3 of previous Lane Initialization.
4.2.1.2.2#3	TD 4.23 TD 4.24 TD 4.25 TD 4.26	A Lane Adapter that enters this state due to the Router entering Sleep state performs Lane Initialization after a Wake event. The Lane Adapter shall start Lane Initialization from Phase 5.

4.2.1.2.2#4	TD 4.33	A Lane Adapter that enters this state due to Link training timeout shall perform Lane Initialization starting from Phase 1
4.2.1.2.2#5	TD 4.7 TD 4.8	A Lane Adapter (that is not the Upstream Adapter) that enters this state due to reception of an LT_Fall Transaction starts Lane Initialization when it receives a Broadcast RT Transaction. The Lane Adapter shall start Lane Initialization from Phase 4. The USB4 Port shall maintain any state acquired in Phases 1 through 3 of previous Lane Initialization.
4.2.1.2.2#6	TD 4.7 TD 4.8	The Lane 0 Adapter shall not start Lane Initialization until it receives a Broadcast RT Transaction with the *Lane0Enabled* bit set to 1b.
4.2.1.2.2#7	TD 4.7 TD 4.8	The Lane 1 Adapter shall not start Lane Initialization until it receives a Broadcast RT Transaction with the *Lane1Enabled* bit set to 1b.
4.2.1.2.3 Exit from State		
4.2.1.2.3#1	NT	A Lane Adapter shall exit this state when the Lane's High-Speed transmitter is transmitting (completion of Phase 4 of Lane Initialization) and its receiver is enabled.
4.2.1.2.3#2	TD 4.9	After exiting the CLd state, a Lane Adapter shall transition to the Training.LOCK1 state.
4.2.1.3 Training		
4.2.1.3.1 Entry to State		
4.2.1.3.1#1	NT	A Lane Adapter shall enter this state on any of the following events: After exiting the CLd state.
4.2.1.3.1#2	TD 4.40 TD 4.41	A Lane Adapter shall enter this state on any of the following events: When recovering from a USB4 Link error.
4.2.1.3.1#3	TD 4.10 TD 4.11 TD 4.12 TD 4.13	A Lane Adapter shall enter this state on any of the following events: After exiting the CL2 or CL1 states.
4.2.1.3.2 Behavior in State		
4.2.1.3.2#1	TD 4.9 TD 4.32 TD 4.33	A Lane Adapter shall follow the Training Sub-state machine described in Figure 4-9 with the behavior described in Table 4-19 and the sub-state transitions described in Table 4-20.
4.2.1.3.2#2	TD 4.9	The sub-state transitions shall occur within tTrainingTransition time from receiving the last bit of the relevant Symbols.

4.2.1.3.2#3	NT	In LOCK1 state, a transmitter shall send back-to-back SLOS1.
4.2.1.3.2#4	NT	In LOCK2 state, a transmitter shall send back-to-back SLOS2.
4.2.1.3.2#5	NT	In TS1 state, a transmitter send back-to-back TS1 Ordered Sets.
4.2.1.3.2#6	NT	In TS2 state, a transmitter send back-to-back TS2 Ordered Sets.
4.2.1.3.3 Exit from State		
4.2.1.3.3#1	TD 4.9	A Lane Adapter that transitions from CLd state to Training state shall complete training and transition to the CL0 state within tTrainingAbort1 after entering the Training state.
4.2.1.3.3#2	NT	If the Adapter does not transition to CL0 state within tTrainingAbort1, the Router shall initiate a Disconnect by driving SBTX to a logical low state for a minimum of tDisconnectTx.
4.2.1.3.3#3	TD 4.40	A Lane Adapter that transitions from a state other than CLd to Training state shall complete training and transition to the CL0 state within tTrainingAbort2 after entering the Training state.
4.2.1.3.3#4	TD 4.33	If the Port does not transition to CL0 state within tTrainingAbort2, the Router shall initiate a Disconnect by driving SBTX to a logical low state for a minimum of tDisconnectTx.
4.2.1.3.3#5	TD 4.6	A Hot Plug Event Packet shall be sent on transition to CL0 state if the Adapter entered Training state from a CLd state.
4.2.1.3.3#6	TD 4.9	A Lane Adapter shall set the Plugged bit to 1b when it transitions from the Training state to the CL0 state.
4.2.1.3.4 SLOS1 and SLOS2		
4.2.1.3.4#1	IOP	When operating in Gen 2 mode with RS-FEC encoding disabled, SLOS shall be encoded using 64b/66b encoding.
4.2.1.3.4#2	IOP	When operating in Gen 2 mode with RS-FEC encoding enabled, SLOS that are not RS-FEC encoded shall be encoded using 128b/132b encoding.
4.2.1.3.4#3	IOP	When operating in Gen 3 mode, SLOS that are not RS-FEC encoded shall be encoded using 128b/132b encoding.
4.2.1.3.4#4	TD 4.9	The SLOS1 and SLOS2 shall not be scrambled, and the scrambler shall not advance upon receive/transmit.
4.2.1.3.4#5	TD 4.9	When transmitting SLOS1 or SLOS2 using 64b/66b encoding, a Router shall transmit all 32 SLOS Symbols in their entirety.
4.2.1.3.4#6	TD 4.9	When using 128b/132b encoding, a Router shall transmit all 16 SLOS Symbols in their entirety.

4.2.1.3.4#7	TD 4.9	A Router shall not transmit an incomplete SLOS.
4.2.1.3.5 TS1 and TS2 Ordered Sets		
4.2.1.3.5#1	NT	A TS1 Ordered Set and a TS2 Ordered Set shall have the structure in Table 4-25.
4.2.1.3.5#2	TD 4.36	Bits 63:59 (Rsvd) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#3	TD 4.9	Bits 58:56 (Lane Bonding Target) of a TS1 or TS2 Ordered Set shall be set according to the value of the Target Link Width field of the USB4 Adapter Configuration Capability: 000b – Establish two single-Lane Links and 001b – Establish a dual-lane Link. All other values are reserved and shall not be used.
4.2.1.3.5#4	TD 4.9	Bits 55:48 (Lane Number) of a TS1 or TS2 Ordered Set shall be set to match the Lane number: 00h - Lane 0 and 01h - Lane 1. All other values are reserved and shall not be used.
4.2.1.3.5#5	TD 4.9 TD 4.36	Bits 47:32 (Rsvd) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#6	BC	Bits 31:29 (Rsvd) of a TS1 or TS2 Ordered Set shall be set to 0 by a transmitter.
4.2.1.3.5#7	TD 4.36	Bits 31:29 (Rsvd) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#8	TD 4.9	A Transmitter shall set bits 28:26 (Lane Bonding Target 2) of a TS1 or TS2 Ordered Set to match the Lane Bonding Target field.
4.2.1.3.5#9	TD 4.36	Bits 28:26 (Lane Bonding Target 2) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#10	TD 4.36	Bits 25:16 (Rsvd) of a TS1 or TS2 Ordered Set shall be ignored by a receiver.
4.2.1.3.5#11	TD 4.9	Bits 9:0 (SCR) of a TS1 or TS2 Ordered Set shall be set to 00 1111 0010b to indicate that Ordered Set contents are scrambled.
4.2.1.4 CL0		
4.2.1.4.1 Entry to State		
4.2.1.4.1#1	TD 4.5 TD 4.9	A Lane Adapter shall enter this state upon any of the following events: Successful completion of Lane training.
4.2.1.4.1#2	TD 4.9	A Lane Adapter shall enter this state upon any of the following events: Successful completion of Lane Bonding.
4.2.1.4.1#3	TD 4.14 TD 4.15	A Lane Adapter shall enter this state upon any of the following events: Exit from CL0s state

4.2.1.4.2 Behavior in State		
4.2.1.4.3 Exit from State		
4.2.1.4.3#1	NT	A Lane Adapter shall exit this state after one of the following occurs: Adapter Disable.
4.2.1.4.3#2	NT	A Lane Adapter that exits this state due to an Adapter disable shall transition to either the Disabled state or the CLd state as defined in Section 4.4.6.
4.2.1.4.3#3	NT	A Lane Adapter shall exit this state after one of the following occurs: Adapter disconnect. An Adapter that exits this state due to a disconnect event shall transition to the CLd state.
4.2.1.4.3#4	TD 4.8	A Lane Adapter shall exit this state after one of the following occurs: Reception of an LT_Fall Transaction. The Adapter shall transition to the CLd state.
4.2.1.4.3#5	TD 4.40 TD 4.41	A Lane Adapter shall exit this state after one of the following occurs: Transition to Training state when: An error event occurs that transitions the Lane Adapter to the Training.LOCK1 state.
4.2.1.4.3#6	TD 4.32 TD 4.33	A Lane Adapter shall exit this state after one of the following occurs: Transition to Training state when: Reception of any 2 SLOS Symbols in a row transitions the Lane Adapter either to the Training.LOCK1 sub-state or to the Training.LOCK2 sub-state.
4.2.1.4.3#7	NT	A Lane Adapter shall exit this state after one of the following occurs: Transition to CL0s, CL1, or CL2 states.
4.2.1.4.3#8	TD 4.9 TD 4.10 TD 4.11 TD 4.14 TD 4.15	A Lane Adapter shall exit this state after one of the following occurs: Transition to Lane Bonding state when either: The *Lane Bonding* bit in the USB4 Adapter Configuration Capability Register of either Adapter in the USB4 Port is set to 1b.
4.2.1.4.3#9	TD 4.10	A Lane Adapter shall exit this state after one of the following occurs: Transition to Lane Bonding state when either: 3 TS1 Ordered Sets are received in a row.
4.2.1.4.3#10	NT	A Lane Adapter shall not exit this state to enter Lane Bonding state while it is sending a Transport Layer Packet.
4.2.1.4.3#11	NT	The Adapter shall complete sending the packet before entering Lane Bonding state.

4.2.1.5 Lane Bonding		
4.2.1.5.1 Entry to State		
4.2.1.5.1#1	TD 4.9	A Lane Adapter shall enter this state from CL0 state on any of the following events: The Lane Bonding bit in the Lane Adapter Capability Register of either Adapter in the USB4 Port is set to 1b.
4.2.1.5.1#2	TD 4.9	An Adapter shall enter this state from CL0 state on any of the following events: Three TS1 Ordered Sets are received in a row.
4.2.1.5.2 Behavior in State		
4.2.1.5.2#1	TD 4.9 TD 4.34	A Lane Adapter shall follow the Lane Bonding sub-state machine described in Figure 4-10 with the behavior described in Table 4-26 and the state transitions described in Table 4-27.
4.2.1.5.2#2	NT	In TS1 state, transmitter shall send back-to-back TS1 Ordered Sets.
4.2.1.5.2#3	NT	In TS2 state, transmitter shall send back-to-back TS2 Ordered Sets.
4.2.1.5.3 Exit from State		
4.2.1.5.3#1	TD 4.9	A Lane Adapter shall exit this state as defined in Table 4-27.
4.2.1.5.3#2	TD 4.9	A Lane Adapter that exits this state due to successful completion shall transition to the CL0 state.
4.2.1.5.3#3	TD 4.9	A Lane Adapter that transitions to CL0 state shall continue sending TS2 Ordered Sets until the other Adapter exits the Lane Bonding state.
4.2.1.5.3#4	NT	A Lane Adapter that exits this state due to unsuccessful completion (i.e. Transitions 2, 4, and 5 in Table 4-27) shall transition to the Training.LOCK2 sub-state
4.2.1.6 Low Power (CL0s, CL1, CL2)		
4.2.1.6#1	NT	When a Lane Adapter supports CLx states, it shall enter or reject a CLx state as described in Section 4.2.1.6.2.
4.2.1.6#2	NT	When a Lane Adapter does not support CLx states, it shall reject entry to CLx state as described in Section 4.2.1.6.2.
4.2.1.6.1 Ordered Sets		
4.2.1.6.1#1	NT	Bits 9:0 (SCR) in a CL2_REQ Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#2	NT	Bits 9:0 (SCR) in a CL1_REQ Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.

4.2.1.6.1#3	TD 4.10 TD 4.11	Bits 9:0 (SCR) in a CL2_ACK Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#4	TD 4.12 TD 4.13	Bits 9:0 (SCR) in a CL1_ACK Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#5	TD 4.14 TD 4.15	Bits 9:0 (SCR) in a CL0s_ACK Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#6	TD 4.10 TD 4.11 TD 4.12 TD 4.13	Bits 9:0 (SCR) in a CL_NACK Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1#7	NT	Bits 9:0 (SCR) in a CL_OFF Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.2.1.6.1.1 CL_WAKE1.X Ordered Sets		
4.2.1.6.1.1#1	NT	A CL_WAKE1.X Ordered Set shall not be scrambled, and the scrambler shall not advance upon receive/transmit.
4.2.1.6.1.1#2	NT	Unless otherwise mentioned, a CL_WAKE1.X Ordered Set shall be transmitted in its entirety.
4.2.1.6.1.2 CL_WAKE2.X Ordered Sets		
4.2.1.6.1.2#1	NT	When operating in Gen 2 mode with RS-FEC encoding disabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 64/66b encoding and the following modifications: Bits [63:56] of an even numbered Symbol payload shall be CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#2	NT	When operating in Gen 2 mode with RS-FEC encoding disabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 64/66b encoding and the following modifications: Bits [63:56] of an odd numbered Symbol payload shall be the logical inverse of CXh, where "X" is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#3	NT	When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [127:120] of an even numbered Symbol payload shall be CXh, where “X” is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.

4.2.1.6.1.2#4	NT	When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [63:56] of an even numbered Symbol payload shall be CXh, where "X" is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#5	NT	When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [127:120] of an odd numbered Symbol payload shall be the logical inverse of CXh, where "X" is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#6	NT	When operating in Gen 2 mode and RS-FEC encoding is enabled, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [63:56] of an odd numbered Symbol payload shall be the logical inverse of CXh, where "X" is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#7	NT	When operating in Gen 3 mode, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [127:120] of an even numbered Symbol payload shall be CXh, where "X" is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#8	NT	When operating in Gen 3 mode, a CL_WAKE2.X Ordered Set has the structure of an SLOS2 with 128b/132b Encoding and the following modifications: Bits [127:120] of an odd numbered Symbol payload shall be the logical inverse of CXh, where "X" is the hexadecimal index from the last CL_WAKE1.X Ordered Set received.
4.2.1.6.1.2#9	TD 4.11 TD 4.13	A CL_WAKE2.X Ordered Set shall not be scrambled, and the scrambler shall not advance upon receive/transmit.
4.2.1.6.1.2#10	TD 4.11 TD 4.13	Unless otherwise mentioned, a CL_WAKE2.X Ordered Set shall be transmitted in its entirety.
4.2.1.6.2 Entry to State		
4.2.1.6.2#1	TD 4.10 TD 4.11 TD 4.12 TD 4.13	(Requesting Port) The request Ordered Set shall be sent back-to-back until a response Ordered Set is received from the Link Partner.
4.2.1.6.2#2	NT	(Requesting Port) An Adapter shall send CL2_REQ Ordered Sets when its USB4 Port does not assert any objections to enter CL2 state.
4.2.1.6.2#3	NT	(Requesting Port) An Adapter shall send CL1_REQ Ordered Sets when its USB4 Port asserts an objection to enter CL2 state but does not assert any objections to enter CL1 state.

4.2.1.6.2#4	NT	(Requesting Port) If a Lane Adapter receives a CL1_REQ Ordered Set or a CL2_REQ Ordered Set from its Link Partner, it shall not request entry to a Low Power state until after transitioning back to CL0.
4.2.1.6.2#5	NT	(Requesting Port) If the Requesting Port asserts an objection after the Lane Adapter has sent a request Ordered Set, the Lane Adapter shall ignore the objection until the Lane Adapter is either in a CLx state or receives a CL_NACK Ordered Set.
4.2.1.6.2#6	NT	(Responding Port) A Lane Adapter shall reject a request to enter a Low Power state when all of the following are true: The Adapter has already sent a request to enter the same low power state; and The *PM Secondary* bit in the Lane 0 Adapter and/or the Lane 1 Adapter of the Responding Port is set to 0b.
4.2.1.6.2#7	TD 4.10 TD 4.11 TD 4.12 TD 4.13	The Lane Adapter shall send CL_NACK Ordered Sets for as long as it receives the request Ordered Set from the Link Partner.
4.2.1.6.2#8	NT	A Lane Adapter that receives a CL1_REQ Ordered Set after it has sent a CL2_REQ Ordered Set, shall accept the request by responding with CL1_ACK Ordered Sets. The Adapter shall stop sending CL2_REQ Ordered Sets.
4.2.1.6.2#9	NT	A Lane Adapter that receives a CL2_REQ Ordered Set after it has sent a CL1_REQ Ordered Set, shall not respond to the request and shall continue sending CL1_REQ Ordered Sets.
4.2.1.6.2#10	TD 4.10 TD 4.11	Else, if the Responding Port does not assert an objection to enter CL2 state, it shall respond to CL2_REQ Ordered Sets with a CL2_ACK Ordered Set. The CL2_ACK Ordered Set shall be sent 375 times.
4.2.1.6.2#11	TD 4.12 TD 4.13	Else, if the Responding Port does not assert an objection to enter CL1 state, it shall respond to CL2_REQ or CL1_REQ Ordered Sets with a CL1_ACK Ordered Set. The CL1_ACK Ordered Set shall be sent 375 times.
4.2.1.6.2#12	TD 4.14 TD 4.15	Else, if the *CL0s Enable* bit is set to 1b in the Lane 0 Adapter of the Responding Port, a Lane Adapter shall respond to a request to enter a Low Power state with a CL0s_ACK Ordered Set. The CL0s_ACK Ordered Set shall be sent 16 times.
4.2.1.6.2#13	TD 4.10 TD 4.11 TD 4.12 TD 4.13	Else, a Lane Adapter shall respond to a request to enter a Low Power state with CL_NACK Ordered Sets. The CL_NACK Ordered Sets shall be sent 16 times.

4.2.1.6.2#14	TD 4.10 TD 4.11 TD 4.12 TD 4.13	The Adapter shall resume regular CL0 operation in the transmit direction once it stops sending the CL_NACK Ordered Sets.
4.2.1.6.2#15	NT	If the Responding Port asserts an objection after the Lane Adapter has sent a CLx_ACK response Ordered Set, but before the transition to CLx state is complete, the Lane Adapter shall ignore the objection until it transitions to the CLx state.
4.2.1.6.2#16	NT	A Lane Adapter shall stop sending a request to enter a Low Power state when it receives a response Ordered Set from the Link Partner.
4.2.1.6.2#17	TD 4.10 TD 4.11 TD 4.12 TD 4.13	(Requesting Port) If the response is a CL2_ACK, a CL1_ACK, or a CL0s_ACK Ordered Set, the Lane Adapter shall send 375 CL_OFF Ordered Sets. The CL_OFF Ordered sets shall be sent back-to-back.
4.2.1.6.2#18	TD 4.10 TD 4.11 TD 4.12 TD 4.13	(Requesting Port) The first CL_OFF Ordered Set shall be sent within tCLxResponse after detection of the response.
4.2.1.6.2#19	TD 4.10 TD 4.11 TD 4.12 TD 4.13	(Requesting Port) If the response is a CL2_ACK or a CL1_ACK Ordered Set, the Adapter shall also shut down its receiver.
4.2.1.6.2#20	TD 4.10 TD 4.11 TD 4.12 TD 4.13	(Requesting Port) If the response is a CL_NACK Ordered Set, the Adapter shall not send another CL2_REQ Ordered Set or CL1_REQ Ordered Set for tCLxRetry after receiving the CL_NACK Ordered Set.
4.2.1.6.2#21	TD 4.10 TD 4.11 TD 4.12 TD 4.13	(Requesting Port) If the response is a CL_NACK Ordered Set, all Lane Adapters in the Requesting Port shall resume regular CL0 operation.
4.2.1.6.2#22	NT	If the Requesting Port detects Link errors in the direction of the Link Partner before receiving a response Ordered Set from the Link Partner, it shall: Stop sending the request to enter a Low Power state.

4.2.1.6.2#23	NT	If the Requesting Port detects Link errors in the direction of the Link Partner before receiving a response Ordered Set from the Link Partner, it shall: Transition its Lane Adapters to the Training.LOCK1 sub-state and send the first SLOS within tCLxResponse of detecting the Link error.
4.2.1.6.2#24	TD 4.10 TD 4.11 TD 4.12 TD 4.13	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 1. Shut down its transmitter within tTxOff time.
4.2.1.6.2#25	TD 4.10 TD 4.11	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 2. Transition state as follows: If the response from the Link Partner was CL2_ACK, transition to CL2 state.
4.2.1.6.2#26	TD 4.12 TD 4.13	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 2. Transition state as follows: If the response from the Link Partner was CL1_ACK, transition to CL1 state.
4.2.1.6.2#27	NT	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 2. Transition state as follows: If the response from the Link Partner was CL0s_ACK, transition to CL0s state.
4.2.1.6.2#28	NT	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 3. Enable exit from CLx state as follows: If the response from the Link Partner was CL2_ACK or CL1_ACK, wait tEnterLFPS1 time after the state transition in Step 2), then enable transmission and detection of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#29	NT	In the Requesting Port, a Lane Adapter shall do the following after sending 375 CL_OFF Ordered Sets: 3. Enable exit from CLx state as follows: If the response from the Link Partner was CL0s_ACK, wait tEnterLFPS4 time after the state transition in Step 2), then enable transmission of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#30	TD 4.10 TD 4.11 TD 4.12 TD 4.13 TD 4.14 TD 4.15	In the Responding Port, a Lane Adapter shall shut down its receiver after receiving a CL_OFF Ordered Set. If the Adapter sent CL0s_ACK Ordered Sets, it shall also transition to the CL0s state.
4.2.1.6.2#31	NT	In the Responding Port, The Adapter shall then enable exit from the Low Power state as follows: If the Adapter sent CL2_ACK or CL1_ACK, wait tEnterLFPS2 time after shutting down the receiver, then enable transmission and detection of Low Frequency Periodic Signaling (LFPS).

4.2.1.6.2#32	NT	In the Responding Port, The Adapter shall then enable exit from the Low Power state as follows: If the Adapter sent CL0s_ACK, wait tEnterLFPS5, then enable detection of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#33	TD 4.10 TD 4.11	In the Responding Port, a Lane Adapter shall do the following after the equivalent of 375 Symbol Times has passed since sending the first response Ordered Set: If the Adapter sent CL2_ACK Ordered Sets, it shall shut down its transmitter and shall shut down its receiver if it has not done so already. It shall then transition to the CL2 state
4.2.1.6.2#34	TD 4.12 TD 4.13	In the Responding Port, a Lane Adapter shall do the following after the equivalent of 375 Symbol Times has passed since sending the first response Ordered Set: If the Adapter sent CL1_ACK Ordered Sets, it shall shut down its transmitter and shall shut down its receiver if it has not done so already. It shall then transition to the CL1 state.
4.2.1.6.2#35	TD 4.15	In the Responding Port, a Lane Adapter shall do the following after the equivalent of 375 Symbol Times has passed since sending the first response Ordered Set: If the Adapter sent CL0s_ACK Ordered Sets, it shall shut down its receiver if it has not done so already. It shall then transition to the CL0s state.
4.2.1.6.2#36	NT	In the Responding Port, a Lane Adapter shall do the following after the equivalent of 375 Symbol Times has passed since sending the first response Ordered Set: Enable exit from CLx state as follows: If the Adapter sent CL2_ACK or CL1_ACK Ordered Sets, wait tEnterLFPS3 time, then enable transmission and detection of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#37	NT	In the Responding Port, a Lane Adapter shall do the following after the equivalent of 375 Symbol Times has passed since sending the first response Ordered Set: Enable exit from CLx state as follows: If the Adapter sent CL0s_ACK Ordered Sets, wait 240 Symbol Times + 100ns, then enable detection of Low Frequency Periodic Signaling (LFPS).
4.2.1.6.2#38	TD 4.37	A Lane Adapter may transition to Training.LOCK1 sub-state as a result of Lane errors during the entry to Low Power state with the following exceptions: After sending the first CL2_ACK, CL1_ACK, or CL0s_ACK Ordered Set, a Lane Adapter shall not enter Training state as a result of Lane errors in its receivers.
4.2.1.6.2#39	NT	A Lane Adapter may transition to Training.LOCK1 sub-state as a result of Lane errors during the entry to Low Power state with the following exceptions: A Lane Adapter that is sending CL_OFF Ordered Sets shall complete the transition to CL2, CL1, or CL0s state.
4.2.1.6.3 Objections		
4.2.1.6.3#1	TD 4.10 TD 4.11	A USB4 Port shall assert an objection to enter CL2 state if: The *CL2 Support* bit in the Lane 0 Adapter is 0.
4.2.1.6.3#2	NT	A USB4 Port shall assert an objection to enter CL2 state if: The *CL2 Enable* bit in the Lane 0 Adapter is 0b.

4.2.1.6.3#3	NT	A USB4 Port shall assert an objection to enter CL2 state if: There is a Transport Layer Packet to be sent over the USB4 Port.
4.2.1.6.3#4	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a PCIe Adapter's Routing Table and the PCIe Adapter is not in PCIe L1 state.
4.2.1.6.3#5	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of the Upstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message transmitted upstream is smaller than the sum of the CL2 entry and exit latency.
4.2.1.6.3#6	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a Downstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message received by the Downstream PCIe Adapter is smaller than the sum of the CL2 entry and exit latency.
4.2.1.6.3#7	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a DP IN Adapter's Routing Table.
4.2.1.6.3#8	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a DP OUT Adapter's Routing Table and a Packet is issued from the DP OUT Adapter.
4.2.1.6.3#9	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a USB3 Adapter's Routing Table and the USB3 link between the USB3 Adapter and the internal USB3 device is not in U2 or U3 state.
4.2.1.6.3#10	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a USB3 Adapter's Routing Table, the USB3 link between the USB3 Adapter and the internal USB3 device is in U2 state, and CL2 entry is disabled in U2 state.
4.2.1.6.3#11	NT	A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a USB3 Adapter's Routing Table, the USB3 link between the USB3 Adapter and the internal USB3 device is in U3 state, and CL2 entry is disabled in U3 state.
4.2.1.6.3#12	NT	A USB4 Port shall assert an objection to enter CL2 state if: Entry to CL2 state would delay a pending Time Sync handshake. This objection shall be asserted until the Time Sync handshake is complete.
4.2.1.6.3#13	NT	(Host Routers Only) A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a Host Interface Adapter's Routing Table, whose Path corresponds to a Transmit Descriptor Ring that disables CL2 entry.

4.2.1.6.3#14	NT	(Host Routers Only) A USB4 Port shall assert an objection to enter CL2 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a Host Interface Adapter's Routing Table and the Host Interface has a Packet to send over the Adapter.
4.2.1.6.3#15	NT	(Device Routers Only) One of its Ports is in the process of CL0s, CL1 or CL2 exit flow.
4.2.1.6.3#16	TD 4.12 TD 4.13	A USB4 Port shall assert an objection to enter CL1 state if: The *CL1 Support* bit in the Lane 0 Adapter is 0b.
4.2.1.6.3#17	NT	A USB4 Port shall assert an objection to enter CL1 state if: The *CL1 Enable* bit in the Lane 0 Adapter is 0b.
4.2.1.6.3#18	NT	A USB4 Port shall assert an objection to enter CL1 state if: There is a Transport Layer Packet to be sent over the USB4 Port.
4.2.1.6.3#19	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a PCIe Adapter's Routing Table and the PCIe Adapter is not in PCIe L1 state.
4.2.1.6.3#20	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of the Upstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message transmitted upstream is smaller than the sum of the CL1 entry and exit latency.
4.2.1.6.3#21	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a Downstream PCIe Adapter's Routing Table, and either the No-Snoop Latency value or the Snoop Latency value in the last LTR Message received by the Downstream PCIe Adapter is smaller than the sum of the CL1 entry and exit latency.
4.2.1.6.3#22	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a DP IN Adapter's Routing Table.
4.2.1.6.3#23	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a DP OUT Adapter's Routing Table and a Packet is issued from the DP OUT Adapter.
4.2.1.6.3#24	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a USB3 Adapter's Routing Table and the USB3 link between the USB3 Adapter and the internal USB3 device is not in U2 or U3 state.
4.2.1.6.3#25	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a USB3 Adapter's Routing Table, the USB3 link between the USB3 Adapter and the internal USB3 device is in U3 state, and CL1 entry is disabled in USB U3 state.

4.2.1.6.3#26	NT	A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a USB3 Adapter's Routing Table, the USB3 Adapter is in USB U3 state, and CL1 entry is disabled in USB U3 state.
4.2.1.6.3#27	NT	A USB4 Port shall assert an objection to enter CL1 state if: Entry to CL1 state would delay a pending Time Sync handshake.
4.2.1.6.3#28	NT	(Host Routers Only) A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a Host Interface Adapter's Routing Table, whose Path corresponds to a Transmit Descriptor Ring that disables CL1 entry.
4.2.1.6.3#29	NT	(Host Routers Only) A USB4 Port shall assert an objection to enter CL1 state if: The Lane 0 Adapter is referenced in an *Egress Adapter* field of a Host Interface Adapter's Routing Table and the Host Interface has a Packet to send over the Adapter.
4.2.1.6.3#30	NT	(Device Routers Only) One of its Ports is in the process of CL0s, CL1 or CL2 exit flow.
4.2.1.6.4 Behavior in State		
4.2.1.6.4#1	TD 4.10 TD 4.11	While in CL2 state, the transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.1.6.4#2	TD 4.12 TD 4.13	While in CL1 state, the transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.1.6.4#3	TD 4.14 TD 4.15	While in CL0s state, the transmitter at the requesting USB4 Port shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.1.6.4#4	TD 4.10 TD 4.11 TD 4.12 TD 4.13 TD 4.14 TD 4.15	Receiver termination shall be maintained in CL0s CL1, and CL2 states.
4.2.1.6.5 Exit from State		
4.2.1.6.5#1	TD 4.16	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: An objection is set in the USB4 Port that would have prevented the Adapter from entering the low power state.

4.2.1.6.5#2	NT	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: The Adapter is in CL0s state and a CL2_REQ Ordered Set or a CL1_REQ Ordered Set is received from the Link Partner.
4.2.1.6.5#3	NT	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: The Adapter is in CL0s state and it detects Link errors that cause the Adapter to transition to Training state.
4.2.1.6.5#4	NT	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: The Adapter is in a CL1 state or a CL2 state and it is referenced in an *Egress Adapter* field of a Lane Adapter's Routing Table and the other Adapter's receiver is exiting from CL0s, CL1, or CL2 states.
4.2.1.6.5#5	NT	A Lane Adapter shall initiate transition out of CL2, CL1, or CL0s state when: The Adapter is in CL0s state and it is referenced in an *Egress Adapter* field of a Lane Adapter's Routing Table and the other Adapter's receiver is exiting from CL0s, CL1, or CL2 states.
4.2.1.6.5.1 Exit Flow from CL0s State		
4.2.1.6.5.1#1	TD 4.14 TD 4.15 TD 4.38 TD 4.16	The USB4 Port initiating exit from CL0s state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on all Lanes for the duration of at least 16 LFPS cycles.
4.2.1.6.5.1#2	TD 4.16	The USB4 Port initiating exit from CL0s state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.1#3	TD 4.16	The USB4 Port initiating exit from CL0s state shall: 3. Start transmitting SLOS1 on each Lane of the USB4 Port. Any received CL_WAKE Ordered Sets shall be ignored.
4.2.1.6.5.1#4	TD 4.16	The USB4 Port initiating exit from CL0s state shall: 4. On detection of 2 back-to-back TS2 Ordered Sets, stop sending SLOS1 and send at least 16 TS2 Ordered Sets.
4.2.1.6.5.1#5	TBD	The first TS2 Ordered Set shall be sent within tTrainingTransition after detection of the second TS2 Ordered Set.
4.2.1.6.5.1#6	NT	Before transmitting the first TS2 Ordered Sets: The scrambler shall load a new seed; Activate RS-FEC; Enable SSC if SSC is disabled.
4.2.1.6.5.1#7	TBD	If the receiver did not detect 2 back-to-back TS2 Ordered Sets within tTrainingAbort2 time after the transmitter started sending SLOS1 it shall initiate a Disconnect by driving SBTX to a logical low state for a minimum of tDisconnectTx.
4.2.1.6.5.1#8	TD 4.16	The USB4 Port initiating exit from CL0s state shall: 5. Transition to CL0 state.

4.2.1.6.5.1#9	TD 4.16	If the USB4 Port operated as a Dual-Lane Link prior to entry to CL0s state, the USB4 Port shall resume operation as a Dual-Lane Link independent of the setting of the TS2 Ordered Sets. A de-skew Ordered Set shall be sent. The scrambler shall load a new seed.
4.2.1.6.5.1#10	NT	If the Router initiated exit from CL0s state due to receiving CL1_REQ or CL2_REQ Ordered Sets, then the Router shall respond to the request Ordered Sets. The Router shall not send any Transport Layer Packets before completing the CLx entry flow.
4.2.1.6.5.1#11	TD 4.14 TD 4.15	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 1. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. An Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.1#12	TD 4.14 TD 4.15	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 2. On reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols by the Lane 0 Adapter, transmit 16 CL_WAKE2.X Ordered Set Symbols on each enabled Lane of the USB4 Port.
4.2.1.6.5.1#13	TD 4.38	If 3 back-to-back CL_WAKE1.(X+1) Ordered Set Symbols or 3 back-to-back SLOS Symbols are not received within tCL0sSwitch time after receiving a CL_WAKE1.X Ordered Set Symbol, then the Adapter shall transition to the Training.LOCK1 sub-state.
4.2.1.6.5.1#14	NT	If the Router initiated exit from CL0s state by sending CL1_REQ or CL2_REQ Ordered Sets, then the Router shall continue sending the Ordered Sets instead of sending Transport Layer Packets. The Router shall not send any Transport Layer Packets after sending the first CL1_REQ or a CL2_REQ Ordered Set.
4.2.1.6.5.1#15	TD 4.14 TD 4.15	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 3. On detection of 3 back-to-back SLOS Symbols by all enabled Adapters of the USB4 Port, transmit 16 TS2 Ordered Sets in each enabled Lane of the USB4 Port
4.2.1.6.5.1#16	TD 4.14 TD 4.15	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 4. On detection of 2 back-to-back TS2 Ordered Sets, transition to CL0 state: If the Router initiated exit from CL0s state by sending CL1_REQ or CL2_REQ Ordered Sets, then the Router shall continue to send the Ordered Sets. The Router shall not send any Transport Layer Packets before completing the CLx entry flow.
4.2.1.6.5.1#17	TD 4.38	Upon detecting 2 LFPS cycles, a Lane Adapter in CL0s state shall: 4. On detection of 2 back-to-back TS2 Ordered Sets, transition to CL0 state: If the Adapter does not detect 2 back-to-back TS2 Ordered Sets in tTS2Timeout from transmitting TS2 Ordered Sets, the Lane Adapters in the Port shall enter the Training state.

4.2.1.6.5.1#18	TBD	In order to limit the CL0s exit time to 230µs, a Router shall comply with the following equation: tWarmUpCL0s = 6 x tWakeResponse + tTrainingTransition < 80 µs.
4.2.1.6.5.2 Exit Flow from CL1 or CL2 State (No Re-timers on the Link)		
4.2.1.6.5.2#1	TD 4.16	The USB4 Port initiating exit from CL1 or CL2 state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on each Lane until the receiver detects LFPS.
4.2.1.6.5.2#2	TBD	If the receiver did not detect LFPS after tTrainingAbort2 time the Router shall initiate a Disconnect by driving SBTX to a logical low state for a minimum of tDisconnectTx.
4.2.1.6.5.2#3	TD 4.16	The USB4 Port initiating exit from CL1 or CL2 state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.2#4	TD 4.16	The USB4 Port initiating exit from CL1 or CL2 state shall: 3. Start transmitting SLOS1 on the Lane.
4.2.1.6.5.2#5	TD 4.16	The USB4 Port initiating exit from CL1 or CL2 state shall: 4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.2#6	TD 4.16	The USB4 Port initiating exit from CL1 or CL2 state shall: 5. Transition the Lane Adapter to Training.LOCK1 sub-state.
4.2.1.6.5.2#7	NT	On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.
4.2.1.6.5.2#8	TD 4.10 TD 4.12	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on the Lane for the duration of at least 3 LFPS cycles.
4.2.1.6.5.2#9	TD 4.10 TD 4.12	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.2#10	TD 4.10 TD 4.12	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 3. Start transmitting SLOS1 on the Lane.
4.2.1.6.5.2#11	TD 4.10 TD 4.12	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.2#12	TD 4.10 TD 4.12	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 5. Transition to Training.LOCK1 sub-state.

4.2.1.6.5.2#13	TD 4.10 TD 4.12	On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled
4.2.1.6.5.3 Exit Flow from CL1 or CL2 State (Re-timers on the Link)		
4.2.1.6.5.3#1	TD 4.16	The USB4 Port initiating exit from CL1 or CL2 state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on each Lane until its receiver detects LFPS.
4.2.1.6.5.3#2	TBD	If the receiver did not detect LFPS after tTrainingAbort2 time the Router shall initiate a Disconnect by driving SBTX to a logical low state for a minimum of tDisconnectTx.
4.2.1.6.5.3#3	TD 4.16	The USB4 Port initiating exit from CL1 or CL2 state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.3#4	TD 4.16	The USB4 Port initiating exit from CL1 or CL2 state shall: 3. Start transmitting SLOS1 on the Lane.
4.2.1.6.5.3#5	TD 4.16	The USB4 Port initiating exit from CL1 or CL2 state shall: 4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.3#6	TD 4.16	The USB4 Port initiating exit from CL1 or CL2 state shall: 5. Upon reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols, start transmitting CL_WAKE2.X Ordered Set Symbols on the Lane. The Adapter shall ignore any received CL_WAKE2.Y (where Y is any value) Symbols interleaved with CL_WAKE1.X Ordered Set SymbolCL_WAKE1.X Ordered Set Symbols when it determines the reception of back-to-back CL_WAKE1.X Ordered Set SymbolCL_WAKE1.X Ordered Set Symbols.
4.2.1.6.5.3#7	TD 4.16	The USB4 Port initiating exit from CL1 or CL2 state shall: 6. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, transition the Adapter to Training.LOCK1 sub-state.
4.2.1.6.5.3#8	NT	On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.
4.2.1.6.5.3#9	TD 4.11 TD 4.13	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 1. Send a Low Frequency Periodic Signaling (LFPS) burst on the Lane for the duration of at least 3 LFPS cycles.
4.2.1.6.5.3#10	TD 4.11 TD 4.13	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 2. Return to Electrical Idle for tPreData.
4.2.1.6.5.3#11	TD 4.11 TD 4.13	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 3. Start transmitting SLOS1 on the Lane.

4.2.1.6.5.3#12	TD 4.11 TD 4.13	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. An Adapter shall complete Symbol lock within tRxLock time.
4.2.1.6.5.3#13	TD 4.11 TD 4.13	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 5. Upon reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols, start transmitting CL_WAKE2.X Ordered Set Symbols on the Lane. The Adapter shall ignore any received CL_WAKE2.Y (where Y is any value) Symbols interleaved with CL_WAKE1.X Ordered Set Symbols when it determines the reception of back-to-back CL_WAKE1.X Ordered Set Symbols.
4.2.1.6.5.3#14	TD 4.11 TD 4.13	Upon detecting 2 LFPS cycles, a Lane Adapter in CL1 or CL2 state shall: 6. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, transition to Training.LOCK1 sub-state.
4.2.1.6.5.3#15	TD 4.11 TD 4.13	On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.
4.2.2 USB4 Link Transitions		
4.2.2#1	IOP	A USB4 Link shall operate as either a Single-Lane Link or a Dual-Lane Link.
4.2.2.1 Transition from One Single-Lane Link to Two Single-Lane Links		
4.2.2.1#1	NT	A USB4 Port shall transition from one single-Lane Link to two single-Lane Links when the Lane 1 Adapter is enabled.
4.2.2.2 Transition from Two Single-Lane Link to Dual-Lane Link		
4.2.2.2#1	TD 4.5	A USB4 Port shall transition its Lane Adapters to the Bonding state when all of the following are true: Both Ports are in the Bonding state; The Supported Link Widths field of both Ports is set to x2 support or more; The Target Link Width field of both Ports is set to establish a dual-Lane Link.
4.2.2.2#2	TD 4.5	The Logical Layer shall transition to a dual-Lane Link when the following conditions are met: Both Adapters have transitioned successfully to CL0 state tBonding time after entry to Lane Bonding state; Link Partner has responded with the following value in all TS1 and TS2 Ordered Sets on both Lanes (Lane Bonding Target is set to 001b).
4.2.2.2#3	TD 4.5	If Lane bonding is successful, then a Router shall set the Adapter State field in the Lane Adapter Configuration Capability of the Lane 0 Adapter to CL0.
4.2.2.2#4	TD 4.5	If Lane bonding is successful, then a Router shall set the Negotiated Link Width field in the Lane Adapter Configuration Capability of the Lane 0 Adapter to indicate a USB4 Link width of x2.
4.2.2.2#5	TD 4.5	If Lane bonding is successful, then a Router shall send a Hot Plug Event Packet with the UPG bit set to 1b for the Lane 1 Adapter.

4.2.2.2#6	TD 4.35	If one of the Lane Adapters is not in CL0 tBonding time after entry to the Lane Bonding state, the Router shall initiate a Disconnect by driving SBTX to a logical low state for a minimum of tDisconnectTx.
4.2.2.2#7	TD 4.20	The Adapters of a dual-Lane Link operate in CL0 state in tandem with the following dependencies: Any Ordered Set sent on the Link shall be sent simultaneously on both Lanes within the permitted transmit skew.
4.2.2.2#8	BC	The Adapters of a dual-Lane Link operate in CL0 state in tandem with the following dependencies: When either Adapter of a dual-Lane Link transitions to one of the Training sub-states, the other Adapter in the USB4 Port shall transition to the same Training sub-state.
4.2.2.2.1 Training a Dual-Lane Link		
4.2.2.2.1#1	TD 4.40 TD 4.41	When an Adapter that is part of a dual-Lane Link enters Training state, the other Adapter in the USB4 Port shall enter Training state as well.
4.2.2.2.1#2	TD 4.9	The Logical Layer shall resume dual-Lane Link operation if both Ports meet the transition conditions in Step 6 of the Training state machine in Table 4-20 within tTrainingAbort2 time.
4.2.2.2.1#3	TD 4.9	The Adapter that transitions to the CL0 state first shall send TS2 Ordered Sets until the other Adapter in the USB4 Port exits the training state.
4.2.2.3 Transition from Dual-Lane Link to Two Single-Lane Links		
4.2.2.4 Transition from Two Single-Lane Links to One Single Lane Link		
4.2.2.4#1	TD 4.6	A USB4 Port shall transition from two Single-Lane Links to one Single-Lane Link when one of its Adapters transitions to the Disabled state.
4.2.3 Logical Layer Link States		
4.3 USB4 Link Encoding		
4.3#1	IOP	If RS_FEC encoding is off, bytes received from the Transport Layer shall be encoded with either 64b/66b encoding (Gen 2) or 128b/132b encoding (Gen 3)
4.3.1 Lane Distribution		
4.3.1#1	IOP	If a USB4 Link operates as a dual-Lane Link, then distribution of Transport Layer bytes among the Lanes shall alternate as depicted in Figure 4-13.
4.3.2 Symbol Encoding		
4.3.2.1 Symbol Encoding of Transport Layer Bytes		
4.3.2.1#1	NT	A Symbol may contain either Transport Layer bytes or Ordered Set, but shall not contain both

4.3.3 Ordered Sets		
4.3.3#1	IOP	Ordered Set shall have the structure depicted in Table 4-35.
4.3.3#2	IOP	For 64b/66b encoding, an Ordered Set Symbol shall contain a single copy of the Ordered Set payload and 2 Sync Bits.
4.3.3#3	IOP	For 128b/132b encoding, an Ordered Set Symbol shall contain two copies of the Ordered Set (i.e. 64 bits followed by a second copy of the same 64 bits) and 4 Sync Bits.
4.3.4 Bit Swap		
4.3.4#1	IOP	Bit Swap of Transport Layer bytes and of Ordered Sets payload delivered to the scrambler in the order that they are transmitted on the wire.
4.3.4.1 Sync Bits		
4.3.4.1#1	IOP	If RS-FEC is off, all Symbols shall be transmitted Sync Bits first.
4.3.4.1#2	IOP	Sync Bits shall be sent in the order of most significant bit to least significant bit.
4.3.4.1#3	IOP	Transport Layer bytes or Ordered Sets shall be transmitted after the Sync Bits.
4.3.4.2 Data Symbol Payload		
4.3.4.2#1	IOP	The payload within a Data Symbol shall be transmitted from left to right as depicted in Figure 4-18.
4.3.4.2#2	IOP	Within each byte of payload, individual bits shall be transmitted from bit 0 to bit 7.
4.3.4.3 Ordered Set Symbol Payload		
4.3.4.3#1	IOP	When an Ordered Set is longer than 64 bits (i.e. SLOS, CL_WAKE1.X, CL_WAKE2.X), it cannot fit into the payload of one Symbol, and shall be divided into multiple Symbol payloads.
4.3.4.3#2	IOP	The Ordered Set shall be transmitted in increasing Symbols, starting with Symbol 0.
4.3.4.3#3	IOP	Within a Symbol payload, the bytes in an Ordered Set shall be transmitted from left to right as depicted in Figure 4-19.
4.3.4.3#4	IOP	Within each byte, individual bits shall be transmitted from bit 0 to bit 7.
4.3.5 Scrambling		
4.3.5#1	IOP	Scrambling shall be performed according to the rules in Table 4-36.

4.3.5#2	IOP	Scrambling and de-scrambling are performed by passing the encoded bits through an Additive LFSR with a polynomial of G(X) = X^23 + X^21 + X^16 + X^8 + X^5 + X^2 + 1.
4.3.5#3	IOP	The most significant bit of the LFSR is XORed with the data stream on a per-bit basis. The data stream is scrambled in the order that it is sent on wire.
4.3.5#4	IOP	The scrambler shall load a new seed on the following transitions: 1. Transition from LOCK2 sub-state to TS1 sub-state in the Training state; Initial value is 1F EEDDh.
4.3.5#5	IOP	The scrambler shall load a new seed on the following transitions: 2. On exit from CL0s state, before the Adapter initiating exit transmits the first TS2 Ordered Set in the direction exiting electrical idle; Initial value is 1F EEDDh.
4.3.5#6	IOP	The scrambler shall load a new seed on the following transitions: 3. On transition from any state to CL0 when going to a dual-Lane Link; When exiting CL0s state, a new seed shall be loaded only in the direction exiting electrical idle; Initial value on the Lane 0 is 1D BFBCh; Initial value on the Lane 1 is 06 07BBh; The per-Lane seeds are used, starting with the first byte after the de-skew Ordered Set.
4.3.5#8	IOP	Any single-bit errors in the SRC field shall be corrected. If the SCR field contains an uncorrectable error, the Logical Layer reports an OSE error.
4.3.6 RS-FEC		
4.3.6#1	IOP	An Adapter shall support RS-FEC at all speeds.
4.3.6#2	IOP	Each block of 194 bytes shall be generated in the following manner: Transport Layer bytes and Ordered Sets are grouped into 16-byte (128 bit) Symbol payloads. Each Symbol payload may contain either one or more Ordered Set or Transport Layer bytes, but shall not contain both.
4.3.6#3	IOP	Each block of 194 bytes shall be generated in the following manner: When operating at Gen 2 speed, the 16-byte Ordered Set Symbol payload shall contain: For a SLOS Ordered Set, 128 bits of the Ordered Set.
4.3.6#4	IOP	Each block of 194 bytes shall be generated in the following manner: When operating at Gen 2 speed, the 16-byte Ordered Set Symbol payload shall contain: For all other Ordered Sets, two 64-bit Ordered Sets.
4.3.6#5	IOP	When only one Ordered Set needs to be sent, the second Ordered Set shall be a SKIP Ordered Set. See Section 4.4.3 for the structure of a SKIP Ordered Set.
4.3.6#6	IOP	Each block of 194 bytes shall be generated in the following manner: When operating at Gen 3 speed, the 16-byte Ordered Set Symbol payload shall contain: For a SLOS Ordered Set, 128 bits of the Ordered Set.

4.3.6#7	IOP	Each block of 194 bytes shall be generated in the following manner: When operating at Gen 3 speed, the 16-byte Ordered Set Symbol payload shall contain: For all other Ordered Sets, two copies of the Ordered Set (i.e. 64 bits followed by a second copy of the same 64 bits).
4.3.6#8	IOP	Each block of 194 bytes shall be generated in the following manner: The RS-FEC encoder is fed with twelve 16-byte Symbol payloads plus 2 bytes of Sync Bits. Each Symbol is allocated a single Sync Bit, indicating whether it contains Transport Layer bytes (Sync Bit = 0b) or Ordered Set (Sync Bit = 1b).
4.3.6#9	IOP	The 2 bytes of Sync Bits contain 12 active bits (one per 16-byte Symbol) and 4 reserved bits.
4.3.6#10	IOP	Sync Bits shall be delivered to the encoder in order that they will be sent to the wire, from bit 15 to bit 0. The active Sync Bits reside in bits[11:0] of the Word. The Sync Bit corresponding to the oldest 16-byte Symbol resides in bit 0 if the Sync Bits.
4.3.6#11	IOP	The 12 active bits are XORed with 333h before being fed to the RS-FEC encoder. The XORed value is the value seen on the wire.
4.3.6#12	IOP	Each block of 194 bytes shall be generated in the following manner: The RS-FEC encoder generates 4 bytes of redundancy bits (P3 to P0). P3 is the first byte to be sent on the wire and P0 is the last. Within each byte, bits are sent in descending order where bit 7 is sent first and bit 0 is sent last.
4.3.6#13	TD 4.39	The RS-FEC decoder shall correct a received block with up to two 1-byte errors anywhere in the block.
4.3.6#14	NT	An error in a received block that is detectable and uncorrectable shall cause an RDE error.
4.3.6.1 RS_FEC Activation and Deactivation		
4.3.6.1#1	IOP	If RS-FEC is enabled during Phase 3 of Lane Initialization, then an Adapter shall activate RS-FEC encoding in the following cases: In Training state, immediately following the last transmitted SLOS2 and before sending the first TS1 Ordered Set.
4.3.6.1#2	IOP	If RS-FEC is enabled during Phase 3 of Lane Initialization, then an Adapter shall activate RS-FEC encoding in the following cases: During exit from CL0s state, immediately before sending the first TS2 Ordered Set.
4.3.6.1#3	IOP	A START_RS_FEC bit sequence shall be sent prior to activating RS-FEC encoding on the Lane.
4.3.6.1#4	IOP	The bit sequence shall not be scrambled and shall not advance the scrambler LFSR.
4.3.6.1#5	IOP	The START_RS_FEC bit sequence shall be sent with bit[31] first on the wire.

4.3.6.1#6	IOP	During exit from CL0s state, the START_RS_FEC bit sequence shall only be sent in the direction exiting electrical idle.
4.3.6.1#7	IOP	The bit following the START_RS_FEC bit sequence shall be the first bit to be RS-FEC encoded.
4.3.6.1#8	IOP	A USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: When to Training state, after transmitting n SLOS1 Symbols in LOCK1 sub-state with RS-FEC on, where 32=<n<=64 in Gen 2 and 16=<n<=32 in Gen 3.
4.3.6.1#9	IOP	A USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to Disabled state.
4.3.6.1#10	IOP	A USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to CLd state.
4.3.6.1#11	IOP	A USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to CL0s state, in the direction entering low power state.
4.3.6.1#12	IOP	A USB4 Port shall deactivate RS-FEC encoding on a Lane in the following cases: Entry to CL2 or CL1 states.
4.3.6.2 Pre-Coding		
4.3.6.2#1	IOP	If pre-coding is on, then before each bit is sent on the wire, it shall be XOR'ed with the bit sent before it, using the value of the bit after it was coded.
4.3.6.2#2	IOP	Pre-coding shall be turned on with the first bit that is RS_FEC encoded.
4.3.6.2#3	IOP	Pre-coding shall be turned off with the first bit that is not RS_FEC encoded.
4.4 USB4 Link Operation		
4.4.1 Start of Data		
4.4.1#1	BC	When an Adapter transitions to CL0 state, the first transmitted bytes after the last TS2 Ordered Set shall be either a Transport Layer header, an Idle Packet or any Ordered Set other than SLOS, TS1 or TS2.
4.4.1#2	BC	For a dual-Lane Link, the first transmitted bytes after the last TS2 Ordered Set shall be a de-skew Ordered Set followed by either a Transport Layer header, an Idle Packet or any Ordered Set other than SLOS, TS1 or TS2.
4.4.2 Error Cases and Recovery		
4.4.2#1	TD 4.40	A Router shall support the Ordered Set Errors (OSE) error case.
4.4.2#2	TD 4.40	When a Router supports an error case, it shall do so as described in this section.

4.4.2#3	TD 4.40	A Router shall support the same error cases on all Lane Adapters.
4.4.2#4	TD 4.40 TD 4.41 TD 4.42	When an Adapter supports an error case, it shall support that error case in all Adapter states unless specified otherwise.
4.4.2#5	NT	If an Adapter reports Alignment Lock Errors, when an Adapter receives a Symbol with illegal Sync bit values, it shall go to Training.LOCK1 sub-state.
4.4.2#6	NT	If an Adapter reports Alignment Lock Errors, when an Adapter receives a Symbol with illegal Sync bit values, it shall set the ALE bit in the Logical Layer Errors field to 1b.
4.4.2#7	NT	If an Adapter reports Alignment Lock Errors, when an Adapter receives a Symbol with illegal Sync bit values, if the ALE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#8	NT	If an Adapter reports Alignment Lock Errors, when an Adapter receives a Symbol with illegal Sync bit values, if the ALE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#9	TD 4.40	If an Adapter reports Ordered Set Errors, when it receives 2 back-to-back Symbols that contain an Ordered Set that is not defined in this specification and/or have an uncorrectable error in the SRC field, it shall go to Training.LOCK1 sub-state.
4.4.2#10	TD 4.40 TD 4.41	If an Adapter reports Ordered Set Errors, when it receives 2 back-to-back Symbols that are not part of an Ordered Set defined in this specification and/or have an uncorrectable error in the SRC field, it shall set the OSE bit in the Logical Layer Errors field to 1b.
4.4.2#11	TD 4.40 TD 4.41	If an Adapter reports Ordered Set Errors, when it receives 2 back-to-back Symbols that are not part of an Ordered Set defined in this specification and/or have an uncorrectable error in the SRC field, if the OSE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#12	TD 4.40 TD 4.41	If an Adapter reports Ordered Set Errors, when it receives 2 back-to-back Symbols that are not part of an Ordered Set defined in this specification and/or have an uncorrectable error in the SRC field, if the OSE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#13	NT	If an Adapter reports Timeout Errors, when an Adapter does not transition from Training state to CL0 state within tTrainingError after achieving Symbol alignment, it shall go to LOCK1 state.
4.4.2#14	TD 4.42	If an Adapter reports Timeout Errors, when an Adapter does not transition from Training state to CL0 state within tTrainingError after achieving Symbol alignment, it shall set the TE bit in the Logical Layer Errors field to 1b.

4.4.2#15	TD 4.42	If an Adapter reports Timeout Errors, when an Adapter does not transition from Training state to CL0 state within tTrainingError after achieving Symbol alignment, if the TE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#16	TD 4.42	If an Adapter reports Timeout Errors, when an Adapter does not transition from Training state to CL0 state within tTrainingError after achieving Symbol alignment, if the TE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#17	NT	If an Adapter reports Elastic Buffer Errors, when the elastic buffer is full, it shall: go to Training.LOCK1 sub-state.
4.4.2#18	NT	If an Adapter reports Elastic Buffer Errors, when the elastic buffer is full, it shall set the EBE bit in the Logical Layer Errors field to 1b.
4.4.2#19	NT	If an Adapter reports Elastic Buffer Errors, when the elastic buffer is full, if the EBE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager (see Section 6.5).
4.4.2#20	NT	If an Adapter reports Elastic Buffer Errors, when the elastic buffer is full, if the EBE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#21	NT	If an Adapter reports De-skew Buffer Errors, when skew is too large resulting in overflow in the de-skew buffer, it shall set the DBE bit in the Logical Layer Errors field to 1b.
4.4.2#22	NT	If an Adapter reports De-skew Buffer Errors, when skew is too large resulting in overflow in the de-skew buffer, if the DBE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#23	NT	If an Adapter reports De-skew Buffer Errors, when skew is too large resulting in overflow in the de-skew buffer, if the DBE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#24	NT	If an Adapter reports RS-FEC decoder errors, when the RS-FEC decoder identifies an uncorrectable error, it shall turn off RS-FEC in both directions of the Link.
4.4.2#25	NT	If an Adapter reports RS-FEC decoder errors, when the RS-FEC decoder identifies an uncorrectable error, it shall set the RDE bit in the Logical Layer Errors field to 1b.
4.4.2#26	NT	If an Adapter reports RS-FEC decoder errors, when the RS-FEC decoder identifies an uncorrectable error, if the RDE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.

4.4.2#27	NT	If an Adapter reports RS-FEC decoder errors, when the RS-FEC decoder identifies an uncorrectable error, if the RDE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.2#28	NT	If an Adapter reports RX Sync Timeout, if, while in LOCK1 sub-state of the Training state, the receiver cannot lock on Sync Bits for an implementation-specific period of time, it shall remain in LOCK1 sub-state.
4.4.2#29	NT	If an Adapter reports RX Sync Timeout, if, while in LOCK1 sub-state of the Training state, the receiver cannot lock on Sync Bits for an implementation-specific period of time, it shall set the RST bit in the Logical Layer Errors field to 1b.
4.4.2#30	NT	If an Adapter reports RX Sync Timeout, if, while in LOCK1 sub-state of the Training state, the receiver cannot lock on Sync Bits for an implementation-specific period of time, if the RST bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager.
4.4.2#31	NT	If an Adapter reports RX Sync Timeout, if, while in LOCK1 sub-state of the Training state, the receiver cannot lock on Sync Bits for an implementation-specific period of time, if the RST bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
4.4.3 Clock Compensation and SKIP		
4.4.3#1	IOP	A receiver shall drop any received SKIP Ordered Sets and shall be capable of operating in the absence of any SKIP Ordered sets.
4.4.3#2	IOP	A Transmitter shall not send SKIP Ordered Sets while the Adapter is in the Training.LOCK1 or Training.LOCK2 sub-states.
4.4.3#3	IOP	A SKIP Ordered Set shall have the structure defined in Table 4-39.
4.4.3#4	IOP	SCR – Shall be set to 11 0000 1101b to indicate that the Ordered Set contents are not scrambled.
4.4.4 Dual-Lane Skew		
4.4.4#1	TD 4.43	A Router shall operate with skew defined in Section 3.5.1 between the receiving Lanes of a Link when measured at the USB Type-C connector.
4.4.4#2	NT	A transmitter shall not introduce skew more than defined in Section 3.4.1.
4.4.4#3	TD 4.9	A single de-skew Ordered Set shall be sent on each Lane after both Adapters transition (from any state) to CL0 state, and the USB4 Port in Dual-Lane Link mode.
4.4.4#4	TD 4.9	When exiting CL0s state, a de-skew Ordered Set shall only be sent in the direction exiting electrical idle.
4.4.4#5	TBD	When a Port operates at Gen 3 speed, the De-Skew Ordered Set shall be transmitted twice. Otherwise it shall be transmitted once.

4.4.4#6	TD 4.9	A de-skew Ordered Set shall be sent simultaneously on both Lanes within the permitted transmit skew
4.4.4#7	TD 4.9	A de-skew Ordered Set shall be sent on both Lanes in the same locations within the Symbol.
4.4.4#8	TD 4.9	The de-skew Ordered Set shall be the first bytes sent after the TS2 Ordered Sets.
4.4.4#9	TD 4.9	TS2 Ordered Sets shall be transmitted on a Lane in CL0 state until the de-skew Ordered Set is sent.
4.4.4#10	NT	SCR in the De-Skew Ordered Set payload shall be set to 00 1111 0010b to indicate that the Ordered Set contents are scrambled.
4.4.5 Disconnect		
4.4.5.1 Upstream Facing Port Disconnect		
4.4.5.1.1 SBRX Goes Low		
4.4.5.1.1#1	TD 4.17	The Router with the disconnected Port shall: Drive SBTX to a logical low state on all USB4 Ports for a minimum of tDisconnectTx.
4.4.5.1.1#2	TD 4.17	The Router with the disconnected Port shall: Transition to the Uninitialized Unplugged state.
4.4.5.1.1#3	CH6	The following events initiate a disconnect as defined in this section: Router Hot Unplug.
4.4.5.1.1#4	CH6	The following events initiate a disconnect as defined in this section: Downstream Facing Port Reset where the Link Partner is an Upstream Facing Port.
4.4.5.1.1#5	TD 4.17	The following events initiate a disconnect as defined in this section: The Domain enters Sleep state, the USB4 Port is Configured bit in a USB4 Port is set to 0b, and the Link Partner is an Upstream Facing Port.
4.4.5.1.1#6	TBD	The following events initiate a disconnect as defined in this section: The Link Partner failed to train the Link before the defined timeout.
4.4.5.1.1#7	TBD	The following events initiate a disconnect as defined in this section: The Lane bonding did not complete before the defined timeout.
4.4.5.1.2 LT_Fall Transaction is Received		
4.4.5.1.3 LT_LRoff Transaction is Received on an Upstream Facing Port		
4.4.5.1.3#1	TD 4.21 TD 4.22	When an Upstream Facing Port receives an LT_LRoff transaction and the *Enter Sleep* bit in the Router Configuration Space is set to 0b, the Port is disconnected. The disconnected Port shall send an LT_LRoff Transaction.

4.4.5.1.3#2	TD 4.21 TD 4.22	The Router with the disconnected Port shall: Drive SBTX to a logical low state on all USB4 Ports for a minimum of tDisconnectTx.
4.4.5.1.3#3	NT	The Router with the disconnected Port shall: Transition to the Uninitialized Unplugged state.
4.4.5.1.3#4	NT	The following events shall initiate a disconnect as defined in this section: The Domain enters Sleep state, in the Downstream Facing Port of the Link Partner the USB4 Port is Configured bit is 0b and the Enable Wake on Connect bit of the USB4 Port is 1b.
4.4.5.2 Downstream Port Disconnect		
4.4.5.2.1 SBRX Goes Low		
4.4.5.2.1#1	TD 4.18	When a Downstream Facing Port detects SBRX at logical low state for tDisconnectRx, the Port is disconnected and shall: Send an LT_LRoff Transaction.
4.4.5.2.1#2	TD 4.18	When a Downstream Facing Port detects SBRX at logical low state for tDisconnectRx, the Port is disconnected and shall: Discard any Transport Layer Packets received from the Ingress Port(s) on the Router.
4.4.5.2.1#3	TD 4.18	When a Downstream Facing Port detects SBRX at logical low state for tDisconnectRx, the Port is disconnected and shall: Transition its Adapters to the CLd state
4.4.5.2.1#4	NT	The Router with the disconnected Port shall continue to send flow control Packets on the Ingress Port(s) for Transport Layer Packets that the disconnected Port discarded.
4.4.5.2.1#5	NT	Flow control credit counts shall be updated as if the discarded packets were dequeued and forwarded to the Egress Adapter.
4.4.5.2.1#6	TD 4.18	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Send the Connection Manager a Hot Plug Event Packet with the *UPG* bit set to 1b.
4.4.5.2.1#7	TD 4.18	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Load the following fields in the Adapter Configuration Space with their default values: Basic Configuration Registers: Link Credits Allocated; TMU Adapter Configuration Capability: Inter-domain Slave; Lane Adapter Configuration Capability: Target Link Width CL0s Enable CL1 Enable CL2 Enable Lane Bonding.
4.4.5.2.1#8	NT	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Load the TxFFE register in the SB Register Space with its default values.

4.4.5.2.2 LT_LRoff Transaction is Received		
4.4.5.2.2#1	TD 4.19	When a Downstream Facing Port receives an LT_LRoff Transaction and the *Enter Sleep* bit in the Router Configuration Space is set to 0b, the Port is disconnected and shall: Send an LT_LRoff Transaction.
4.4.5.2.2#2	NT	When a Downstream Facing Port receives an LT_LRoff Transaction and the *Enter Sleep* bit in the Router Configuration Space is set to 0b, the Port is disconnected and shall: Discard any Transport Layer Packets received from the Ingress Port(s) on the Router.
4.4.5.2.2#3	TD 4.19	When a Downstream Facing Port receives an LT_LRoff Transaction and the *Enter Sleep* bit in the Router Configuration Space is set to 0b, the Port is disconnected and shall: Transition its Adapters to the CLd state.
4.4.5.2.2#4	NT	The Router with the disconnected Port shall continue to send flow control Packets on the Ingress Port(s) for Transport Layer Packets that the disconnected Port discarded.
4.4.5.2.2#5	NT	Flow control credit counts shall be updated as if the discarded packets were dequeued and forwarded to the Egress Adapter.
4.4.5.2.2#6	TD 4.19	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Send the Connection Manager a Hot Plug Event Packet with the UPG bit set to 1b.
4.4.5.2.2#7	TD 4.19	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Load the following fields in Adapter Configuration Space with their default values: Basic Configuration Registers: Link Credits Allocated; TMU Adapter Configuration Capability: Inter-domain Slave; Lane Adapter Configuration Capability: Target Link Width CL0s Enable CL1 Enable CL2 Enable Lane Bonding.
4.4.5.2.2#8	NT	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Load the TxFFE register in SB Register Space with its default values.
4.4.5.2.2#9	TD 4.19	The Router shall do the following for each enabled Lane Adapter in the disconnected Port: Start Lane Initialization.
4.4.6 Lane Adapter Disable and Enable		
4.4.6.1 Disabled Adapter is the Upstream Adapter		
4.4.6#1	NT	After the *Lane Disable* bit in its Upstream Adapter is set to 1b, a Router shall: 1. Send an LT_Fall Transaction to the Link Partner of the Upstream Facing Port to signal transition to the Disabled state.
4.4.6#2	NT	After the *Lane Disable* bit in its Upstream Adapter is set to 1b, a Router shall: 2. Drive SBTX to a logical low state on all USB4 Ports for a minimum of tDisconnectTx.

4.4.6#3	NT	After the *Lane Disable* bit in its Upstream Adapter is set to 1b, a Router shall: 3. Transition to the Uninitialized Unplugged state.
4.4.6#4	NT	After the *Lane Disable* bit in its Upstream Adapter is set to 1b, a Router shall: 4. Start Lane Initialization from phase 1.
4.4.6#5	NT	After the *Lane Disable* bit in its Upstream Adapter is set to 1b, a Router shall: 5. After detecting a Router on the Upstream Facing Port, transition to the Uninitialized Plugged state.
4.4.6.2 Disabled Adapter is not the Upstream Adapter		
4.4.6.2.1 Disable Flow		
4.4.6.2.1#1	TD 4.6	After the *Lane Disable* bit in the Adapter Configuration Space of the Lane Adapter is set to 1b, the Router shall: 1. Send an LT_Fall Transaction to the Link Partner of the Upstream Facing Port to signal transition to the Disabled state.
4.4.6.2.1#2	TD 4.6	After the *Lane Disable* bit in the Adapter Configuration Space of the Lane Adapter is set to 1b, the Router shall: 2. Send a Hot Plug Event Packet for the disabled Adapter with the UPG bit set to 1b to the Connection Manager.
4.4.6.2.1#3	TD 4.6	After the *Lane Disable* bit in the Adapter Configuration Space of the Lane Adapter is set to 1b, the Router shall: 3. Transition the Adapter to the Disabled State.
4.4.6.2.1#4	NT	After the *Lane Disable* bit in the Adapter Configuration Space of the Lane Adapter is set to 1b, the Router shall: 4. If the Router detects that SBRX of the disabled Adapter transitions to a low logical state for more than tDisconnectRx, the Router shall perform the disconnect flow defined in Section 4.4.5.2.1.
4.4.6.2.1.1 Link Partner is not the Upstream Adapter		
4.4.6.2.1.1#1	TD 4.7	If the Link Partner of the disabled Adapter is not the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 1. Send a Hot Plug Event Packet with the UPG bit set to 1b to the Connection Manager.
4.4.6.2.1.1#2	TD 4.7	If the Link Partner of the disabled Adapter is not the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 2. Load the following fields in the Adapter Configuration Space of the Adapter with their default values: Basic Configuration Registers: Link Credits Allocated; TMU Adapter Configuration Capability: Inter-domain Slave USB4 Port Configuration Capability: Target Link Width CL0s Enable CL1 Enable CL2 Enable Lane Bonding.
4.4.6.2.1.1#3	TD 4.7	If the Link Partner of the disabled Adapter is not the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 3. Transition to the CLd state.

4.4.6.2.1.2 Link Partner is the Upstream Adapter		
4.4.6.2.1.2#1	TD 4.7	If the Link Partner of the disabled Adapter is the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 1. Drive SBTX to a logical low state on all USB4 Ports for a minimum of tDisconnectTx.
4.4.6.2.1.2#2	TD 4.7	If the Link Partner of the disabled Adapter is the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 2. Transition to the Uninitialized Unplugged state.
4.4.6.2.1.2#3	NT	If the Link Partner of the disabled Adapter is the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 3. Transition to the Uninitialized Plugged state as a result of detecting SBRX driven high.
4.4.6.2.1.2#4	TD 4.7	If the Link Partner of the disabled Adapter is the Upstream Adapter, it shall do the following upon receiving the LT_Fall Transaction: 4. Start lane Initialization from phase 1.
4.4.6.2.2 Enable Flow		
4.4.7 Time Sync Notification Ordered Set (TSNOS)		
4.4.7#1	NT	When a Router receives a Time Sync Notification Ordered Set (TSNOS) it shall generate a time stamp.
4.4.7#2	NT	The Time Sync Notification Ordered Set shall have the structure in Table 4-41.
4.4.7#3	NT	SCR in the Time Sync Notification Ordered Set payload shall be set to 11 0000 1101b to indicate that the Ordered Set contents are not scrambled.
4.5 Sleep and Wake		
4.5.1 Entry to Sleep		
4.5.1#1	TD 4.21 TD 4.22	(Host Router) A Router shall enter sleep state when the *Enter Sleep* bit is set to 1b and one of the following sleep events occur: The Router is a PCIe Host Router and it receives a PCIe PERST# signal that transitions from logical high to logical low.
4.5.1#2	CH11	If the Router tunnels PCIe traffic, then it shall send at least 3 PERST Active Tunneled Packets on each Downstream Facing Port before entering Sleep state.
4.5.1#3	NT	(Host Router) A Router shall enter sleep state when the *Enter Sleep* bit is set to 1b and one of the following sleep events occur: The Router receives an implementation-specific signal indicating entry to Sleep state.

4.5.1#4	CH11	(Device Router) A Router shall enter sleep state when the Enter Sleep bit is set to 1b and one of the following sleep events occur: The Router tunnels PCIe traffic and receives a PERST Active Tunneled Packet on the Upstream Facing Port.
4.5.1#5	TD 4.21 TD 4.22	(Device Router) A Router shall enter sleep state when the Enter Sleep bit is set to 1b and one of the following sleep events occur: The Router receives an LT_LRoff Transaction on the Sideband Channel of an Upstream Facing Port.
4.5.1#6	TD 4.21 TD 4.22	A Router shall not enter sleep state unless the Enter Sleep bit is set to 1b before a sleep event occurs.
4.5.1#7	NT	After the Enter Sleep bit is set to 1b, the Router shall complete any pending transactions on the Sideband Channel.
4.5.1#8	TD 4.21 TD 4.22	When the Router is ready for the sleep event it shall set the *Sleep Ready* bit to 1b.
4.5.1#9	TD 4.21 TD 4.22	After a sleep event occurs, the Router shall do the following for each USB4 Port: If the *USB4 Port is inter-Domain* bit is 0b, the *USB4 Port is Configured* bit is 0b, and the *Enable Wake on Connect* bit of the USB4 Port is 0b, perform a disconnect by driving its SBTX line low for a minimum of tDisconnectTx.
4.5.1#10	TD 4.21 TD 4.22	After a sleep event occurs, the Router shall do the following for each USB4 Port: If the USB4 Port is inter-Domain bit is 1b and the Enable Wake on inter-Domain bit is set to 0b, perform a disconnect by driving its SBTX line low for a minimum of tDisconnectTx.
4.5.1#11	CH11	After a sleep event occurs, the Router shall do the following for each USB4 Port: Else: If a Downstream Facing Port supports PCIe tunneling, send at least 3 PERST Active Tunneled Packets.
4.5.1#12	TD 4.21 TD 4.22	After a sleep event occurs, the Router shall do the following for each USB4 Port: Else: Send an LT_LRoff Transaction on the Sideband Channel within tLRoffResponse from detecting the sleep event.
4.5.1#13	NT	After a sleep event occurs, the Router shall do the following for each USB4 Port: Else: If the *USB4 Port is Inter-Domain* bit is 0b and the *USB4 Port is Configured* bit is 1b, wait for an LT_LRoff Transaction on the Sideband Channel, unless an LT_LRoff Transaction was already received from the time the *Enter Sleep* bit was set to 1b.
4.5.1#14	TD 4.21 TD 4.22	After a sleep event occurs, the Router shall do the following for each USB4 Port: Else: Transition the Adapters to CLd state if they are not already disabled.
4.5.2 Behavior in Sleep State		
4.5.2#1	TD 4.21 TD 4.22	On entry to sleep state, a Router shall restore all Configuration Spaces to their default values.

4.5.2#2	NT	If the Enter Sleep bit is set to 1b, a Router shall retain a copy of the state information listed in Table 4-42 separate from Configuration Space.
4.5.2#3	TD 4.21 TD 4.22	If a USB4 Port has the USB4 Port is inter-Domain state set to 1b, then the USB4 Port shall ignore any Transactions received on the Sideband Channel while in Sleep state.
4.5.3 Wake Events		
4.5.3#1	TD 4.23	A Router shall issue a Wake on Connect if the Enable Wake on Connect bit of a USB4 Port is set to 1b, the USB4 Port is Configured bit is 0b, and it detects either of the following after the Enter Sleep bit is set to 1b and it detects either of the following: A connection on the USB Type-C connector attached to the USB4 Port.
4.5.3#2	TD 4.23	A Router shall issue a Wake on Connect if the Enable Wake on Connect bit of a USB4 Port is set to 1b, and it detects either of the following: SBRX is at logic high on the USB4 Port for tConnectRx.
4.5.3#3	TD 4.24	A Router shall issue a Wake on Disconnect event if the Enable Wake on Disconnect bit of a USB4 Port is set to 1b, the USB4 Port is Inter-Domain bit is set to 0b, the USB4 Port is Configured bit is set to 1b, and the Router detects either of the following after the Enter Sleep bit is set to 1b: A disconnect on the USB Type-C connector attached to the USB4 Port.
4.5.3#4	TD 4.24	A Router shall issue a Wake on Disconnect event if the *Enable Wake on Disconnect* bit of a USB4 Port is set to 1b, the *USB4 Port is Inter-Domain* bit is set to 0b, the *USB4 Port is Configured* bit is set to 1b, and the Router detects either of the following after the *Enter Sleep* bit is set to 1b: SBRX is at logic low on the USB4 Port for tDisconnectRx.
4.5.3#5	TD 4.25	A Router shall issue a Wake on Inter-Domain event if the Enable Wake on Inter-Domain bit is set to 1b, the USB4 Port is Inter-Domain bit is set to 1b, and the Router detects either of the following after the Enter Sleep bit is set to 1b: A disconnect on the USB Type-C connector attached to the USB4 Port.
4.5.3#6	TD 4.25	A Router shall issue a Wake on Inter-Domain event if the Enable Wake on Inter-Domain bit is set to 1b, the USB4 Port is Inter-Domain bit is set to 1b, and the Router detects either of the following after the Enter Sleep bit is set to 1b: SBRX is at logic low on the USB4 Port for tDisconnectRx.
4.5.3#7	CH11	A Router shall issue a Wake on PCIe event if the Enable Wake on PCIe bit is set to 1b, and it detects a PCIe Wake event from any connected PCIe Endpoint or Switch after a Sleep Event occurs.
4.5.3#8	CH11	A Router shall issue a Wake on USB3 event if the Enable Wake on USB3 bit is set to 1b, and it detects a USB Wake event from any connected USB device after a Sleep Event occurs.

4.5.3#9	TD 4.26	A Router shall issue a Wake on USB4 event if the USB4 Port is inter-Domain bit is set to 0b, the USB4 Port is Configured bit is set to 1b, and the Router detects at least one transition of SBRX to logical low for tWake time after a Sleep Event occurs.
4.5.4 Exit from Sleep		
4.5.4#1	TD 4.23 TD 4.24 TD 4.25 TD 4.26	A Router shall assert SBRX to logical low for tWake time to indicate a Wake on USB4 event.
4.5.4#2	IOP	After detecting a wake event, a Router shall: 1. issue a Wake on USB4 event on all connected USB4 Ports by asserting SBTX to logical low for tWake time.
4.5.4#3	TD 4.23 TD 4.24 TD 4.25 TD 4.26	After detecting a wake event, a Router shall: 2. begin Lane Initialization on all connected USB4 Ports.
4.5.4#4	NT	The transmitting USB4 Port shall retry the Transactions as defined in Section 4.1.1.2.5.
4.5.4#5	TD 4.23 TD 4.24 TD 4.25 TD 4.26	After detecting a wake event, the Router shall: 3. for every Adapter that reaches CL0 state, send a Hot Plug Event Packet to the Connection Manager with the UPG bit set to 0b.
4.6 Timing Parameters		

Assertion #	Test Name	Assertion Description
8 Registers		
8.1 Configuration Fields Access Types		
8.2.2.4#21	TD 4.23	An Adapter shall set the Router Detected bit to 1b when the USB4 Port detects a connected Router.
8.2.2.4#22	TD 4.24	An Adapter shall set the Router Detected bit to 0b upon a disconnect.
8.2.2.4#23	TD 4.23	An Adapter shall set the Wake on Connect Status bit to 1b after a wake event is generated by the USB4 Port as a result of a connect to the USB4 Port.
8.2.2.4#24	TD 4.23	The Wake on Connect Status bit shall not be set to 1b unless the Enable Wake on Connect bit is 1b.
8.2.2.4#25	TD 4.23	The Wake on Connect Status bit shall be set to 0b on entry to sleep.
8.2.2.4#26	TD 4.24	An Adapter shall set the Wake on Disconnect Status bit to 1b after a wake event is generated by the USB4 Port as a result of a disconnect from the USB4 Port.
8.2.2.4#27	TD 4.24	The Wake on Disconnect Status bit shall not be set to 1b unless the Enable Wake on Disconnect bit is 1b.
8.2.2.4#28	TD 4.24	The Wake on Disconnect Status bit shall be set to 0b on entry to sleep.
8.2.2.4#29	TD 4.25	An Adapter shall set the *Wake on USB4 Wake Status* bit to 1b after a wake event is generated by the USB4 Port as a result of a USB4 Wake.
8.2.2.4#30	TD 4.25	The *Wake on USB4 Wake Status* bit shall not be set to 1b unless the *Enable Wake on USB4 Wake* bit is 1b.
8.2.2.4#31	TD 4.25	The *Wake on USB4 Wake Status* bit shall be set to 0b on entry to sleep.
8.2.2.4#32	TD 4.26	An Adapter shall set the Wake on Inter-Domain Status bit to 1b after a wake event is generated by the USB4 Port as a result of an inter-Domain Wake.
8.2.2.4#33	TD 4.26	The Wake on Inter-Domain Status bit shall not be set to 1b unless the Enable Wake on inter-Domain bit is 1b.
8.2.2.4#34	TD 4.26	The Wake on Inter-Domain Status bit shall be set to 0b on entry to sleep.

Chapter 13

The following Table presents the USB4 Specification Chapter 13 asserts.

Assertion #	Test Name	Assertion Description
13 Interoperability with Thunderbolt™ 3 (TBT3) Systems		
13.2 Logical Layer		
13.2.1 Sideband Channel		
13.2.1.1 Bidirectional Re-timer		
13.2.1.1#1	IOP	A Router shall implement a bidirectional Sideband Channel when attached directly to a bidirectional Cable Re-timer.
13.2.1.1#2	IOP	A Router shall implement a unidirectional Sideband Channel when not attached directly to a bidirectional Cable Re-timer.
13.2.1.1#3	IOP	A Router that is connected directly to a bidirectional Re-timer shall support concurrent reception of Transactions on SBTX and on SBRX.
13.2.1.1#4	NT	A Router shall drive its SBTX for up to 2 bit times after the last Stop bit of an AT Command.
13.2.1.2 Transactions		
13.2.1.2.1 LT Transactions		
13.2.1.2.1#1	IOP	A Router shall support the additional LT Transaction types defined in Table 13-2.
13.2.1.2.2 AT Transactions		
13.2.1.2.2#1	BC	The structure of the STX Symbol within an AT Transaction shall be as defined in Table 13-3.
13.2.1.2.2#2	NT	Bit 4 in the STX symbol (Responder) shall be set to 1b by a Re-timer in an AT Response when operating in an active cable with bidirectional Re-timers.
13.2.1.2.2#3	BC	Bit 4 in the STX symbol (Responder) shall be set to 0b in all other cases.
13.2.1.2.2#4	NT	Bit 2 in the STX symbol (Recipient): For an AT Command: shall be 0b if a Cable Re-timer is the intended final recipient or 1b if a Router is the intended final recipient
13.2.1.2.2#5	BC	Bit 2 in the STX symbol (Recipient): For an AT Response: shall be set to 1b

13.2.1.2.2#6	NT	A Router shall not send an AT Command that targets Register 13 of a Re-timer or Router SB Register Space unless the Re-timer or Router is directly attached to it.
13.2.1.2.2.1 Bounce Mechanism		
13.2.1.2.2.1#1	TD 4.44	A Router shall support the Bounce Mechanism.
13.2.1.2.2.1#2	TD 4.44	A Router shall set the Bounce bit to 1b and the ReturnBounce bit to 1b to target a Cable Re-timer that is adjacent to the Router's Link Partner.
13.2.1.2.2.1#3	TD 4.44	A Router that receives an AT Transaction with the Bounce bit set to 1b and the ReturnBounce bit to 1b shall set the Bounce bit to 0b, then forward the AT Transaction towards its adjacent Cable Re-timer.
13.2.1.2.2.1#4	TD 4.44	A Router that receives an AT Response with the Bounce bit set to 1b and the ReturnBounce bit to 0b shall set the Bounce bit to 0b, then forward the AT Response to its Link Partner.
13.2.1.2.3 RT Transactions		
13.2.1.2.3#1	BC	Byte 2 in a Broadcast RT Transaction shall have the format in Table 4-7 with the changes in Table 13-4.
13.2.1.3 SB Register Space		
13.2.1.3#1	0	A Router shall support the additional registers and register fields in Table 13-5 and Table 13-6.
13.2.1.4 Lane Initialization		
13.2.1.4.1 Phase 1 – Determination of Initial Conditions		
13.2.1.4.1#1	IOP	A Router shall not continue on to Phase 2 until it has obtained the connection information described in this section and in Section 4.1.2.1.
13.2.1.4.1#2	IOP	If TBT3 Mode is established on the Link, a Router shall proceed with Lane Initialization as defined in Section 4.1.2 with the changes defined in this chapter.
13.2.1.4.2 Phase 3 – Determination of USB4 Port Characteristics		
13.2.1.4.2#1	IOP	Router shall decide the Lane attributes using the decision criteria in Table 4-18 with the changes defined in Table 13-7.
13.2.1.4.2#2	IOP	Router A shall enable RS-FEC if at least one side of the Link requests it (i.e. the RS-FEC Request (Gen 2) bit is set to 1b in the SB Register Space of the local USB4 Port and/or its Link Partner).
13.2.1.4.2#3	IOP	Otherwise, RS-FEC shall not be enabled.

13.2.1.4.2#4	IOP	Router A shall set the RS-FEC Enabled (Gen 2) bit in the USB4 Port Capability to reflect whether it is operating with RS-FEC.
13.2.1.4.2#5	0	The Sideband Channel of Router A shall operate as a USB4 Sideband Channel if all of the following are true: The USB4 Sideband Channel Support bit in the SB Register Space of both Routers is 1b; The Link is over either a Passive Cable or an Active Cable with unidirectional Re-timers.
13.2.1.4.2#6	0	Else, the Sideband Channel of Router A shall operate as a TBT3-Compatible Sideband Channel.
13.2.1.4.2#7	0	When sending a Broadcast RT Transaction on a USB4 Sideband Channel, Router A shall set the USB4 bit to 1b.
13.2.1.4.2#8	0	When sending a Broadcast RT Transaction on a TBT3-Compatible Sideband Channel, Router A shall set the USB4 bit to 0b.
13.2.1.4.3 Phase 4 – Lane Parameters Synchronization and Transmit Start		
13.2.1.4.3#1	0	Router A shall do the following for each enabled Lane to indicate that it is ready to start transmission on a given Lane:
13.2.1.4.3#2	0	If the Router Assembly for Router A does not include any On-Board Re-timers, and if operating at Gen 2 speed, Router A shall send an LT_Gen_2 Transaction for each enabled Lane every tLaneParams.
13.2.1.4.3#3	0	Router A shall continue sending LT_Gen_2 Transactions until all of the following are true, then continue to Step 2: At least tLTPhase4 time has passed from completion of Phase 2; Router A has sent LT_Gen_2 Transactions at least twice; Router A has received an LT_Gen_2 Transaction from Router B.
13.2.1.4.3#4	0	If the Router Assembly for Router A does not include any On-Board Re-timers, and if operating at Gen 3 speed, Router A shall send an LT_Gen_3 Transaction for each enabled Lane every tLaneParams.
13.2.1.4.3#5	0	Router A shall continue sending LT_Gen_3 Transactions until all of the following are true, then continue to Step 2: At least tLTPhase4 time has passed from completion of Phase 2; Router A has sent LT_Gen_3 Transactions at least twice; Router A has received an LT_Gen_3 Transaction from Router B.
13.2.1.4.3#6	0	If the Router Assembly for Router A includes one or more On-Board Re-timers, and if operating at Gen 2 speed, Router A shall send a Broadcast RT Transaction every tLaneParams.
13.2.1.4.3#7	0	The Broadcast RT Transaction shall have the parameter values in Table 4-18.
13.2.1.4.3#8	0	Router A shall also send an LT_Gen_2 Transaction for each enabled Lane.
13.2.1.4.3#9	0	Router A shall continue sending the Broadcast RT and LT_Gen_2 Transactions until all of the following conditions are true: At least tLTPhase4 time has passed from completion of Phase 2; Router A has sent LT_Gen_2 Transactions at least twice; Router A has received an LT_Gen_2 Transaction from Router B.

13.2.1.4.3#10	0	If the Router Assembly for Router A includes one or more On-Board Re-timers, and if operating at Gen 3 speed, Router A shall send a Broadcast RT Transaction every tLaneParams.
13.2.1.4.3#11	0	The Broadcast RT Transaction shall have the parameter values in Table 4-18.
13.2.1.4.3#12	0	Router A shall also send an LT_Gen_3 Transaction for each enabled Lane.
13.2.1.4.3#13	0	Router A shall continue sending the Transactions until all of the following conditions are true: At least tLTPhase4 time has passed from completion of Phase 2; Router A has sent LT_Gen_3 Transactions at least twice; Router A has received an LT_Gen_3 Transaction from Router B.
13.2.1.4.4 Phase 5 – Link Equalization		
13.2.1.4.4#1	0	(Transmitter) If Router A connects to an On-Board Re-timer in the same Router Assembly, then Router A's transmitter shall perform the transmitter flow in the symmetric equalization flow defined in Section 4.1.2.5.1.
13.2.1.4.4#2	0	(Transmitter) If Router A connects to a Cable Re-timer: Router A's transmitter shall perform the Primary Partner flow in the Asymmetric TxFFE Parameter Negotiation with a transmitting Primary Partner defined in Section 13.2.1.4.4.1.
13.2.1.4.4#3	0	(Transmitter) If Router A connects to a Cable Re-timer: Once a transmitter completes TxFFE negotiation with the Cable Re-timer's receiver, Router A shall send an LT_Resume2 Transaction on the USB4 Port that completed negotiation with the LSELane field matching the Lane number that completed negotiation.
13.2.1.4.4#4	0	(Transmitter) If Router A either connects directly to Router B or connects to an On-Board Re-timer in the Router Assembly of Router B (through a Passive Cable or Cable with re-driver), then Router A's transmitter shall perform the transmitter flow in the symmetric equalization flow defined in Section 4.1.2.5.1.
13.2.1.4.4#5	0	(Receiver) If Router B connects to an On-Board Re-timer, then Router B's receiver shall perform the receiver flow in the symmetric equalization flow defined in Section 4.1.2.5.1.
13.2.1.4.4#6	0	(Receiver) When a receiver's equalization flow is complete on a Lane, the Router shall set the Lane's Clock Switch Done bit to 1b
13.2.1.4.4#7	0	(Receiver) If Router B connects to a Cable Re-timer, then Router B's receiver shall perform the Primary Partner flow in the Asymmetric TxFFE Parameter Negotiation with a Receiving Primary Partner defined in Section 13.2.1.4.4.2.
13.2.1.4.4#8	0	(Receiver) If Router B either connects directly to Router A or connects to an On-Board Re-timer in the Router Assembly of Router A, then Router B's receiver shall perform the receiver flow in the symmetric equalization flow defined in Section 4.1.2.5.1.

13.2.1.4.4.1 Phase 5 – Asymmetric TxFFE Parameter Negotiation with a Transmitting Primary Partner		
Transmitting Primary Partner flow:		
13.2.1.4.4.1#1	0	1) The transmitter shall start with the TX Active bit set to 1b (default value) in the Tx Status byte of the TxFFE register
13.2.1.4.4.1#2	0	2) The transmitter shall send an AT Transaction with a write Command to the receiver that sets the Tx Active bit to 1b in the Partner Tx Status byte in the TxFFE register
13.2.1.4.4.1#3	0	3) The transmitter shall read the local Rx Status & TxFFE Request byte from the receiver.
13.2.1.4.4.1#4	0	4) On reception of an AT Response from the receiver, the transmitter shall copy the transaction contents into its Rx Status & TxFFE Request byte.
13.2.1.4.4.1#5	0	4) If Rx Locked = 1b, then negotiation is complete and no further TxFFE negotiation steps shall be taken.
13.2.1.4.4.1#6	0	4) Else if New Request = 0b and TxFFE Request is the same as the previous TxFFE Request, the receiver has not provided a new request yet. The Router shall go to Step 3. The Router shall perform Step 3 within tPollTXFFE of receiving the AT Response.
13.2.1.4.4.1#7	0	4) Else, this is a new request to update TxFFE parameters. Continue on to Step 5.
13.2.1.4.4.1#8	0	5) The transmitter shall update its transmitter parameters based on the new parameters received in the AT Response
13.2.1.4.4.1#9	0	5) If both Lane Adapters in the Port are enabled and have not yet completed TxFFE negotiation, both transmitters must complete Step 5 before continuing to Step 6. If the other Lane Adapter has not yet completed Step 5, the transmitter shall wait for the other Lane to finish Step 5 before continuing to Step 6.
13.2.1.4.4.1#10	0	6) The transmitter shall inform the receiver that it has updated to new parameters by sending an AT Transaction with a write Command to the receiver targeting its Partner Tx Status byte in the TxFFE register with the following contents: Tx Active = 1b; TxFFE Setting = value received in Step 4.
13.2.1.4.4.1#11	0	7) The transmitter shall read the local Rx Status & TxFFE Request byte from the receiver.
13.2.1.4.4.1#12	0	8) On reception of an AT Response from the receiver, the transmitter shall copy the transaction contents into its Rx Status & TxFFE Request byte
13.2.1.4.4.1#13	0	8) If New Request = 1b and TxFFE Request is the same as the previous TxFFE Request, the Router shall return to and perform Step 7 within tPollTXFFE of receiving the AT Response.

13.2.1.4.4.1#14	0	8) Else, go to Step 3.
13.2.1.4.4.2 Phase 5 – Asymmetric TxFFE Parameter Negotiation with a Receiving Primary Partner		
Receiving Primary Partner flow:		
13.2.1.4.4.2#1	0	1) The receiver shall start with the following default values in the Rx Status & TxFFE Request byte of the TxFFE register: Rx Locked = 0b; New Request bit = 0b; Rx Active bit = 0b.
13.2.1.4.4.2#2	0	2) The receiver shall read the Local Tx Status byte of the transmitter.
13.2.1.4.4.2#3	0	2) On reception of an AT Response from the transmitter, the receiver shall do the following: If Tx Active = 1b (i.e. the transmitter is transmitting), then enable the receiver, set Rx Active to 1b, and go to Step 3. Else, repeat Step 2 within tPollTXFFE of receiving the AT Response.
13.2.1.4.4.2#4	0	3) The receiver shall evaluate its receiver behavior. If equalization is complete, the receiver shall set the Rx Locked field to 1b.
13.2.1.4.4.2#5	0	4) The receiver shall do the following: If Rx Locked = 1, then go to Step 5. Else, go to Step 6
13.2.1.4.4.2#6	0	5) TXFFE negotiation is complete.
13.2.1.4.4.2#7	0	6) The receiver shall select a new set of TxFFE parameters.
13.2.1.4.4.2#8	0	7) The receiver shall write the Partner Rx Status & TxFFE Request byte at the transmitter as follows: If the Transmitting Primary Partner finished TxFFE on both Lanes, then the receiver sends an AT Command with a write Command targeting the Partner Rx Status & TxFFE Request byte of the TxFFE register of the transmitter. Else, the receiver will wait for the next AT Command with a write Command to the TxFFE Register from the Transmitting Primary Partner and use it to write the Partner Rx Status & TxFFE Request byte of the TxFFE register of the transmitter. The AT command shall write to following values to the following fields: New Request = 1b; Rx Active = 1b; TxFFE Request = index of selected set of TxFFE parameters.
13.2.1.4.4.2#9	0	8) The receiver shall wait for a write Response indicating the transmitter is using the new requested TxFFE settings.
13.2.1.4.4.2#10	0	9) The receiver shall evaluate its receiver behavior. If equalization is complete, the receiver shall set the Rx Locked field to 1b.
13.2.1.4.4.2#11	0	10) The receiver shall write the Partner Rx Status & TxFFE Request byte at the transmitter as follows: If the Transmitting Primary Partner finished TxFFE on both Lanes, then the receiver sends an AT Command with a write Command targeting the Partner Rx Status & TxFFE Request byte of the TxFFE register of the transmitter.

13.2.1.4.4.2#12	0	10) The receiver shall write the Partner Rx Status & TxFFE Request byte at the transmitter as follows: Else, the receiver will wait for the next AT Command with a write Command to the TxFFE Register from the Transmitting Primary Partner and use it to write the Partner Rx Status & TxFFE Request byte of the TxFFE register of the transmitter. The AT Command shall write to following values to the following fields: New Request = 0b; Rx Active = 1b; Rx Locked = updated value
13.2.1.4.4.2#13	0	11) The receiver shall do the following: If Rx Locked = 1, then go to Step 5. Else, go to Step 6.
13.2.2 Logical Layer State Machine		
13.2.2.1 CLd State		
13.2.2.1.1 Behavior in State		
13.2.2.1.1#1	TD 4.47	A USB4 Port that is TBT3-Compatible shall support the behavior defined in this section in addition to the behavior described in Section 4.2.1.2.2.
13.2.2.1.1#2	TD 4.47	A Lane Adapter (that is not the Upstream Adapter) that enters this state due to reception of an LT_Fall Transaction shall start Lane Initialization when it receives a Broadcast RT Transaction, an LT_Gen_2 Transaction, or an LT_Gen_3 Transaction.
13.2.2.1.1#3	TD 4.47	A Lane 0 Adapter shall not start Lane Initialization until it receives one of the following: A Broadcast RT Transaction with the Lane0Enabled bit set to 1b; An LT_Gen_2 Transaction with the LSELane bit set to 0b; An LT_Gen_3 Transaction with the LSELane bit set to 0b.
13.2.2.1.1#4	TD 4.47	A Lane 1 Adapter shall not start Lane Initialization until it receives one of the following: A Broadcast RT Transaction with the Lane1Enabled bit set to 1b; An LT_Gen_2 Transaction with the LSELane bit set to 1b; An LT_Gen_3 Transaction with the LSELane bit set to 1b.
13.2.2.1.1#5	TD 4.47	The Lane Adapter shall start Lane Initialization from Phase 4.
13.2.2.1.1#6	TD 4.47	The Lane Adapter shall maintain any state acquired in Phases 1 through 3 of previous Lane Initialization.
13.2.2.2 TS1 and TS2 Ordered Sets		
13.2.2.2#1	IOP	When operating in TBT3 mode, TS1 and TS2 Ordered Sets shall have the format shown in Table 4-25 with the changes in Table 13-8.
13.2.2.2#2	IOP	Lane Bonding Target 2. Transmitter shall either set this value to match the Lane Bonding Target field or shall set this value to 001b.
13.2.2.2#3	NT	Lane Bonding Target 2. A Receiver shall ignore this field.

13.2.3 USB4 Link Operation		
13.2.3.1 USB4 Link Transitions		
13.2.3.1#1	TD 4.48	When TBT3 Mode is established on the Link, a USB4 Port shall support the transitions described in Section 4.2.2 with the following changes:
13.2.3.1#2	TD 4.48	For a Device Router, the USB4 Port shall support operation with two independent Single-Lane Links.
13.2.3.1#3	TD 4.48	For a Device Router, the USB4 Port shall support operation with a Single-Lane Link using the Lane 1 Adapter of the USB4 Port.
13.2.3.1#4	NT	For a Device Router, the USB4 Port shall support configuration where the Lane 1 Adapter is the Upstream Adapter when the Lane 1 Adapter is the only Adapter in CL0 state.
13.2.3.2 Pre-Coding		
13.2.3.2#1	NT	Pre-coding shall be off when the Link Partner has the USB4 Sideband Channel Support bit in SB Register Space set to 0b.
13.2.4 Sleep and Wake		
13.2.4#1	TD 4.49	If bits 15:12 in the Connection Manager USB4 Version field in the Router Configuration Space are 0b (indicating a TBT3 Connection Manager), a Router shall support Sleep and Wake per Section 4.5 with the changes defined in this section.
13.2.4.1 Entry to Sleep		
13.2.4.1#1	TD 4.49	After the Enter Sleep bit is set to 1b in all Ports, a Device Router shall do the following for each USB4 Port: Transition the USB4 Adapters to CLd state.
13.2.4.1#2	TD 4.49	After the Enter Sleep bit is set to 1b in all Ports, a Device Router shall do the following for each USB4 Port: If any of the following conditions apply, the USB4 Port shall go through disconnect: For Lane 0 in a USB4 Port: The Lane 0 is Inter-Domain bit is 0b and the Lane 0 Configured bit is 0b; The Lane 0 is Inter-Domain bit is 1b and the Inter-Domain Disconnect on Sleep bit is set to 1b.
13.2.4.1#3	TD 4.49	After the Enter Sleep bit is set to 1b in all Ports, a Device Router shall do the following for each USB4 Port: If any of the following conditions apply, the USB4 Port shall go through disconnect: For Lane 1 in a USB4 Port: The Lane 1 is Inter-Domain bit is 0b and the Lane 1 Configured bit is 0b; The Lane 1 is Inter-Domain bit is 1b and the Inter-Domain Disconnect on Sleep bit is set to 1b.

13.2.4.2 Behavior in Sleep State		
13.2.4.2#1	NT	A Device Router shall retain a copy of the state information listed in Table 13-9 separate from Configuration Space.
13.2.4.2#2	NT	If Lane 0 of a USB4 Port is disconnected while in Sleep state, then the internal Lane 0 is Inter-Domain state and Lane 0 Configured state listed in Table 13-9 shall both transition to 0b.
13.2.4.2#3	NT	If Lane 1 of a USB4 Port is disconnected while in Sleep state, then the internal Lane 1 is Inter-Domain state and Lane1 Configured state listed in Table 13-9 shall both transition to 0b.
13.2.4.3 Wake Events		
13.2.4.3#1	TD 4.50	A Device Router shall support all of the wake events listed in the Enable Wake Events field of the USB4 Port Region in the Vendor Specific Extended 6 Capability of the Router Configuration Space.
13.2.4.4 Exit From Sleep		
13.2.4.4#1	TD 4.51	A Device Router shall not start Lane Initialization for Lane 0 until the Start Link Initialization bit is set to 1b, if either of the following is true on exit from sleep: The Lane 0 Configured state is set to 0b; The Lane 0 is Inter-Domain bit is 1b.
13.2.4.4#2	TD 4.51	A Device Router shall not start Lane Initialization for Lane 1 until the Start Link Initialization bit is set to 1b, if either of the following is true on exit from sleep: The Lane 1 Configured state is set to 0b; The Lane 1 is Inter-Domain bit is 1b.
13.2.5 Timing Parameters		

Re-timer Assertions

Chapter 4

The following Table presents the USB4 Re-timer Specification Chapter 4 asserts.

Assertion #	Test Name	Assertion Description
4. Logical Layer		
4#1rt	NT	A Re-timer shall have two USB4 Ports.
4#2rt	NT	The USB4 Ports on a Re-timer shall have the same number of Lane Adapters and shall support the same capabilities.
4.1 Sideband Channel		
4.1.1 Transactions		
4.1.1#1rt	IOP	When forwarding Transactions from an SBRX input to an SBTX output, a Re-timer shall maintain the order of Transactions as received on the SBRX input.
4.1.1.1 LT Transactions		
4.1.1.1#1rt	IOP	A Re-timer shall support LT Transactions as defined in the USB4 Base Specification with the following changes:
4.1.1.1#2rt	IOP	When a Re-timer receives an LT Transaction, it shall forward the Transaction to its other USB4 Port.
4.1.1.2 AT Transactions		
4.1.1.2#1rt	NT	A Re-timer shall support AT Transactions as defined in the USB4 Base Specification with the following changes:
4.1.1.2#2rt	NT	A Cable Re-timer shall forward an AT Transaction, regardless of the value of the Recipient bit.
4.1.1.2#3rt	NT	An On-Board Re-timer shall forward an AT Transaction, regardless of the value of the Recipient bit.
4.1.1.2#4rt	NT	A Re-timer shall not initiate AT Commands.
4.1.1.3 RT Transactions		
4.1.1.3#1rt	NT	A Re-timer shall support RT Transactions as defined in the USB4 Base Specification with the changes defined in this section.

4.1.1.3.1 Broadcast RT Transaction		
4.1.1.3.1#1rt	TD 4.5	When a Re-timer receives a Broadcast RT Transaction on its Router-Facing USB4 Port, it shall increment the value in the Index field of the Transaction by one and shall store the resulting Re-timer Index locally as its Router-Facing Index.
4.1.1.3.1#2rt	TD 4.5	The Re-timer shall then forward the Broadcast RT Transaction.
4.1.1.3.1#3rt	NT	When a Re-timer receives a Broadcast RT Transaction on its Cable-Facing USB4 Port, it shall increment the value in the Index field of the Transaction by one and shall store the resulting Re-timer Index locally as its Cable-Facing Index.
4.1.1.3.1#4rt	NT	The Re-timer shall then forward the Broadcast RT Transaction.
4.1.1.3.1#5rt	TD 4.5	When a Re-timer forwards a Broadcast Transaction, it shall set the SSCalways bit to 0b to indicate that the Re-timer supports exiting CLx state with SSC turned off.
4.1.1.3.2 Addressed RT Transaction		
4.1.1.3.2#1rt	NT	When sending an Addressed RT Command, a Re-timer shall set the Index field to 0.
4.1.1.3.2#2rt	IOP	When a Re-timer receives an Addressed RT Command with the Index field set to 0, it shall process the Command and send a response as described in the USB4 Base Specification. The Re-timer shall not forward the Transaction.
4.1.1.3.2#3rt	NT	When a Re-timer receives an Addressed RT Command on its Router-Facing USB4 Port with an Index field that matches its Router-Facing Index, it shall process the Command and send a response as described in the USB4 Base Specification. The Re-timer shall not forward the Transaction.
4.1.1.3.2#4rt	NT	When an On-Board Re-timer receives an Addressed RT Command on its Cable-Facing USB4 Port with an Index field that matches its Cable-Facing Index, it may process the Command and send a response as described in Section 4.1.2.5.1 of the USB4 Specification, but is not required to do so. It shall not forward the Command.
4.1.1.3.2#5rt	NT	When a Cable Re-timer receives an Addressed RT Command on its Cable-Facing USB4 Port with an Index field that matches its Cable-Facing Index, it shall process the Command and send a response as described in the USB4 Base Specification. The Re-timer shall not forward the Transaction.
4.1.1.3.2#6rt	NT	When a Re-timer receives an Addressed RT Transaction on its Router-Facing USB4 Port with an Index field that does not match its Router-Facing Index, it shall forward the RT Transaction without sending a response.
4.1.1.3.2#7rt	TD 4.1	When a Re-timer receives an Addressed RT Transaction on its Cable-Facing USB4 Port with an Index field that does not match its Cable-Facing Index, it shall forward the RT Transaction without sending a response.

4.1.1.3.2#8rt	IOP	If the Index field in the Addressed RT Transaction is 0, then the Re-timer shall consume the Addressed RT Response.
4.1.1.3.2#9rt	IOP	If the Index field in the Addressed RT Transaction is not 0, the Re-timer shall forward the Addressed RT Response.
4.1.1.4 SB Register Space		
4.1.1.4#1rt	IOP	A Re-timer shall maintain the SB Register Space defined in Table 4-1.
4.1.1.4#2rt	NT	Read Only. An AT Write Command or an RT Write Command to a field with this access type shall have no effect. An AT Read Command or an RT Read Command shall return a meaningful value
4.1.1.4#3rt	NT	Read/Write. A field with this access type shall be capable of both Read Commands and Write Commands. The value read from this field shall reflect the last value written to it unless the field was reset in the interim.
4.1.1.4#4rt	NT	Reserved. Reserved for future implementation. A Write Command to this field shall have no effect.
4.1.1.4#5rt	NT	Reserved with Non-Zero Value. Reserved for future implementation. A Write Command to this field shall have no effect. A read shall return the specified value.
4.1.1.4#6rt	IOP	The SB Register Space registers shall have the structure and fields described in Table 4-3.
4.1.2 Lane Initialization		
4.1.2#1rt	NT	A Re-timer shall perform Lane Initialization as described in the USB4 Base specification with the modifications described in this section.
4.1.2.1 Phase 1 - Determination of Initial Conditions		
4.1.2.1#1rt	IOP	An On-Board Re-timer shall also determine whether or not there is a reverse insertion at the USB Type-C connector.
4.1.2.1#2rt	NT	A Re-timer shall not continue on to Phase 2 until it has obtained the connection information listed above.
4.1.2.1#3rt	NT	A Re-timer shall not proceed to phase 2 unless USB4 Mode is established on the Link.
4.1.2.1.1 Lane Reversal		
4.1.2.1.1#1rt	IOP	When necessary to correct for Lane mismatch, Lane reversal shall take place in phase 1.
4.1.2.1.1#2rt	IOP	An On-Board Re-timer that is adjacent to the USB Type-C connector shall swap its SBTX and SBRX lines facing the connector.

4.1.2.1.1#3rt	IOP	An On-Board Re-timer shall swap its designation of Lane 0 and Lane 1 in both USB4 Ports.
4.1.2.2 Phase 2 - Router Detection		
4.1.2.2#1rt	TD 4.23 TD 4.24 TD 4.26	When a Re-timer detects a logic high on SBRX of one USB4 Port for tConnectRx time, it shall drive SBTX on the other USB4 Port to logic high.
4.1.2.2#2rt	IOP	The Re-timer shall then begin forwarding Transactions on the Sideband Channel in this direction.
4.1.2.2#3rt	IOP	After both USB4 Ports detect a logic high on SBRX and drive SBTX high, the Re-timer shall transition to phase 4 of Lane Initialization.
4.1.2.3 Phase 3 - Determination of USB4 Port Characteristics		
4.1.2.4 Phase 4 - Lane Parameters Synchronization		
4.1.2.4#1rt	IOP	When a Re-timer receives a Broadcast RT Transaction it shall update its Link parameters to match the Link parameters in the Transaction.
4.1.2.4#2rt	IOP	When a Re-timer detects an LT_Resume Transaction on any USB4 Port, it shall transition to phase 5.
4.1.2.5 Phase 5 - Lane Equalization		
4.1.2.5#1rt	NT	Upon entry to phase 5, a receiver shall perform the receiver flow for symmetric TxFFE negotiation as defined in the USB4 Base Specification.
4.1.2.5#2rt	TD 4.5	The Re-timer shall use RT Transactions (with the Index field set to 0b) to access the SB Register Space of the adjacent USB4 Port.
4.1.2.5#3rt	TD 4.5	When the Rx Active bit for a receiver is set to 1b, the Re-timer shall turn on the Corresponding Transmitter and shall start transmitting CL_WAKE1.X Ordered Set Symbols, where X is the Re-timer Index assigned by the Router that is the target of the CL_WAKE1.X Ordered Set Symbols.
4.1.2.5#4rt	NT	The transmitter shall use a locally generated, non-SSC clock to transmit the CL_WAKE1.X Ordered Set Symbols.
4.1.2.5#5rt	NT	The Corresponding Transmitter shall then perform the transmitter flow for symmetric TxFFE negotiation as defined in the USB4 Base Specification.
4.1.2.5#6rt	NT	The Re-timer shall use Addressed RT Transactions (with the Index field set to 0b) to access the SB Register Space of the adjacent USB4 Port.

4.1.2.5#7rt	TD 4.5	A transmitter shall stop using the local clock and shall start using the recovered clock from the Corresponding Receiver when all of the following are true: The Re-timer has completed TxFFE negotiation for all transmitters in that USB4 Port and all their Corresponding Receivers; and The Clock Switch Done bit for Lane 0 of the adjacent USB4 Port is 1b.
4.1.2.5#8rt	TD 4.5	After a transmitter switches to using the receiver clock, it shall forward the bit stream it receives from the Corresponding Receiver instead of transmitting its locally-generated CL_WAKE1.X Ordered Set Symbols.
4.1.2.5#9rt	TD 4.5	The Re-timer shall set the Clock Switch Done bit in the Corresponding Receiver to 1b.
4.1.2.5#10rt	NT	During the transition from local clock to receiver clock, the Re-timer shall meet the SSC_SLEW_RATE requirement as specified in the USB4 Base Specification. The transition may or may not take place on Symbol boundary.
4.2 Re-timer Channel State Machine		
4.2#1rt	NT	A Re-timer Channel shall support the following states: CLd state, Bit Lock state, Forwarding state, CL0s, CL1, CL2 states.
4.2.1 CLd		
4.2.1.1 Entry to State		
4.2.1.1#1rt	NT	A Re-timer Channel shall transition to the CLd state when any of the following occur: The Re-timer is first powered on.
4.2.1.1#2rt	NT	A Re-timer Channel shall transition to the CLd state when any of the following occur: The Re-timer detects a disconnect event (i.e. SBRX transitions to logical low on any USB4 Port for more than tDisconnectRx time).
4.2.1.1#3rt	NT	A Re-timer Channel shall transition to the CLd state when any of the following occur: The SBRX of both Re-timer USB4 Ports are at logical high and both USB4 Ports receive an LT_LRoff Transaction within tLROff of each other.
4.2.1.1#4rt	NT	A Re-timer Channel shall transition to the CLd state when any of the following occur: The Re-timer Channels for Lane 0 shall also transition to CLd state when the Re-timer receives an LT_Fall Transaction on any USB4 Port with LSELane field set to 0b.
4.2.1.1#5rt	NT	A Re-timer Channel shall transition to the CLd state when any of the following occur: The Re-timer Channels for Lane 1 shall also transition to CLd state when the Re-timer receives an LT_Fall Transaction on any USB4 Port with LSELane field set to 1b.
4.2.1.1#6rt	NT	A Re-timer Channel that transitions to CLd state due to an LT_Fall Transaction shall maintain any Lane state acquired in phase 1 and phase 2 of the previous Lane Initialization.

4.2.1.2 Behavior in State		
4.2.1.2#1rt	NT	The Re-timer Channels for Lane 0 shall start Lane Initialization when the Re-timer receives a Broadcast RT Transaction on any USB4 Port with the Lane0 Enabled bit set to 1b.
4.2.1.2#2rt	NT	The Re-timer Channels for Lane 1 shall start Lane Initialization when the Re-timer receives a Broadcast RT Transaction on any USB4 Port with the Lane1 Enabled bit set to 1b.
4.2.1.3 Exit from State		
4.2.1.3#1rt	NT	A Re-timer Channel shall exit this state when its transmitter is transmitting and its receiver is enabled.
4.2.1.3#2rt	NT	After exiting the CLd state, a Re-timer Channel shall transition to the Bit Lock state.
4.2.2 Bit Lock		
4.2.2.1 Entry to State		
4.2.2.1#1rt	NT	A Re-timer Channel shall enter this state when it exits the CLd state.
4.2.2.2 Behavior in State		
4.2.2.3 Exit from State		
4.2.2.3#1rt	NT	A Re-timer Channel shall exit this state after its receiver achieves bit lock and its transmitter is transmitting the bit stream received by its receiver.
4.2.2.3#2rt	NT	After exiting the Bit Lock state, a Re-timer Channel shall transition to the Forwarding state.
4.2.3 Forwarding		
4.2.3.1 Entry to State		
4.2.3.1#1rt	NT	A Re-timer Channel shall enter this state upon successful completion of receiver lock.
4.2.3.2 Behavior in State		
4.2.3.2#1rt	NT	When a Re-timer Channel is in Forwarding state, it shall forward traffic from its receiver to its transmitter.
4.2.3.2#2rt	NT	A Re-timer shall forward traffic regardless of whether or not it receives Logical Layer Symbols.
4.2.3.2#3rt	NT	A Re-timer Channel shall not modify the logical level of a bit. A Re-timer Channel shall neither add nor discard any bits.

4.2.3.3 Exit from State		
4.2.3.3#1rt	NT	A Re-timer Channel shall only exit this state after one of the following occurs: Transition to CLd state.
4.2.3.3#2rt	NT	A Re-timer Channel shall only exit this state after one of the following occurs: Transition to CL0s, CL1, or CL2 states.
4.2.4 Low Power (CL0s, CL1, and CL2)		
4.2.4.1 Entry to State		
4.2.4.1#1rt	NT	On detection of 3 back-to-back CL2_ACK Ordered Sets, the Re-timer Lane Adapter shall start counting time in Symbol Time units.
4.2.4.1#2rt	NT	The initial value of CL2_ACK Counter shall be the number of CL2_ACK Ordered Set Symbols that were already forwarded.
4.2.4.1#3rt	NT	On detection of 3 back-to-back CL1_ACK Ordered Sets, the Re-timer Lane Adapter shall start counting time in Symbol Time units.
4.2.4.1#4rt	NT	The initial value of CL1_ACK Counter shall be the number of CL1_ACK Ordered Set Symbols that were already forwarded.
4.2.4.1#5rt	NT	While the receiver is shut down and the Channel still in Forwarding state, the transmitter shall transmit a DC balanced signal and may use a local clock without SSC.
4.2.4.1#6rt	NT	When the CL2_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Transition the Re-timer Channel in the direction forwarding the CL2_ACK Ordered Sets to a CL2 state.
4.2.4.1#7rt	NT	When the CL2_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Reset the CL2_ACK Counter.
4.2.4.1#8rt	NT	When the CL2_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Transition the Re-timer Channel transmitter to electrical idle within tTxOff time from expiration of the CL2_ACK Counter.
4.2.4.1#9rt	NT	When the CL2_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Wait tEnterLFPS1, then enable detection of Low Frequency Periodic Signaling (LFPS).
4.2.4.1#10rt	NT	While the receiver is shut down and the Channel still in Forwarding state, the transmitter shall transmit a DC balanced signal and may use local clock without SSC.
4.2.4.1#11rt	NT	When the CL1_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Transition the Re-timer Channel in the direction forwarding the CL1_ACK Ordered Sets to a CL1 state.

4.2.4.1#12rt	NT	When the CL1_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Reset the CL1_ACK Counter.
4.2.4.1#13rt	NT	When the CL1_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Transition the Re-timer Channel transmitter to electrical idle within tTxOff time from expiration of the CL1_ACK Counter.
4.2.4.1#14rt	NT	When the CL1_ACK Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Wait tEnterLFPS1, then enable detection of Low Frequency Periodic Signaling (LFPS).
4.2.4.1#15rt	NT	On detection of 3 back-to-back CL_OFF Ordered Sets, the Re-timer Lane Adapter shall start counting time in Symbol Time units.
4.2.4.1#16rt	NT	The initial value of CL_OFF Counter shall be the number of CL_OFF Ordered Set Symbols that were already forwarded.
4.2.4.1#17rt	NT	While the receiver is shut down and the Channel still in Forwarding state, the transmitter shall transmit a DC balanced signal and may use local clock without SSC.
4.2.4.1#18rt	NT	When the CL_OFF Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Transition the Re-timer Channel in the direction forwarding the CL_OFF Ordered Sets to a low power state as follows: If CL2_ACK Ordered Sets were detected during the entry flow, transition to CL2 state; If CL1_ACK Ordered Sets were detected during the entry flow, transition to CL1 state; If CL0s_ACK Ordered Sets were detected during the entry flow, transition to CL0s state.
4.2.4.1#19rt	NT	When the CL_OFF Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Reset the CL_OFF Counter.
4.2.4.1#20rt	NT	When the CL_OFF Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Transition the Re-timer Channel transmitter to electrical idle within tTxOff time from expiration of the CL_OFF Counter.
4.2.4.1#21rt	NT	When the CL_OFF Counter reaches a count of tEnterCLx, the Re-timer Lane Adapter shall: Wait tEnterLFPS1, then enable detection of Low Frequency Periodic Signaling (LFPS).
4.2.4.1#22rt	NT	A Re-timer Lane Adapter shall respond to Logical Layer Errors as defined in Section 4.3.1.
4.2.4.1#23rt	NT	If a Re-timer Lane Adapter detects 15 back-to-back SLOS Symbols, it shall abort the entry flow.
4.2.4.1#24rt	NT	The Re-timer Lane Adapter shall also reset the CL2_ACK Counter and the CL1_ACK Counter to zero.
4.2.4.2 Behavior in State		
4.2.4.2#1rt	TD 4.11	While a Re-timer Channel is in CL2 state, its transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.

4.2.4.2#2rt	TD 4.13	While a Re-timer Channel is in CL1 state, its transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.4.2#3rt	TD 4.15	While a Re-timer Channel is in CL0s state, its transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.
4.2.4.3 Exit from State		
4.2.4.3.1 CL0s Exit		
4.2.4.3.1#1rt	NT	When a Re-timer detects an LFPS burst on one of its receivers, the Re-timer shall: Send a Low Frequency Periodic Signaling (LFPS) burst from the Corresponding Transmitter. The duration of the LFPS burst shall be at least 16 LFPS cycles and no more than tLFPSDuration.
4.2.4.3.1#2rt	NT	When a Re-timer detects an LFPS burst on one of its receivers, the Re-timer shall: Return the Corresponding Transmitter to Electrical Idle for tPreData.
4.2.4.3.1#3rt	TD 4.15	When a Re-timer detects an LFPS burst on one of its receivers, the Re-timer shall: Enable the receiver to start calibration. The Re-timer shall not enable the receiver until at least tIdleRx after the last LFPS cycle was received.
4.2.4.3.1#4rt	NT	When a Re-timer detects an LFPS burst on one of its receivers, the Re-timer shall: Start sending CL_WAKE1.X Ordered Set Symbols from the Corresponding Transmitter, where X is the Re-timer Index assigned by the Router that is the target of the CL_WAKE1.X Ordered Set Symbols. The Re-timer shall transmit the Symbols using a locally generated, non-SSC, clock.
4.2.4.3.1#5rt	NT	After a Re-timer receives 3 back-to-back CL_WAKE2.X Ordered Set Symbols (where X is the same value as in step 4) on at least one Lane Adapter, the Re-timer shall transition each Re-timer Channel that is in CL0s state to transmit on the clock recovered from the received Symbols rather than on its local clock.
4.2.4.3.1#6rt	NT	The transition shall happen only after bit lock is achieved by all Re-timer Channels that are in CL0s state.
4.2.4.3.1#7rt	TD 4.15	Each Re-timer Channel in CL0s state shall transition to Forwarding state. From this point on, a Re-timer Channel shall forward the bit stream it receives from the Lane and stop generating CL_WAKE1.X Ordered Set Symbols.
4.2.4.3.1#8rt	NT	During the transition from local clock to receiver clock, the Re-timer shall meet the SSC_SLEW_RATE requirement as specified in the USB4 Base Specification.

4.2.4.3.2 CL1/CL2 Exit		
4.2.4.3.2.1 Phase 1		
4.2.4.3.2.1#1rt	TD 4.11 TD 4.13	When a Re-timer detects an LFPS burst of 2 cycles on one of its Lane Adapters, it shall do the following: 1. Send LFPS as follows: The Lane Adapter that detected the LFPS shall send LFPS for at least 5 LFPS cycles and no more than tLFPSDuration.
4.2.4.3.2.1#2rt	NT	When a Re-timer detects an LFPS burst of 2 cycles on one of its Lane Adapters, it shall do the following: 1. Send LFPS as follows: The Corresponding Adapter shall send LFPS until it detects LFPS.
4.2.4.3.2.1#3rt	NT	When a Re-timer detects an LFPS burst of 2 cycles on one of its Lane Adapters, it shall do the following: 2. Enable the receivers for the Lane Adapter and its Corresponding Adapter.
4.2.4.3.2.1#4rt	TD 4.11 TD 4.13	The Re-timer shall wait at least tIdleRx after a Lane Adapter stops detecting LFPS before enabling the receiver for that Lane Adapter.
4.2.4.3.2.1#5rt	TD 4.11 TD 4.13	For each Adapter, after the last LFPS is transmitted, transition the transmitter to Electrical Idle for tPreData. Then, start transmitting CL_WAKE1.X Ordered Set Symbols, where X is the index of the Re-timer provided by the Router that is the target of the CL_WAKE1.X Ordered Set Symbols.
4.2.4.3.2.1#6rt	NT	The Re-timer shall transmit the Symbols using a locally generated, non-SSC, clock.
4.2.4.3.2.2 Phase 2		
4.2.4.3.2.2#1rt	NT	When a Re-timer receives 3 CL_WAKE2.(X+1) Symbols (where X is the Re-timer Index programmed by the Router that is the source of the CL_WAKE2.(X+1) Symbols), and if the Re-timer is still transmitting on its local clock in this Re-timer Channel, then the Re-timer shall transition this Re-timer Channel to toggle between transmitting two locally-generated CL_WAKE1.X Ordered Set Symbols and transmitting the last two CL_WAKE2.Y Symbols received by the Re-timer Channel.
4.2.4.3.2.2#2rt	NT	CL_WAKE1 Symbols received by the Port shall not be transmitted while the Port is in toggling mode.
4.2.4.3.2.3 Phase 3		
4.2.4.3.2.3#1rt	NT	After a Re-timer receives 3 back-to-back CL_WAKE2.X Symbols (where X is the Re-timer Index programmed by the Router that is the source of the CL_WAKE2.X Symbols) on Lane 0 of a Re-timer Channel in a given direction, the Re-timer shall transition all Re-timer Channels in the opposite direction to transmit on the clock recovered from the received traffic rather than on its local clock.

4.2.4.3.2.3#2rt	NT	A Re-timer Channel shall ignore any received CL_WAKE1.Y (where Y is any value) Symbols interleaved with CL_WAKE2.X Ordered Set Symbols when it determines the reception of back-to-back CL_WAKE2.X Ordered Set Symbols.
4.2.4.3.2.3#3rt	NT	The transition shall happen only after bit lock is achieved by both active receivers in the Re-timer Channel performing the transition.
4.2.4.3.2.3#4rt	TD 4.11 TD 4.13	Each Re-timer Channel performing the transition shall transition to Forwarding state. From this point on, the Re-timer Channel shall forward the bit stream it receives from the Lane and stop generating CL_WAKE1.X Ordered Set Symbols.
4.2.4.3.2.3#5rt	NT	During the transition from local clock to receiver clock, the Re-timer Channel shall meet the SSC_SLEW_RATE requirement as specified in the USB4 Base Specification.
4.2.4.3.3 Timing Requirements		
4.2.4.3.3#1rt	NT	A Re-timer shall meet the following timing requirements during exit from CL0, CL1, or CL2 states:
4.2.4.3.3#2rt	TD 4.11 TD 4.13 TD 4.15	A receiver shall complete Symbol lock within tCLxLock of receiving SLOS or CL_WAKE1.X Ordered Set Symbols.
4.2.4.3.3#3rt	NT	A transmitter shall complete the transition to a recovered clock within tSwitchNoSSC if the received clock is a non-SSC clock.
4.2.4.3.3#4rt	NT	A transmitter shall complete the transition to a recovered clock within tSwitchSSC if the received clock is an SSC clock.
4.3 Lane Decoding		
4.3#1rt	NT	To track entry into CLx states and to participate in exit from CLx states, a Re-timer shall decode Ordered Sets received on its Lane Adapters as defined in the USB4 Specification.
4.3.1 Error Cases		
4.3.1#1rt	NT	Table 4-4 lists the error cases that a Re-timer shall support along with how that error shall be handled.
4.3.1#2rt	NT	If Lane Adapter detects 3 SLOS in Forwarding state with RS-FEC on or Lane Adapter detects 15 SLOS in Forwarding state with RS-FEC off, it is a SLOS Detection Error. If RS-FEC decoding is on, turn-off RS-FEC decoding on this Lane in both USB4 Ports and perform Symbol lock on received SLOS

4.3.1#3rt	NT	If The RS-FEC decoder identifies an uncorrectable error, it is an RS-FEC Decoder error. Turn off RS-FEC decoding on this Lane. Perform Symbol lock on received SLOS.
4.4 Timing Parameters		

Chapter 6

The following Table presents the USB4 Re-timer Specification Chapter 6 asserts.

Assertion #	Test Name	Assertion Description
6 Interoperability with Thunderbolt™ 3 (TBT3) Systems		
6#1rt	NT	A Cable Re-timer shall support the requirements defined in this chapter.
6.2 Logical Layer		
6.2.1 Sideband Channel		
6.2.1#1rt	NT	This section defines the additional Sideband Channel behavior that a Re-timer shall implement when operating in a TBT3-Compatible that uses a TBT3-Compatible Sideband Channel
6.2.1.1 Bidirectional Re-timers		
6.2.1.1.1 Cable Re-timers		
6.2.1.1.1#1rt	IOP	A Cable Re-timer shall implement a unidirectional behavior when the Sideband Channel operates in TBT3-Compatible mode.
6.2.1.1.2 On-Board Re-timers		
6.2.1.1.2#1rt	NT	An On-Board Re-timer that is adjacent to a USB Type-C connector shall implement both unidirectional and bidirectional behavior.
6.2.1.1.2#2rt	IOP	When the Re-timer is adjacent to a Thunderbolt Cable Re-timer, it shall operate as a bidirectional Re-timer on its Cable-Facing USB4 Port. The Router-Facing USB4 Port shall operate as a unidirectional Re-timer.
6.2.1.1.2#3rt	IOP	When the Re-timer is not adjacent to a Thunderbolt Cable Re-timer, it shall operate as a unidirectional Re-timer on both USB4 Ports.
6.2.1.1.2#4rt	IOP	An On-Board Re-timer that is not adjacent to a USB Type-C connector shall implement unidirectional behavior on both USB4 Ports.
6.2.1.1.2#5rt	NT	When a USB4 Port on an On-Board Re-timer is operating in bidirectional mode: The USB4 Port shall support concurrent reception of Transactions on SBTX and on SBRX.
6.2.1.1.2#6rt	NT	When a USB4 Port on an On-Board Re-timer is operating in bidirectional mode: The USB4 Port shall drive its SBTX for up to 2 bit times after the last Stop bit of an AT Command.
6.2.1.1.2#7rt	NT	When a USB4 Port on an On-Board Re-timer is operating in bidirectional mode: The USB4 Port shall not forward a received Transaction if it is still waiting for a Response to a RT Command it sent.

6.2.1.2 Transactions		
6.2.1.2.1 LT Transactions		
6.2.1.2.1#1rt	IOP	A Re-timer shall forward an LT_Resume Transaction received on one USB4 Port to its other USB4 Port.
6.2.1.2.1#2rt	IOP	A Cable Re-timer shall forward an LT_Resume2 Transaction received on its Router-Facing USB4 Port to its Cable-Facing USB4 Port.
6.2.1.2.1#3rt	IOP	A Re-timer shall forward a received LT_Gen_2 Transaction to its other USB4 Port.
6.2.1.2.1#4rt	IOP	A Re-timer shall forward a received LT_Gen_3 Transaction to its other USB4 Port.
6.2.1.2.2 AT Transactions		
6.2.1.2.2.1 Cable Re-timers		
6.2.1.2.2.1#1rt	NT	A Cable Re-timer shall support the Bounce mechanism as defined in the USB4 Specification.
6.2.1.2.2.1#2rt	NT	A Cable Re-timer shall not initiate AT Commands.
6.2.1.2.2.1#3rt	NT	A Cable Re-timer shall respond to a received AT Command that has the Recipient bit set to 0b and the *Bounce* bit set to 0b.
6.2.1.2.2.1#4rt	NT	Else, it shall forward the received AT Command to its other USB4 Port.
6.2.1.2.2.2 On-Board Re-timers		
6.2.1.2.2.2#1rt		An On-Board Re-timer shall respond to a received AT Command with the *Recipient* bit set to 1b that access the TxFFE Register in the SB Register Space.
6.2.1.2.2.2#2rt		It shall forward other received AT Commands to its other USB4 Port.
6.2.1.2.2.2#3rt		An On-Board Re-timer shall process to a received AT Response with the *Recipient* bit set to 1b that access the TxFFE Register in the SB Register Space.
6.2.1.2.2.2#4rt		It shall not forward the AT Response to its other USB4 Port.
6.2.1.2.2.2#5rt		It shall forward other received AT Responses to its other USB4 Port.
6.2.1.2.3 RT Transactions		
6.2.1.2.3#1rt	NT	An On-Board Re-timer that is adjacent to a USB Type-C connector shall not forward Broadcast RT Transactions towards the cable.

6.2.1.2.4 SB Register Space		
6.2.1.2.4#1rt	TBD	The SB Register Space of a Re-timer shall have the additional fields described in Table 6-1 and Table 6-2.
6.2.1.3 Lane Initialization		
6.2.1.3.1 Phase 1 – Determination of Initial Conditions		
6.2.1.3.2 Phase 2 – Lane Parameters Synchronization		
6.2.1.3.2#1rt	IOP	An On-Board Re-timer shall decode Broadcast RT Transactions, LT_Gen_2 Transactions, and LT_Gen_3 Transactions, and shall use the Link parameter from the most recently received Transaction.
6.2.1.3.2#2rt	NT	A Cable Re-timer shall decode LT_Gen_2 Transactions and LT_Gen_3 Transactions, and shall use the Link parameter from the most recently received LT Transaction.
6.2.1.3.2#3rt	NT	If, on any USB4 Port, a Cable Re-timer detects LT_Resume for Lane 0 before it detects at least one LT_Gen_2 Transaction or LT_Gen_3 Transaction for Lane 1, then the Re-timer shall keep the Lane 1 Adapters in both USB4 Ports in the CLd state and shall not proceed with Lane Initialization.
6.2.1.3.2#4rt	IOP	When a Re-timer detects LT_Resume on any Lane of any USB4 Port, it shall transition to phase 5.
6.2.1.3.3 Phase 3 – Lane Equalization		
6.2.1.3.3#1rt	IOP	Table 6-3 lists which TxFFE negotiation flows a transmitter or receiver shall perform in phase 5.
6.2.1.3.3#2rt	NT	An On-Board Re-timer Lane Adapter that is not adjacent to a USB Type-C connector shall turn on its transmitter when the *Rx Active* bit of its Corresponding Receiver is set to 1b.
6.2.1.3.3#3rt	NT	An On-Board Re-timer Lane Adapter that is not adjacent to a USB Type-C connector: It shall start transmitting CL_WAKE1.X Ordered Set Symbols, where X is the Re-timer Index assigned by the Router that is the target of the CL_WAKE1.X Ordered Set Symbols.
6.2.1.3.3#4rt	NT	An On-Board Re-timer Lane Adapter that is not adjacent to a USB Type-C connector: The transmitter shall use a locally generated, non-SSC clock to transmit the CL_WAKE1.X Ordered Set Symbols.
6.2.1.3.3#5rt	NT	An On-Board Re-timer Lane Adapter that is not adjacent to a USB Type-C connector: It shall then set the *Tx Active* bit for the Lane Adapter to 1b.
6.2.1.3.3#6rt	NT	A Re-timer adjacent to a USB Type-C connector shall set the *Clock* Switch *Done* bit to 1b in a Router-Facing Adapter when all receivers in Router-Facing Adapters complete TxFFE negotiation.

6.2.1.3.3#7rt	NT	Once the *Clock Switch Done* bit is set to 1b, a transmitter adjacent to a USB Type-C connector that is turned on shall forward the bit stream it receives from the Corresponding Receiver using a recovered clock.
6.2.1.3.3#8rt	NT	When all of the following are true, a transmitter that is not adjacent to a USB Type-C connector shall stop using the local clock, shall start using the recovered clock from the Corresponding Receiver, and shall forward the bit stream it receives from the Corresponding Receiver: In the transmitter's USB4 Port, TxFFE negotiation is complete between all transmitters and their Adjacent Receivers; In the USB4 Port opposite the transmitter's USB4 Port, TxFFE negotiation is complete between all receivers and their Adjacent Transmitter; The *Clock Switch Done* bit for Lane 0 of the transmitter's adjacent USB4 Port is 1b.
6.2.1.3.3#9rt	NT	A Re-timer adjacent to a Router shall set the *Forward Switch Done* bit to 1b in a Lane Adapter of a Cable-Facing USB4 Port when transmitter of the Lane Adapter is using the receiver clock from the Corresponding Receiver.
6.2.1.3.3#10rt	NT	A Re-timer shall set the *Forward Switch Done* bit to 1b in a Lane Adapter if the *Forward Switch Done* bit is set to 1b in the adjacent USB4 Port of the Corresponding Receiver.
6.2.1.3.3#11rt	NT	When the *Forward Switch Done* bit is set to 1b in an adapter adjacent to a USB Type-C connector, the Lane Adapter shall turn on its transmitter, if it has not done so already. It shall then set the *Tx Active* bit to 1b and perform TxFFE Parameter Negotiation.
6.2.1.3.3#12rt	NT	When an On-Board Re-timer transmitter completes TxFFE negotiation with a Cable Re-timer receiver, the transmitter shall send an LT_Resume2 Transaction. The *LSELane* field in the LT_Resume2 Transaction shall equal the Lane number associated with the transmitter.
6.2.1.3.3#13rt	NT	A Cable Re-timer shall set the *Tx Active* bit to 1b in a Router-Facing Adapter when the Lane Adapter is transmitting the bit stream received by a Lane Adapter at the other end of the Cable, and transmission uses the recovered clock from the Lane Adapter at the other end of the Cable.
6.2.1.3.3.1 Asymmetric TxFFE Parameter Negotiation with a Receiving Subordinate Partner		
Receiver flow:		
6.2.1.3.3.1#1rt	IOP	The steps that the receiver shall perform to complete negotiation are listed below:
6.2.1.3.3.1#2rt	NT	1) The receiver shall set the following initial values on entry to Phase 5: Local Rx Status & TxFFE Request byte of the *TxFFE* register: *Rx* Locked bit = 0b; *TxFFE Request* field = index of an initial set of TXFFE parameters; *Rx Active* bit =0b; *New Request* bit = 0b; *Partner Tx Status* byte of the *TxFFE* register: *Tx Active* bit = 0b; Request Done bit = 0b.

6.2.1.3.3.1#3rt	NT	2) The receiver shall evaluate the value of the *Tx Active* bit in the *Partner Tx Status* byte of the *TxFFE* register: If *Tx Active* = 1b (i.e. the transmitter is transmitting), then the receiver shall enable the receiver, set *Rx Active* bit to 1b, and continue to Step 3.
6.2.1.3.3.1#4rt	NT	2) The receiver shall evaluate the value of the *Tx Active* bit in the *Partner Tx Status* byte of the *TxFFE* register: Else, repeat Step 2 within tPollTxFFE.
6.2.1.3.3.1#5rt	NT	3) The receiver shall evaluate its behavior. If equalization is complete, the receiver shall set the *Rx Locked* field in the *Local Rx Status & TxFFE Request* byte to 1b
6.2.1.3.3.1#6rt	NT	4) The receiver shall do the following: If the *Rx Locked* bit is set to 1b, negotiation is complete and no further TxFFE negotiation steps shall be taken.
6.2.1.3.3.1#7rt	NT	4) The receiver shall do the following: Else: *TxFFE Request* field shall be set to the index of a selected set of TXFFE parameters; *New Request* bit shall be set to 1b to indicate the receiver is providing a new TxFFE index.
6.2.1.3.3.1#8rt	NT	5) Continue to Step 6 only after sending a read Response with the updated values of its TxFFE Register.
6.2.1.3.3.1#9rt	NT	6) On reception of an AT Command with a write Command targeting its *Partner Tx Status* byte of the *TxFFE* register, the receiver shall: If (*Tx* Active = 1b) AND (*TxFFE setting* = value of *TxFFE Request* in the *Local Rx Status & TxFFE Request* byte), go to Step 7.
6.2.1.3.3.1#10rt	NT	6) On reception of an AT Command with a write Command targeting its *Partner Tx Status* byte of the *TxFFE* register, the receiver shall: Else, repeat Step 6.
6.2.1.3.3.1#11rt	NT	7) The receiver shall evaluate its receiver behavior. If equalization is complete, the receiver shall set the *Rx Locked* field in the *Local Rx Status & TxFFE Request* byte to 1b.
6.2.1.3.3.1#12rt	NT	8) The receiver shall set the *New Request* field in the *Local Rx Status & TxFFE Request* byte to 0b.
6.2.1.3.3.1#13rt	NT	9) On reception of an AT command with a read Command targeting the TxFFE register go to Step 4.
6.2.1.3.3.2 – Asymmetric TxFFE Parameter Negotiation with a Transmitting Subordinate Partner		
Transmitter flow:		
6.2.1.3.3.2#1rt	IOP	The steps that the transmitter shall perform to complete negotiation are listed below:

6.2.1.3.3.2#2rt	NT	1) The transmitter shall set the following initial values on entry to Phase 5: *Local Tx Status* byte of the TxFFE register: *Tx Active* bit = 1b; *Request Done* bit = 0b; *TxFFE Setting* field = index of an initial set of TxFFE parameters; Partner Rx Status & TxFFE Request byte of the TxFFE register: *New Request* bit = 0b.
6.2.1.3.3.2#3rt	NT	2) On reception of an AT Command with a write Command targeting the *Partner Rx Status & TxFFE Request* byte of the *TxFFE* register, the transmitter shall: If (*New Request* = 0b), repeat Step 2.
6.2.1.3.3.2#4rt	NT	2) On reception of an AT Command with a write Command targeting the *Partner Rx Status & TxFFE Request* byte of the *TxFFE* register, the transmitter shall: Else, continue to Step 3.
6.2.1.3.3.2#5rt	NT	3) Load one of 16 predefined TxFFE configurations that matches the *TxFFE Request* field of the received AT Command.
6.2.1.3.3.2#6rt	NT	4) Send an AT Response to indicate the transmitter is using the new TxFFE request.
6.2.1.3.3.2#7rt	NT	5) On reception of an AT Command with a write Command targeting the *Partner Rx Status & TxFFE Request* byte of the TxFFE register, the transmitter shall: If (*New Request* = 1b), repeat Step 4.
6.2.1.3.3.2#8rt	NT	5) On reception of an AT Command with a write Command targeting the *Partner Rx Status & TxFFE Request* byte of the TxFFE register, the transmitter shall: Else, continue to Step 2.
6.2.2 Re-timer Channel State Machine		
6.2.2.1 CLd State		
6.2.2.1.1 Behavior in State		
6.2.2.1.1#1rt	NT	In addition to the conditions described in Section 4.2.1.2, a Re-timer Channel shall begin Lane Initialization in phase 4 when: If the Re-timer Channel entered this state after detecting an LT_Fall Transaction, then: The Re-timer Channel for Lane 0 shall start Lane Initialization when the Re-timer receives a Broadcast RT Transaction with the *Lane0 Enabled* bit set to 1b, an LT_Gen_2 Transaction with the *LSELane* bit set to 0b, or an LT_Gen_3 Transaction with the *LSELane* bit set to 0b.
6.2.2.1.1#2rt	NT	In addition to the conditions described in Section 4.2.1.2, a Re-timer Channel shall begin Lane Initialization in phase 4 when: If the Re-timer Channel entered this state after detecting an LT_Fall Transaction, then: The Re-timer Channel for Lane 1 shall start Lane Initialization when the Re-timer receives a Broadcast RT Transaction with the *Lane1 Enabled* bit set to 1b, an LT_Gen_2 Transaction with the *LSELane* bit set to 1b, or an LT_Gen_3 Transaction with the *LSELane* bit set to 1b.

Test Requirements

Hardware

Vendor provides the Unit Under Test (UUT) in a reference system for testing. The reference system must expose one USB Type-C™ connector per USB4™ Port. The USB Type-C connector is the test point for the UUT.

For a USB4 host:

- Reference system must be x64-based, run Windows 10
- Host Router must be PCIe-based

Note: In the future, will expand host testing to other OS and architectures.

Timing

Exerciser adds additional time to simulate 2 Cable Re-timers and 2 On-Board Re-timers (worst case latency) on the Link between Exerciser and UUT. The total roundtrip latency is calculated as follows:

Total Latency = 2 (# of Re-timers) (individual Re-timer Latency)

For Gen 2 speeds, the Exerciser adds 400 ns delay.

Total Latency = 2(4)(50 ns) = 400 ns

For Gen 3 speeds, the Exerciser adds 240 ns delay.

Total Latency = 2(4)(30 ns) = 240 ns

Product

The Vendor Info File (VIF) is used in conjunction with test software to indicate RUT product implementation. This file can be generated using the following tool:

http://www.usb.org/developers/tools/#PDFile

https://www.usb.org/document-library/usb-vendor-info-file-generator-version-2010

Note: The VIF may be generated by test equipment vendors as well.

USB4 Mode Test Setups

This section defines the test setups for a Router Assembly that is part of a USB4™ host, hub, or device. The test setups in this section are used for the USB4 Mode Tests.

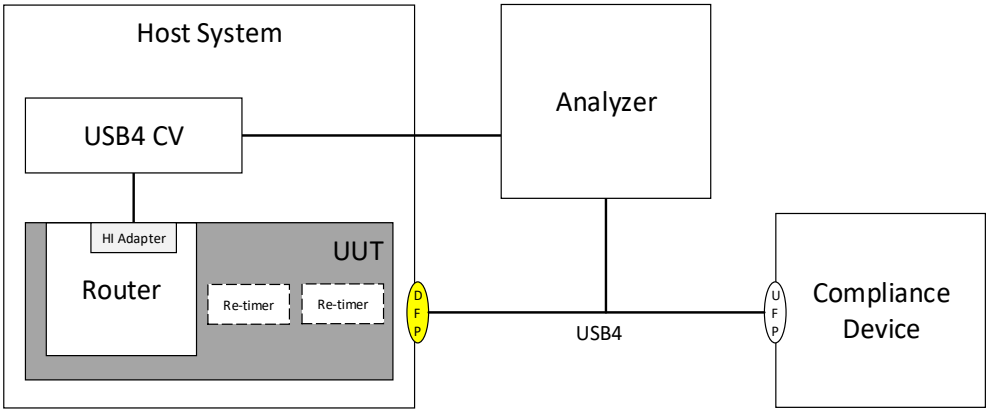
A USB4-Based Dock is tested as a USB4 hub.

USB4 Host

This section describes the test setups for a Router Assembly that is part of a USB4 host. The Port Under Test (PUT) is highlighted in each figure.

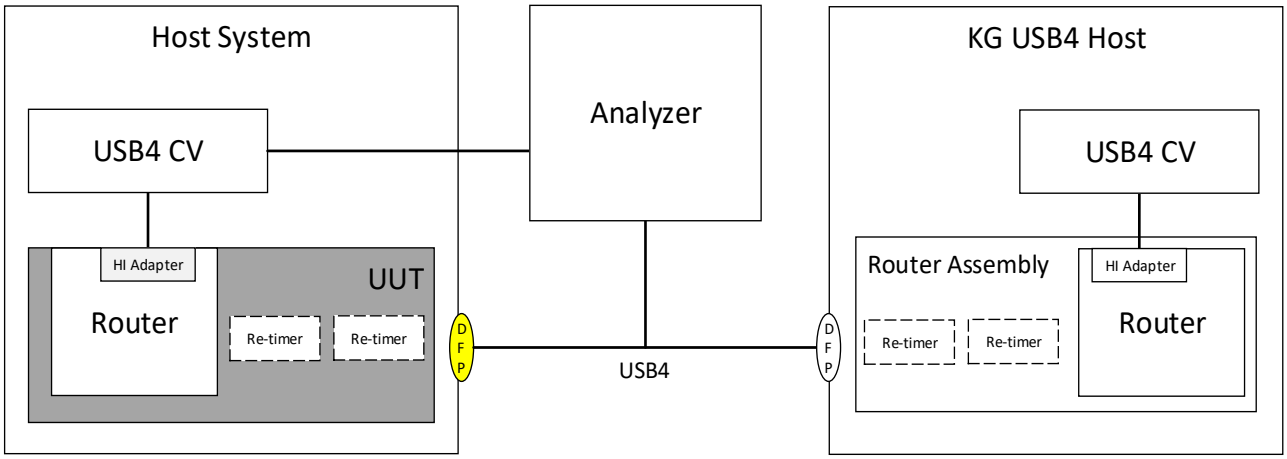
Setup H1 – DFP Test Setup with Compliance Device

- A Compliance Device is connected to the DFP of the UUT
- USB4 CV is installed on the Host System with the UUT
- A USB4 Analyzer is connected between the UUT and Compliance Device



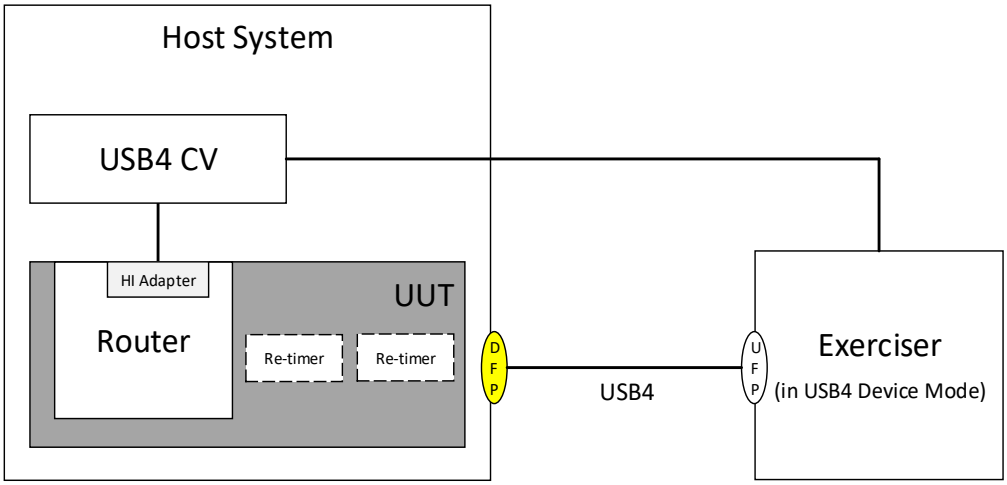
Setup H2 – DFP Test Setup with KG USB4 Host

- A KG USB4 host is connected to the UUT
- USB4 CV is installed on the Host System with the UUT
- A USB4 Analyzer is connected between the UUT and KG USB4 Host



Setup H3 – DFP Test Setup with Exerciser (Single-Domain)

- The Exerciser is connected to the UUT
- The Exerciser is configured as a USB4 UFP
- USB4 CV is installed on the Host System with the UUT

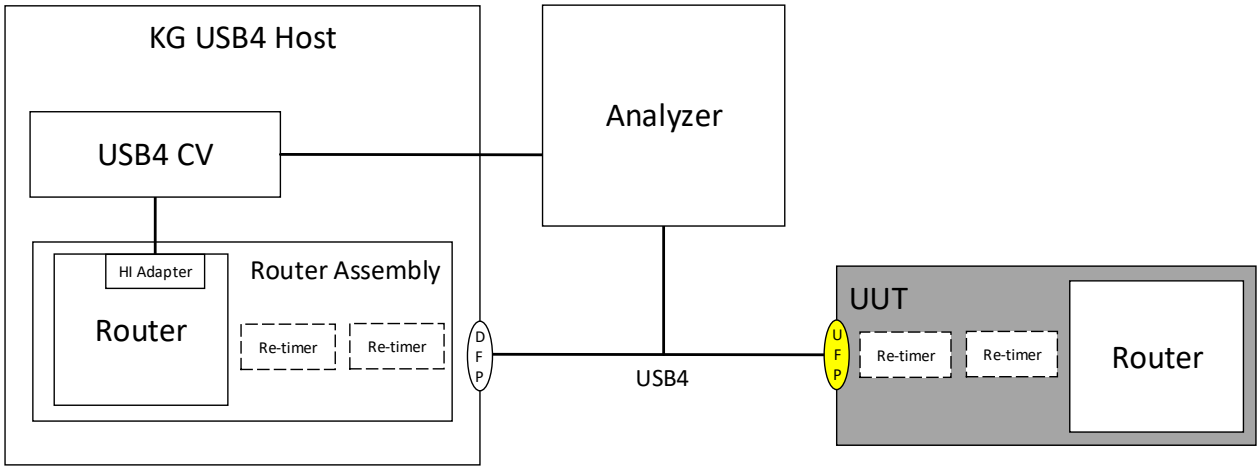


USB4 Device

This section describes the test setup for a Router Assembly that is part of a USB4 device. The Port Under Test (PUT) is highlighted in each figure.

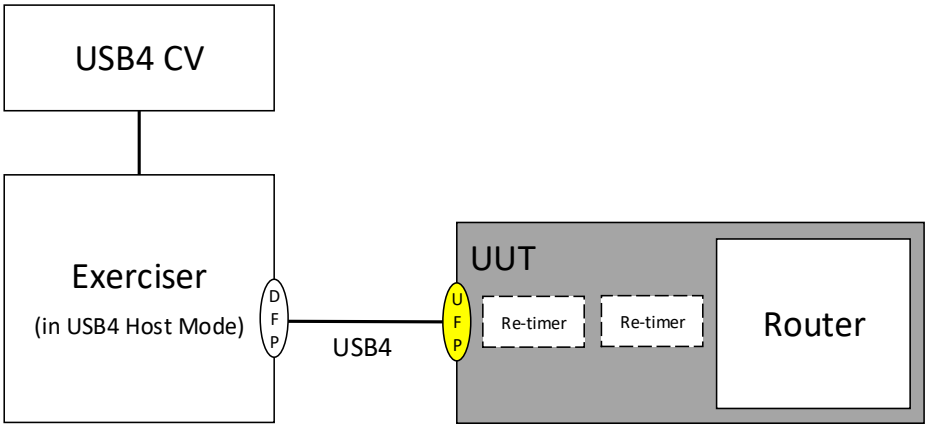
Setup D1 – UFP Test Setup with KG USB4 Host

- A KG USB4 Host is connected to the UUT
- USB4 CV is installed on the KG Host System
- A USB4 Analyzer is connected between the UUT and KG USB4 Host



Setup D2 – UFP Test Setup with Exerciser

- The Exerciser is connected to the UUT
- The Exerciser is configured as a USB4 DFP

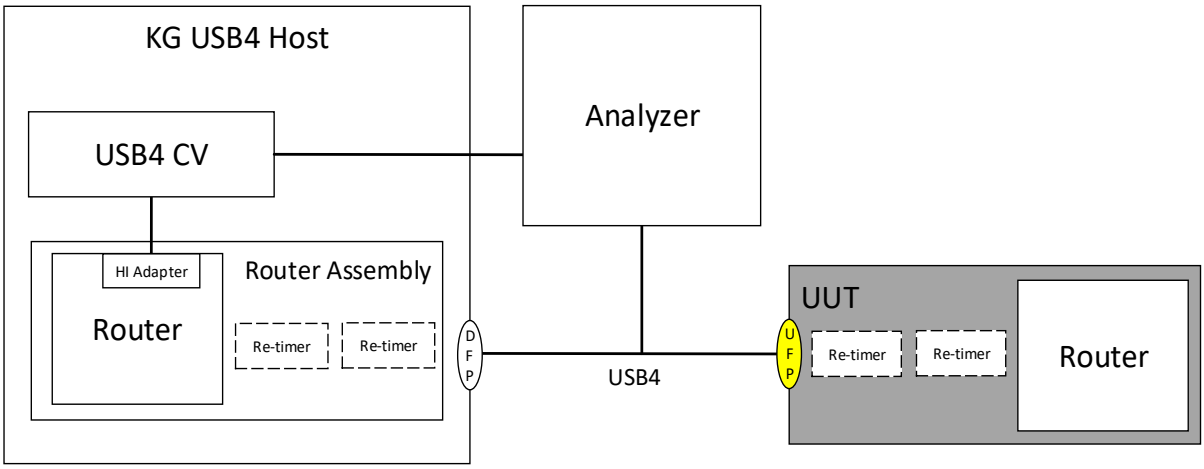


USB4 Hub

This section describes the test setups for a Router Assembly that is part of a USB4 hub. The Port Under Test (PUT) is highlighted in each figure.

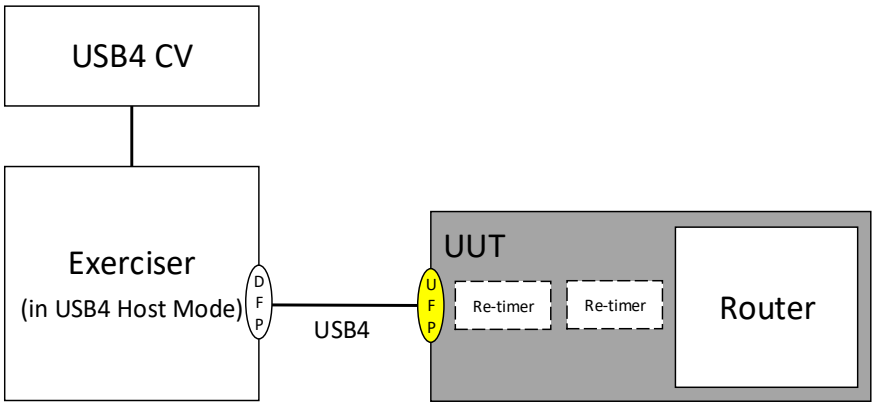
Setup D3 – UFP Test Setup with KG USB4 Host

- A KG USB4 Host is connected to the UUT
- USB4 CV is installed on the KG Host System
- A USB4 Analyzer is connected between the UUT and Compliance Device



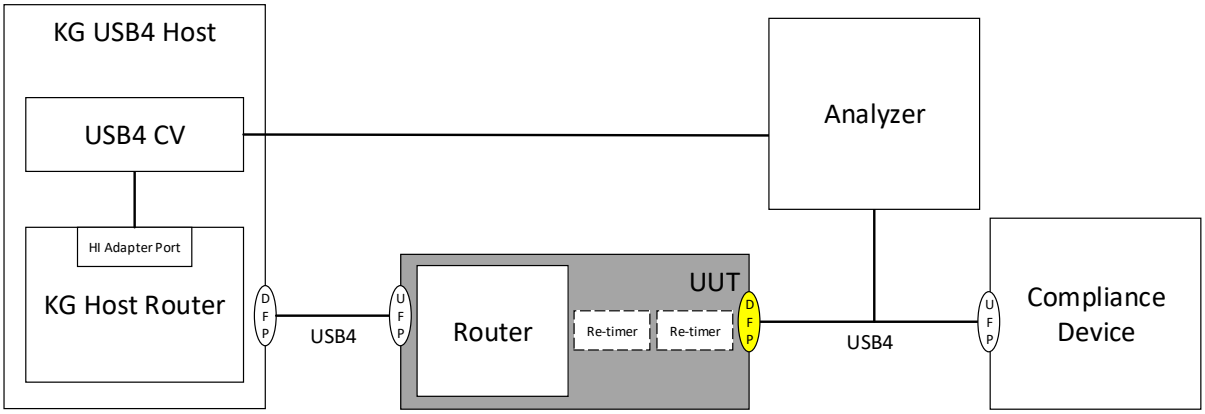
Setup D4 – UFP Test Setup with Exerciser

- The Exerciser is connected to the UUT
- Exerciser is configured as a USB4 DFP



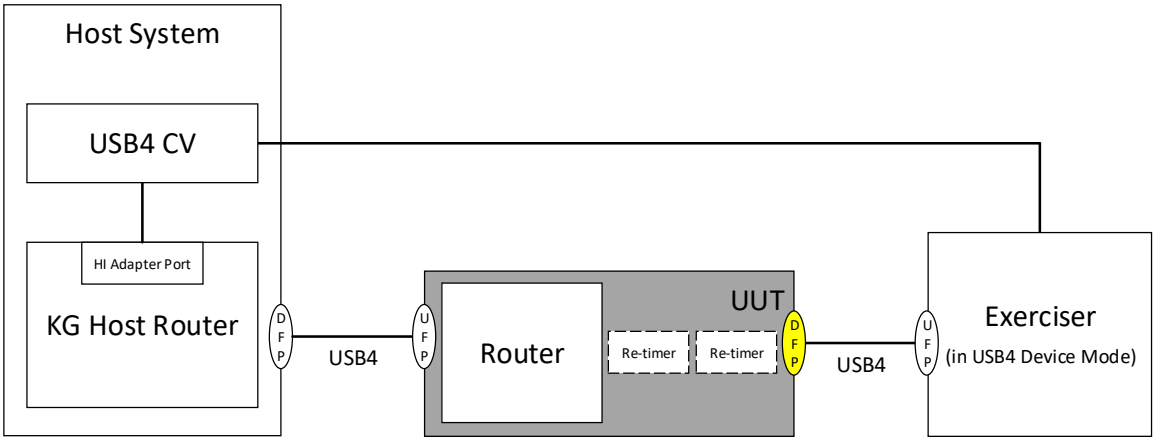
Setup D5 – DFP Test Setup with Compliance Device

- A KG USB4 host is connected to the UFP of the UUT
- A Compliance Device is connected to the DFP of the UUT
- USB4 CV is installed on the KG Host System
- A USB4 Analyzer is connected between the UUT and Compliance Device



Setup D6 – DFP Test Setup with Exerciser (Single-Domain)

- A KG USB4 host is connected to the UFP of the UUT
- The Exerciser is connected to the DFP of the UUT
- The exerciser is configured as a USB4 UFP



TBT3-Compatibility Mode Test Setups

This section defines the test setups for a Router Assembly that is part of a USB4™ host, hub, or device. The test setups in this section are used for the TBT3-Compatibility Tests.

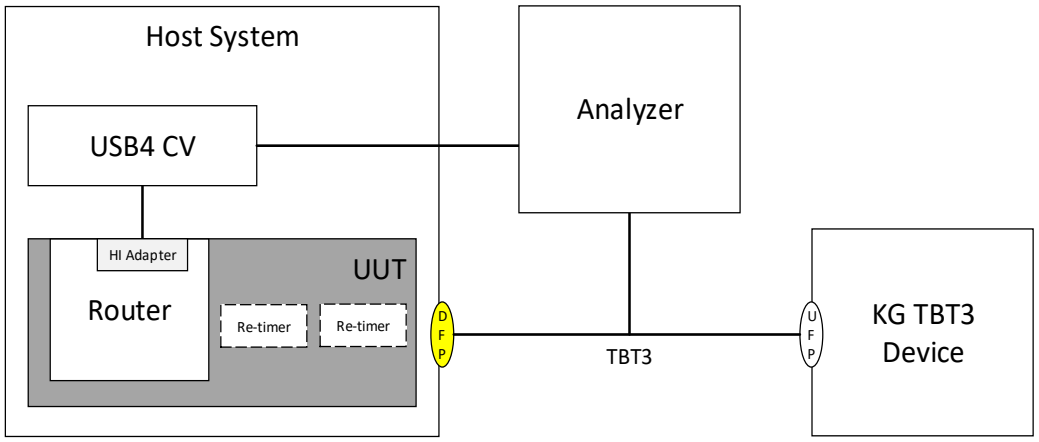
A USB4-Based Dock is tested as a USB4 hub.

USB4 Host

This section describes the test setups for a Router Assembly that is part of a USB4 host. The Port Under Test (PUT) is highlighted in each figure.

Setup H4 – DFP Test Setup with KG TBT3 Device

- A KG USB4 device is connected to the UUT
- USB4 CV is installed on the Host System with the UUT
- A TBT3 Analyzer is connected between the UUT and KG TBT3 Device

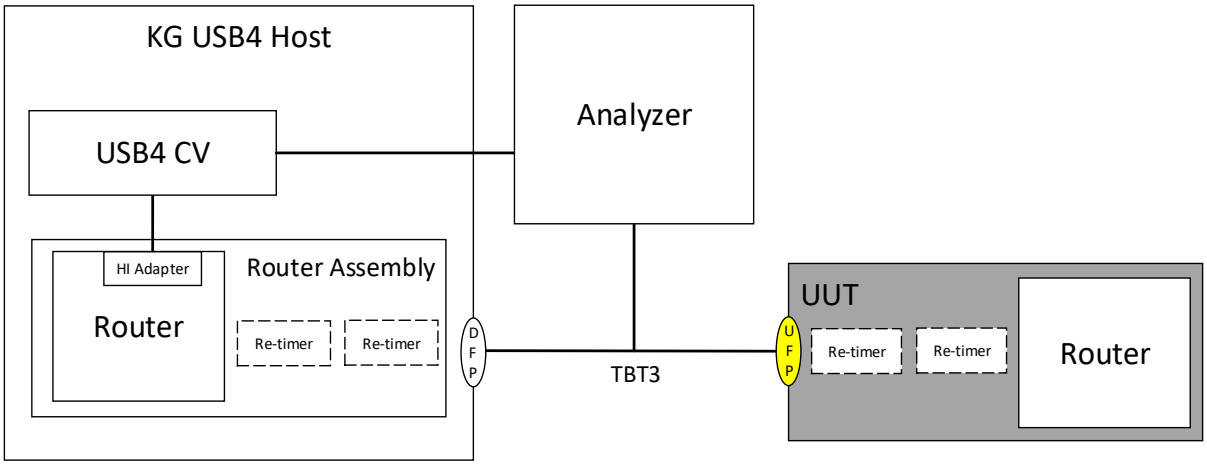


USB4 Device

This section describes the test setup for a Router Assembly that is part of a USB4 device. The Port Under Test (PUT) is highlighted in each figure.

Setup D7 – UFP Test Setup with KG USB4 Host

- A KG USB4 Host is connected to the UUT via certified TBT3 active cable
- USB4 CV is installed on the KG Host System
- A TBT3 Analyzer is connected between the UUT and KG USB4 Host

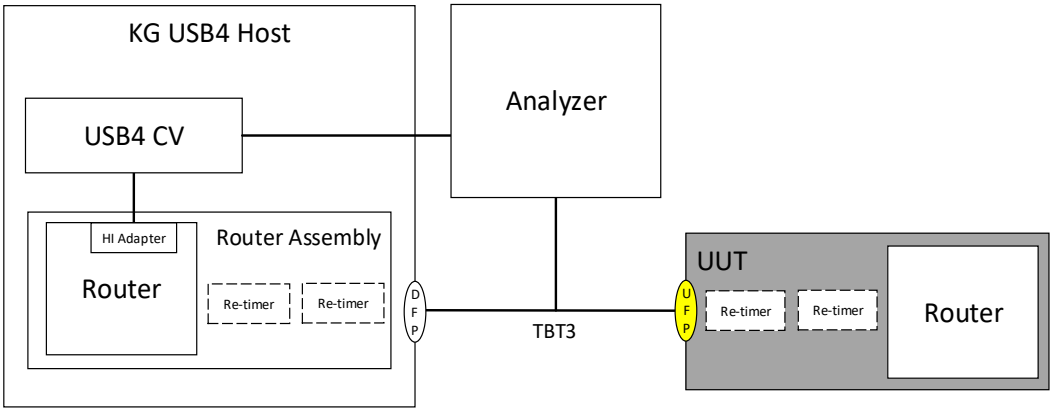


USB4 Hub

This section describes the test setups for a Router Assembly that is part of a USB4 hub. The Port Under Test (PUT) is highlighted in each figure.

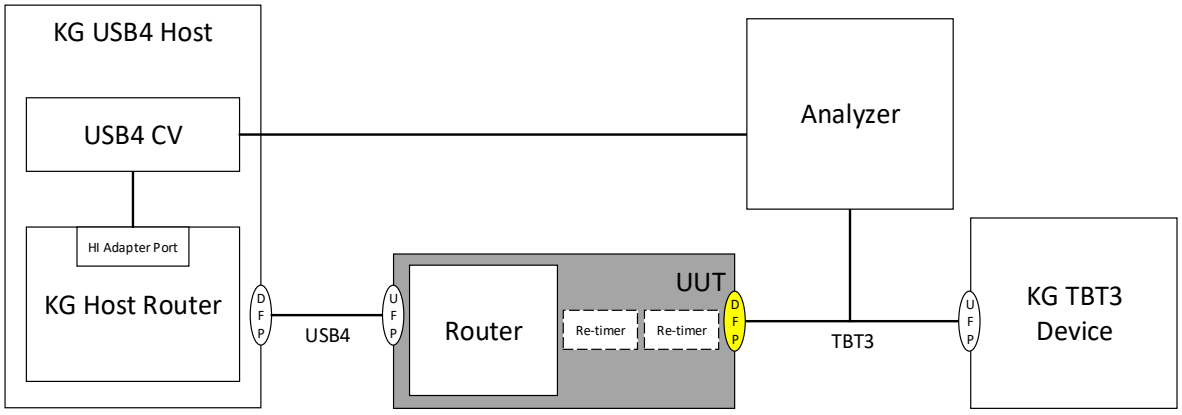
Setup D8 – UFP Test Setup with KG USB4 Host

- A KG USB4 Host is connected to the UUT via certified TBT3 active cable
- USB4 CV is installed on the KG Host System
- A TBT3 Analyzer is connected between the UUT and KG USB4 Host



Setup D9 – DFP Test Setup with KG TBT3 Device

- A KG USB4 Host is connected to the UFP of the UUT
- A KG TBT3 Device is connected to the DFP of the UUT
- USB4 CV is installed on the KG Host System
- A USB4 Analyzer is connected between the UUT and KG TBT3 Device



Subroutines

Router Enumeration Procedure

The steps in this section are performed whenever a test step calls for a Router to be enumerated.

1. Wait for a Hot Plug Event Packet with UPG=0 for Lane 0 and Lane 1
2. Set the *Lock* bit in the Port that detected the connection to 0b
3. Send the UUT a Write Request that writes the following fields:
    a. *Connection Manager USB4 Version* = 1.0 (for a USB4 Connection Manager)
    b. *Connection Manager USB4 Version* = 0.0 (for a TBT3 Connection Manager)
    c. *Topology ID* = Router TopologyID (assigned per USB4 Specification)
    d. *Depth* = Router depth (0 for a Host Router, or 1 for a Device Router)
    e. *Valid* = 1b

Lane Bonding Initiation Procedure

The steps in this section are performed whenever a test step calls for Lane bonding to be initiated.

1. Send the UUT a Write Request that writes the following fields:
    a. *Target Link Width* = 1b
2. Send the Link Partner of the UUT a Write Request that writes the following fields:
    a. *Target Link Width* = 1b
3. Send the Lane 0 Adapter in the DFP (whether it's the UUT or its Link Partner) a Write Request that writes the following fields:
    a. *Lane Bonding* = 1b
4. Wait for a Hot Plug Packet with UPG=1 for Lane 1

Router Assembly Reset Procedure

The steps in this section are performed whenever a test calls for a UUT to be reset.

Host Router

1. Teardown any Paths in the RUT
2. Disable, then enable all Transmit and Receive Rings
3. Perform a DFP Reset in each of the Downstream Facing Ports
4. Reset the Host Interface using the Host Interface Reset Register

Device Router

Upstream of the UUT in the DFP that is connected to the UUT:

1. Set the *Downstream Port Reset* bit to 1b
2. Read the *Lock* bits for the Lane 0 and Lane 1 Adapters
3. Poll the *Lock* bits until both are 1b
4. Set the *Downstream Port Reset* bit to 0b

Router Assembly Connect Procedure

The steps in this section are performed whenever a test calls for a USB4 device or the Exerciser to be connected to a USB4 Port. The Adapters in the DFP being connected are enabled, which simulates a new connection.

Upstream of the UUT in the DFP that is being connected:

1. Set the *Lane Disable* bit in the Lane 0 Adapter to 0b
2. Wait at least tDisabled time (10ms)
3. Set the *Lane Disable* bit in the Lane 1 Adapter to 0b
4. Set the *Lock* bit in the DFP to 0b

Note: This step assumes that the USB4 device/Exerciser is physically connected to the DFP and the DFP Adapters have been disabled using the Router Assembly Disconnect Procedure below.

Router Assembly Disconnect Procedure

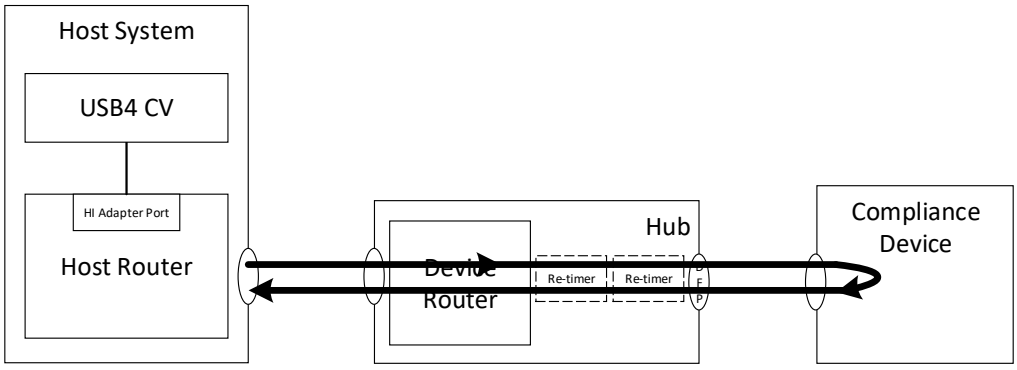
The steps in this section are performed whenever a test calls for a USB4 device or the Exerciser to be disconnected from a USB4 Port. The Adapters in the DFP being disconnected are disabled, which simulates a disconnect.

Upstream of the UUT in the DFP that is connected to the device being disconnected:

1. Set the *Lane Disable* bit in the Lane 1 Adapter to 1b
2. Wait for a Hot Plug Event Packet with UPG=1 for Lane 1
3. Set the *Lane Disable* bit in the Lane 0 Adapter to 1b
4. Wait for a Hot Plug Event Packet with UPG=1 for Lane 0

Loopback Path Setup

A Loopback Path allows USB4 CV to inject traffic into a USB4 fabric by sending itself USB4 Packets using Host-to-Host Tunneling. The USB4 Packets are generated by USB4 CV and routed through the UUT out to the Compliance Device and back through the UUT. The loopback Path uses Ring 1.



The steps in this section are performed whenever a test calls for a loopback path to be setup.

Note: When Lanes are bonded, only Lane 0 Path Configuration Space needs to be configured.

Part 0 – Configure Adapters Credits fields

Upstream of the UUT, in each Lane Adapter along the loopback Path configure the following:

- If loopback path is set for Flow Control Disabled, set *Non-Flow Controlled Buffers* in the Adapter Configuration Space to: *Total Buffers – Path Credits Allocated* for Path 0
- If loopback path is set for Restricted Shared or Shared, set *Link Credits Allocated* in the Adapter Configuration Space to: MAX(*Total Buffers, 128)* – *Path Credits Allocated* for Path 0

Part 1 – Configure the Path Segments

Upstream of the UUT, in each Adapter along the loopback Path starting with the Source Adapter and ending with the Destination Adapter:

1. For all Adapters, configure the HopID/routing table using the following fields in Path Configuration Space:
    a. *Output Adapter*
    b. *Output HopID*
    c. *Priority*
    d. *Weight*
2. If Adapter is Lane Adapter, set the Flow Control parameters using the following fields in Path Configuration Space:
    a. *Path Credits Allocated*
    b. *ESE*
    c. *ISE*
    d. *EFC*
    e. *IFC*
3. Set the *Valid* bit in Path Configuration Space to 1b

Part 2 – Enable Loopback

After all Path segments are configured, do the following in each Protocol Adapter along the loopback Path starting with the Source Adapter and ending with the Destination Adapter

4. Set the *Enable* bit in Adapter Configuration Space to 1b

Loopback Path Teardown

The steps in this section are performed whenever a test calls for a loopback Path to be torn down.

Part 1 – Disable Loopback

Upstream of the UUT, in each Protocol Adapter along the loopback Path starting with the Destination Adapter and ending with the Source Adapter:

1. Set the *Enable* bit in Adapter Configuration Space to 0b

Part 2 – Teardown Path Segments

Upstream of the UUT in each Adapter along the loopback Path starting with the Destination Adapter and ending with the Source Adapter:

2. Set the *Valid* bit in Path Configuration Space to 0b

3. Read the *Pending Requests* bit in Path Configuration Space
4. Poll the *Pending Requests* bit until it is 0b
5. Wait tTeardown time

Transition Host System to Sleep

The steps in this section are performed whenever a test calls for the hosts system to be transitioned to sleep.

1. Set *Enter Sleep* bit to 1b
2. Poll the *Sleep Ready* bit until it is 1b
3. In the Host Router, transition PCIe PERST# from high to low

Initiate Read From SB Register Space

The steps in this section are performed whenever a test calls for a Read Command to be sent.

1. Write to the following fields in the USB4 Port Capability in PUT Configuration Space:
    a. *Target*
    b. *Address*
    c. *Length*
    d. *WnR* = 0 (Read)
2. Set the *Pending* bit in the USB4 Port Capability in PUT Configuration Space to 1b
3. Poll the *Pending* bit until it is 0b
4. Read the following fields and verify values:
    a. *No Response* = 0
    b. *Result Code* = 0 (success)

Initiate Write to SB Register Space

The steps in this section are performed whenever a test calls for a Write Command to be sent.

1. Write to the following fields in the USB4 Port Capability in PUT Configuration Space:
    a. *Target*
    b. *Address*
    c. *Length*
    d. *WnR* = 1 (Write)
    e. *Data* DW
2. Set the *Pending* bit in the USB4 Port Capability in PUT Configuration Space to 1b
3. Poll the *Pending* bit until it is 0b
4. Read the following fields and verify values:
    a. *No Response* = 0
    b. *Result Code* = 0 (success)

USB4 Mode Tests – No Exerciser

The tests in this section are performed in USB4 mode, where all connected Ports negotiate and enter USB4 operation as described in the USB Type-C Specification and the USB PD Specification. The Sideband Channel operates as a USB4 Sideband Channel.

Unless specified otherwise, the tests in this section are performed on all Ports of a UUT. The tests are performed at the highest speed that the UUT supports. Lanes are bonded and RS-FEC is enabled.

Unless otherwise noted, a test will timeout if it takes more than 500ms to go from one step to the next step. It is a test failure if a test step times out.

Sideband Channel Tests

The tests in this section verify that the Sideband Channel of the PUT is compliant with the USB4 Specification.

Background Check

This test is performed by the Analyzer or Exerciser in conjunction with all of the Sideband Channel Tests.

1. Parse each LT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.1#1)
    a. A DLE symbol (FEh)
    b. A LSE symbol
    c. A CLSE symbol
2. Parse the LSE Symbol in each LT Transaction and verify that:
    a. Bits [7:6] (*StartLT*) are set to 10b (4.1.1.2.1#4)
    b. Bit 5 (*LSELane*) is 0 for an LT_LRoff Transaction (4.1.1.2.1#3)
    c. Bit 4 is reserved (0b) (1.7#5)
    d. Bits [3:0] (*LSESymbol*) do not contain reserved values (1.7#1)

    Note: Defined LSESymbol values are 0000b (LT_Fall), 0010b (LT_Resume), and 0011b (LT_LRoff)
3. Parse each AT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.2#1)
    a. A DLE symbol (FEh)
    b. A STX symbol
    c. No more than 66 Data Symbols (4.1.1.2.2#2)
    d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5,4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
    e. A DLE symbol (FEh)
    f. An ETX symbol (40h)
4. For each AT Command:
    a. Parse the STX Symbol and verify that:
        i. Bits [7:6] (*StartAT*) are 00b (4.1.1.2.2#8)
        ii. Bit 5 is reserved (0b) (1.7#5)
        iii. Bit 4 (*Responder*) is 0b (4.1.1.2.2#7)
        iv. Bit 3 (*Bounce*) is set to 0b (4.1.1.2.2#6)
        v. Bit 2 (*Recipient*) is 1b (4.1.1.2.2#5)
        vi. Bit 1 (*ReturnBounce*) is set to 0b (4.1.1.2.2#4)

b. Parse the Data Symbols and verify that: (4.1.1.3.1#1)
    i. The REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 127 to 255
    ii. The LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
    iii. If WnR=0, there is no COMMAND_DATA
    iv. If WnR=1b, the COMMAND_DATA is the same length as in the LEN field

5. For each AT Response:
    a. Parse the STX Symbol and verify that:
        i. Bits [7:6] (*StartAT*) are 00b (4.1.1.2.2#8)
        ii. Bit 5 is reserved (0b) (1.7#5)
        iii. Bit 4 (*Responder*) is 0b (4.1.1.2.2#7)
        iv. Bit 3 (*Bounce*) is set to 0b (4.1.1.2.2#6)
        v. Bit 2 (*Recipient*) is 1b (4.1.1.2.2#5)
        vi. Bit 1 (*ReturnBounce*) is set to 0b (4.1.1.2.2#4)
    b. Parse the Data Symbols and verify that: (4.1.1.3.1#2)
        i. A REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 127 to 255
        ii. A LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
        iii. If WnR=0b, RESPONSE_DATA is the same length as in the LEN field (unless test specifies otherwise)
        iv. If WnR=1n, RESPONSE_DATA is 00h (unless test specified otherwise)
    c. Verify that the value in the LEN field is not greater than 64 (4.1.1.3.1#2)

6. When the PUT receives an AT Command with the Recipient bit set to 1b, verify that the PUT responds with an AT Response (unless the test specifies otherwise). (4.1.1.2.2#9)
7. Parse each Broadcast RT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.3.1#1)
    a. A DLE symbol (FEh)
    b. A STX symbol
    c. Two Link Parameters symbols
    d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5,4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
    e. A DLE symbol (FEh)
    f. An ETX symbol (40h)

8. Parse the STX Symbol for a Broadcast RT Transaction and verify that:
    a. *Index* = 0 (4.1.1.2.3.1#4)
    b. *CmdNotResp*=1b (4.1.1.2.3.1#5)

9. Parse Byte 2 of a Broadcast RT Transaction and verify that:
    a. Bits [7:5] are 0 (reserved) (1.7#5)
    b. Bit 4 (*TBTCompatibleSpeed*) is 0b (4.1.1.2.3.1#6)
    c. Bit 1 (reserved) is 0b (1.7#5)
    d. Bit 0 (*USB4*) is 1b (4.1.1.2.3.1#7)

10. Parse each Addressed RT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.3.2#1)
    a. A DLE symbol (FEh)
    b. A STX symbol
    c. No more than 66 Data Symbols (4.1.1.2.3.2#2)
    d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5,4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
    e. A DLE symbol (FEh)
    f. An ETX symbol (40h)

11. Parse each RT Command and verify that: (4.1.1.3.1#1)
    a. The REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 127 to 255
    b. The LEN symbol does not contain a value greater than 64
    c. If WnR=0, there is no COMMAND_DATA
    d. If WnR=1b, the COMMAND_DATA is the same length as in the LEN field
12. Parse each RT Response and verify that: (4.1.1.3.1#2)
    a. The REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 127 to 255
    b. The LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
    c. If WnR=0b, RESPONSE_DATA is the same length as in the LEN field (unless test specifies otherwise)
    d. If WnR=1n, RESPONSE_DATA is 00h (unless test specified otherwise)
13. Verify that the PUT sends an AT Response within tCmdResponse (50ms) of receiving an AT Command. (4.1.1.2.5.1#1)
14. Verify that the PUT sends an Addressed RT Response within tCmdResponse (50ms) of receiving an Addressed RT Command. (4.1.1.2.5.2#1)

Transaction Tests

TD 4.1 Invalid Index Test

A. Purpose

- Verify that the PUT ignores an Addressed RT Command with an Invalid Index

B. Asserts:

- 4.1.1.2.3.2#9
- 4.1.1.3.2#7rt

C. Test Setups

- H1 (Host)
- D1 (Device)
- D3 (Hub UFP)
- D5 (Hub DFP)

D. Procedure:

USB4 CV performs the following steps:

1. Start Analyzer
2. Reset UUT
3. Enumerate UUT Router
4. Initiate Lane Bonding
5. Tell the Link Partner to send an Addressed RT Transaction to the PUT with the following:
    a. Read Command
    b. *Index* = 7
    c. *Target* = Register 9 (Metadata)
    d. *Length* = 4
6. Wait for the Transaction to timeout
7. Verify that the PUT did not send a Read Response (4.1.1.2.3.2#9, 4.1.1.3.2#7rt)
8. Tell the Link Partner to send an Addressed RT Transaction to the PUT with the following:
    a. Write Command
    b. *Index* = 7
    c. *Target* = Register 9 (Metadata)
    d. *Length* = 4
    e. *Command Data* = FFFF FFFFh
9. Wait for the Transaction to timeout
10. Verify that the PUT did not send a Write Response (4.1.1.2.3.2#9, 4.1.1.3.2#7rt)
11. Tell the Link Partner to send the PUT an Addressed RT Transaction with the following:
    a. Read Command
    b. *Index* = index of PUT
    c. *Target* = Register 9 (Metadata)
    d. *Length* = 4
12. Wait for the Read Response from the PUT
13. Verify that the previous Read and Write Commands had no effect (i.e. the contents of Register 9 are 0 (default value))
14. Stop Analyzer

TD 4.2 FEh Data Symbol Test

A. Purpose:

- Verify that the PUT correctly handles Transactions with FEh data symbols

B. Asserts:

- 4.1.1.2.4#3, 4.1.1.2.4#4

C. Test Setups

- H1 (Host)
- D1 (Device)
- D3 (Hub UFP)
- D5 (Hub DFP)

D. Repetitions:

- Repeat with AT Transactions
- Repeat with Addressed RT Transactions with the following:
  - *Index* = 0
  - *Index* = First On-Board Re-timer (if present)
  - *Index* = Second On-Board Re-timer (if present)

E. Procedure:

USB4 CV performs the following steps:

1. Start Analyzer
2. Reset UUT
3. Enumerate UUT Router
4. Initiate Lane Bonding
5. Tell the Link Partner to send the PUT a Write Command with the following:
   a. *Target* = Register 9 (Metadata)
   b. *Length* = 4
   c. *Command Data* = FE 00 FE 00h
   d. Insert a leading FEh before each FEh data symbol
6. Verify that the PUT sends a Write Response with no error (4.1.1.2.4#4)
7. Tell the Link Partner to send the PUT a Read Command with the following:
   a. *Target* = Register 9 (Metadata)
   b. *Length* = 4
8. Wait for the AT Read Response from the PUT
9. Verify that the contents of Register 9 are the same as previously written (FE 00 FE 00h) (4.1.1.2.4#3)
10. Stop Analyzer

TD 4.3 SB Register Write Error Test

A. Purpose:

- Verify that the PUT correctly handles Write Request error cases

B. Asserts:

- 4.1.1.3.1#12-16
- 4.1.1.3.3#1

C. Test Setups

- H1 (Host)
- D1 (Device)
- D3 (Hub UFP)
- D5 (Hub DFP)

D. Repetitions:

- Repeat with AT Transactions
- Repeat with Addressed RT Transactions with the following:
  - *Index* = 0
  - *Index* = First On-Board Re-timer (if present)
  - *Index* = Second On-Board Re-timer (if present)

E. Procedure:

USB4 CV does the following:

Part 0 - Setup

1. Start Analyzer
2. Reset UUT
3. Enumerate UUT Router
4. Initiate Lane Bonding

Part 1 – Invalid Target

5. Tell the Link Partner to send the PUT a Write Command that targets an undefined register
6. Verify that the PUT responds with a Write Response with:
   a. LEN = 0
   b. RESPONSE_DATA = 01h (error Result Code) (4.1.1.3.1#12)

Part 2 – Write Length Mismatch

7. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 9 (Metadata)
8. Record the RESPONSE_DATA returned by the PUT
9. Tell the Link Partner to send the PUT a Write Command with:
   a. *Target* = Register 9 (Metadata)
   b. COMMAND_DATA is 8 bytes
   c. LEN = 9
10. Verify that the PUT responds with a Write Response with:
    a. LEN = 0 (4.1.1.3.1#13)
    b. RESPONSE_DATA = 01h (error Result Code) (4.1.1.3.1#13)
11. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 9 (Metadata)

12. Verify that the RESPONSE_DATA in the Read Response from the PUT is the same as the RESPONSE_DATA recorded in Step 4 (4.1.1.3.1#13)

Part 3 – Write to Read-Only Register

13. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 0 (Vendor ID)
14. Record the RESPONSE_DATA returned by the PUT
15. Tell the Link Partner to send the PUT a Write Command with *Target* = Register 0 (Vendor ID)
16. Verify that the PUT responds with a Write Response with:
    a. LEN = 0 (4.1.1.3.1#14)
    b. RESPONSE_DATA = 01h (error Result Code) (4.1.1.3.1#14)
17. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 0 (Vendor ID)
18. Verify that the RESPONSE_DATA in the Read Response from the PUT is the same as the RESPONSE_DATA recorded in Step 10 (4.1.1.3.3#1)

Part 4 – Long Write

19. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 9 (Metadata)
20. Record the RESPONSE_DATA returned by the PUT
21. Tell the Link Partner to send the PUT a Write Command with:
    a. *Target* = Register 9 (Metadata)
    b. LEN = 5
22. Verify that the PUT responds with a Write Response with:
    a. LEN = 0 (4.1.1.3.1#15)
    b. RESPONSE_DATA = 01h (error Result Code) (4.1.1.3.1#15)
23. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 9 (Metadata)
24. Verify that the RESPONSE_DATA in the Read Response from the PUT is the same as the RESPONSE_DATA recorded in Step 16 (4.1.1.3.1#15)

Part 5 – Short Write

25. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 9 (Metadata)
26. Record the RESPONSE_DATA returned by the PUT
27. Tell the Link Partner to send the PUT a Write Command with:
    a. *Target* = Register 9 (Metadata)
    b. LEN = 3
    c. COMMAND_DATA = FF FF FFh
28. Verify that the PUT responds with a Write Response with:
    a. LEN = 4 (4.1.1.3.1#16)
    b. RESPONSE_DATA = 00h (Success Result Code) (4.1.1.3.1#16)
29. Tell the Link Partner to send the PUT a Read Command with *Target* = Register 9 (Metadata)
30. Verify that the RESPONSE_DATA in the Read Response from the PUT is the same as the RESPONSE_DATA recorded in Step 22 (4.1.1.3.1#16)
31. Stop Analyzer

TD 4.4 Command Timeout Test

A. Purpose:

- Verify that the PUT records a Transaction timeout in SB Register Space
- Verify that the PUT waits tATTimeout before timing out an AT Command
- Verify that the PUT only sends one AT Command or Addressed RT Command at a time

B. Asserts:

- 4.1.1.2.5#3
- 4.1.1.2.5.1#3
- 4.1.1.2.5.2#2
- 4.1.1.3.2#20-22, 4.1.1.3.2#24

C. Test Setups

- H1 (Host)
- D1 (Device)
- D3 (Hub UFP)
- D5 (Hub DFP)

D. Repetitions:

- Repeat with AT Transactions that target the Link Partner (*Target* = 001b)
- Repeat with Addressed RT Transactions with invalid index (*Target* = 010b, *Index* = 7)

E. Procedure:

USB4 does the following:

Part 0 - Setup

1. Start Analyzer
2. Reset UUT
3. Enumerate UUT Router
4. Initiate Lane Bonding
5. Configure KG Host/Device to not respond to any Commands

Part 1 – Write Command

6. Initiate a Write Command by writing the following to the USB4 Port Capability in PUT Configuration Space:
    a. *Target* = see repetitions
    b. *Address* = Register 9 (Metadata)
    c. *Length* = 4
    d. *WnR* = 1 (Write)
    e. *Data* DW = FFFF FFFFh
7. Set the *Pending* bit in the USB4 Port Capability in PUT Configuration Space to 1b
8. Wait 1 second.
9. Verify that the PUT sets the *Pending* bit to 0b (4.1.1.3.2#24)

10. Read the following fields from the USB4 Port Capability in PUT Configuration Space:
    a. *Length*
    b. *No Response*
    c. *Result Code*
11. Verify that:
    a. *Length* = 4 (4.1.1.3.2#20)
    b. *No Response* = 0 (4.1.1.3.2#21)
    c. *Result Code* = 1 (error) (4.1.1.3.2#22)

Part 2 – Parse Analyzer Trace

12. Read the trace file from the Analyzer
13. Parse the trace file and verify the following:
    a. PUT did not resend the Read Command or send another AT Command or Addressed RT Command until after the Read Command timed out (4.1.1.2.5#3)
    a. If Read Command is an AT Command, timeout = tATTimeout (4.1.1.2.5.1#3)
    b. If Read Command is an Addressed RT Command, timeout = tRTTimeout (4.1.1.2.5.2#2)
14. Stop Analyzer

Lane Initialization Tests

Note: The tests in this section are performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.

TD 4.5 Lane Initialization Phase Test

A. Purpose:

- Verify that the PUT behaves correctly during Lane Initialization
- Verify that SB Register Space format, fields, and values are correct
- Verify maximum sized read (64 bytes) from SB Register space

B. Asserts:

- 4.1.1.2.3.1#4, 4.1.1.2.3.1#8-9
- 4.1.1.3.1#1rt, 4.1.1.3.1#2rt, 4.1.1.3.1#5rt
- 4.1.1.3.3#6, 4.1.1.3.3#8-13, 4.1.1.3.3#13-15, 4.1.1.3.3#18-27
- 4.1.2.2#2
- 4.1.2.3#1-2, 4.1.2.3#4-8, 4.1.2.3#11, 4.1.2.3#14, 4.1.2.3#17
- 4.1.2.4#1-5
- 4.1.2.5#2, 4.1.2.5#4, 4.1.2.5#5
- 4.1.2.5#2rt, 4.1.2.5#3rt, 4.1.2.5#7rt-9rt
- 4.1.2.5.1.1#2-7
- 4.1.2.5.1.2#2, 4.1.2.5.1.2#3, 4.1.2.5.1.2#5-7, 4.1.2.5.1.2#9-12
- 4.2.1.4.1#1
- 4.2.2.2#1, 4.2.2.2#3-5

C. Test Setups

- H1 (Host)
- D1 (Device)
- D3 (Hub UFP)
- D5 (Hub DFP)

D. Repetitions:

- Repeat at all supported Link Configurations:
  - For 20G: Gen 2x1, Gen 2x2
  - For 40G: Gen 2x1, Gen 2x2, Gen 3x1, Gen 3x2
- Repeat with:
  - RS-FEC on (Configurations A, D)
  - RS-FEC off (Configurations B, C, E, F, G)

E. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Start Analyzer
2. Reset UUT
3. Enumerate UUT Router
4. Set the Link speed in the PUT and Link Partner:
   a. For Gen 2x2:
      i. *Target Link Speed* = Gen 2
      ii. *Lane Disable (Lane 0)* = 0b
      iii. *Lane Disable (Lane 1)* = 0b

b. For Gen 3x1:
    i. *Target Link Speed* = Gen 3
    ii. *Lane Disable (Lane 0)* = 0b
    iii. *Lane Disable (Lane 1)* = 1b
c. For Gen 3x2:
    i. *Target Link Speed* = Gen 3
    ii. *Lane Disable (Lane 0)* = 0b
    iii. *Lane Disable (Lane 1)* = 0b

5. Set RS-FEC on/off in the PUT and Link Partner:
    a. Gen 2 – RS-FEC is on (Configuration A)
        i. *Request RS-FEC Gen 2* = 1b in DFP
    b. Gen 2 – RS-FEC is off (Configuration B)
        i. *Request RS-FEC Gen 2* = 0b in DFP
    c. Gen 3 – RS-FEC is on (Configuration C)
        i. *Request RS-FEC Gen 3* = 1b in DFP
    d. Gen 3 – RS-FEC is off (Configuration D)
        i. *Request RS-FEC Gen 3* = 0b in DFP

Part 1 – Phases 1 and 2

6. Disconnect then connect the PUT by performing a Downstream Port Reset (DPR)
    a. If the PUT is a UFP, perform the DPR on the DFP connected to the PUT
    b. If the PUT is a DFP, perform the DPR on the PUT
7. Verify that SBTX goes high on the UUT for at least tConnectRx time

Part 2 – Phase 3

8. Verify that the PUT sends one or more AT Transactions to read the Link Configuration Register (Register 12) of the Link Partner (4.1.2.3#1)
9. Verify that the PUT avoids a tATTimeout delay by sending one or more additional AT Transactions (4.1.2.3#2)

Part 3 – Phase 4

10. Verify that the PUT sends a Broadcast RT Transaction every tLaneParams (4.1.2.4#1, 4.1.1.3.1#2rt)
11. Record the value in the Re-timer Index field of the Broadcast Transaction

    Note: The Re-Timer Index is 0 when a Router first creates and sends a Broadcast Transaction. It is then is incremented by 1 by each re-timer on the Link. The number of On-Board Re-timers on the PUT is equal to the Re-timer Index field minus the number of any additional Cable Re-timers and On-Board Re-timers the Broadcast RT Transaction traverses before being captured.

12. Verify that the Re-timer Index indicates the correct number of On Board Re-timers on the PUT, as indicated in the USB4_Num_Retimers field in the VIF (4.1.1.2.3.1#4, 4.1.1.3.1#1rt)
13. Verify that the PUT sends Broadcast RT Transactions until all of the following are true: (4.1.2.4#2)
    a. At least tLTPhase4 time has passed from completion of Phase 2
    b. The PUT sent at least two Broadcast RT Transactions

14. For each Broadcast RT Transaction from the PUT, verify: (4.1.2.4#1)
    a. *TBT3-Compatible Speed* = 0b
    b. If Link is configured with RS-FEC encoding on, *RS_FEC* = 1b
    c. If Link is configured with RS-FEC encoding off, *RS_FEC* = 0b
    d. *USB4* bit = 1b
    e. If Link is configured for Gen 2 speed, *Selected Gen* = 0001b
    f. If Link is configured for Gen 3 speed, *Selected Gen* = 0010b
    g. Bits [3:2] (Reserved) are 0 (1.7#5)
    h. If Link is configured for x1, *Lane1Enabled* = 0b (4.1.1.2.3.1#8)
    i. If Link is configured for x2, *Lane1Enabled* = 1b (4.1.1.2.3.1#8)
    j. *Lane0Enabled* = 1b (4.1.1.2.3.1#9)
    k. If PUT has On-Board Re-timers, *SSCAlwaysOn* is 0b (4.1.1.3.1#5rt)
15. Verify that the PUT sends SLOS1 (4.1.2.4#3)
16. Verify that the PUT sends an LT_Resume Transaction with *LSELan*e field = 0b (4.1.2.4#4, 4.1.2.4#5)
17. If Link is configured for x2, verify that the PUT sends an LT_Resume Transaction with *LSELan*e field = 1b (4.1.2.4#4, 4.1.2.4#5)
18. Send the PUT an Addressed RT Transaction with:
    a. Read Command
    b. *Index* = 0
    c. *Target* = Register 13 (TxFFE)
19. In the Read Response from the PUT parse the RESPONSE_DATA and verify that:
    a. *Tx Active (Lane 0)* = 1b (4.1.2.4#4)
    b. If Link is configured for x1, *Tx Active (Lane 1)* = 0b (4.1.2.4#4)
    c. If Link is configured for x2, *Tx Active (Lane 1)* = 1b (4.1.2.4#4)
    d. *Clock Switch Done* = 0b (4.1.2.5#7rt)

Part 4 – Phase 5

Note: The first two steps in Part 4 (Step 20 and Step 21) are performed simultaneously

20. To test the PUT Transmitter:
    a. Verify that the PUT sends an Addressed RT Transaction with:
        i. Read Command (4.1.2.5#2, 4.1.2.5#2rt)
        ii. *Target* = Rx Status & TxFFE Request byte (4.1.2.5.1.1#2)
        iii. *Index* = 0b (4.1.2.5#2)
    b. If the *New Request* bit in the receiver is 0b:
        a. Verify that the PUT resends a second Read Command within tPollTXFFE of receiving the Read Response (4.1.2.5.1.1#3)
        b. Wait for the *New Request* bit to be 1b
    c. Read the Tx Status byte of the PUT and verify:
        i. TxFFE Setting matches the receiver setting in the Read Response (4.1.2.5.1.1#4)
        ii. Request Done = 1b (4.1.2.5.1.1#5)
    d. Verify that the PUT sends a Read Command to read the Rx Status & TxFFE Request byte (4.1.2.5.1.1#6)
    e. Verify that the PUT resends the Read Command within tPollTXFFE of receiving the Response (4.1.2.5.1.1#7)
    f. Verify that the PUT sends a Read Command to read the Rx Status & TxFFE Request byte (4.1.2.5.1.1#6)
    g. Wait for the *Request Done* bit in the TX Status byte of the PUT to be 0b.
    h. Verify that the PUT does not send any more Read Commands targeting the Rx Status & TxFFE Request byte (4.1.2.5.1.1#7)

i. If the PUT has On-Board Re-timers, verify that it sends CL_WAKE1.X Ordered Set Symbols after *Rx Active* is 1b. (4.1.2.5#3rt)
j. Set the *Clock Switch Done* bit to 1b.

21. To test the PUT Receiver:
    a. Verify that the PUT sends an Addressed RT Transaction with:
        i. Read Command (4.1.2.5#4)
        ii. *Target* = TxFFE register (4.1.2.5.1.2#2)
        iii. *Index* = 0b (4.1.2.5#4)
    b. Send a Read Response
    c. If the *Tx Active* bit is 0b:
        a. Verify that the PUT resends the Read Command within tPollTXFFE of receiving the Response (4.1.2.5.1.2#3)
        b. Wait for the *Tx Active* bit to be 1b
    d. Verify that the PUT sends a Read Command targeting the TX Status byte (4.1.2.5.1.2#7)
    e. Verify that the PUT sends a Read Request targeting the TX Status byte within tPollTXFFE of receiving the Read Response (4.1.2.5.1.2#9)
    f. Verify that the PUT sends a Read Command targeting the TX Status Register (4.1.2.5.1.2#12)
22. If PUT contains two On-Board Re-timers:
    a. When the PUT stops sending CL_WAKE1.X:
        i. Read the *Clock Switch Done* bit and verify that it is 1b (4.1.2.5#8rt)
        ii. Verify that the PUT sends CL_WAKE1.(X+1)
        iii. When the PUT stops sending CL_WAKE1.(X+1), verify that it sends SLOS
23. If PUT contains one On-Board Re-timer:
    a. When the PUT stops sending CL_WAKE1.X:
        i. Read the *Clock Switch Done* bit and verify that it is 1b (4.1.2.5#8rt)
        ii. Verify that the PUT sends SLOS
24. If PUT does not contain On-Board Re-timers, wait for PUTs to reach CL0 state.

Part 5 – SB Register Space Verification

25. Read the SB Registers Spaces of the PUT:
    a. Send AT Transactions to read all defined registers in the SB Register Space of the PUT
    b. Send Addressed RT Transactions to read all defined registers in the SB Register Space of all On-Board Re-timer Ports
26. Verify the following for each SB Register Space:
    a. For Register 0 (Vendor ID):
        i. Vendor ID Low field matches the Vendor ID field in Router Configuration Space (4.1.1.3.3#8)
        ii. Vendor ID High field matches the Vendor ID field in Router Configuration Space (4.1.1.3.3#9)
        iii. Bytes 2 and 3 are 0 (4.1.1.3.3#6)
    b. For Register 1 (Device ID):
        i. Verify that the Device ID Low field matches the Device ID field in Router Configuration Space (4.1.1.3.3#10)
        ii. Verify that the Device ID High field matches the Device ID field in Router Configuration Space (4.1.1.3.3#11)
        iii. Verify that bytes 2 and 3 are 0. (4.1.1.3.3#6)

c. For Register 8 (Opcode):
    i. All bits are 0 (default value) (4.1.1.3.3#6)
d. For Register 9 (Metadata):
    i. All bits are 0 (default value) (4.1.1.3.3#6)
e. For Register 12 (Link Configuration):
    i. Bits 2 through 7 of byte 0 are 0 (reserved) (4.1.1.3.3#6)
    ii. *Enabling Request* (Lane 1) is 0b if x1 Link (4.1.1.3.3#18)
    iii. Bits 2 and 3 in byte 1 are 0 (reserved) (4.1.1.3.3#6)
    iv. *Enabling Decision (Lane 0)* is 1b (4.1.2.3#4, 4.1.1.3.3#13)
    v. *Enabling Decision (Lane 1)* is 1b if Link is x2 (4.1.2.3#4, 4.1.1.3.3#14)
    vi. *Enabling Decision (Lane 1)* is 0b if Link is x1 (4.1.2.3#6)
    vii. *Gen 3 Support* bit is 1b if all of the following are true: (4.1.1.3.3#19)
        a. On-Board Re-timers connected between the PUT and the cable support Gen 3 speeds (USB4_Max_Speed field in VIF is Gen 3)
        b. The *Target Link Speed* field in the Lane Adapter Configuration Capability is 1100b (Gen 3)
    viii. *Gen 3 Support* bit is 0b if any of the following are true: (4.1.1.3.3#20)
        a. On-Board Re-timers connected between the PUT and the cable do not support Gen 3 speeds (USB4_Max_Speed field in VIF is Gen 2)
        b. The *Target Link Speed* field in the Lane Adapter Configuration Capability is 1000b (Gen 2)
    ix. *RS-FEC Request (Gen 2)* bit is the same as the *Request RS-FEC Gen 2* bit in the USB4 Port Capability of the PUT (4.1.1.3.3#21)
    x. *RS-FEC Request (Gen 3)* bit is the same as the *Request RS-FEC Gen 3* bit in the USB4 Port Capability of the PUT (4.1.1.3.3#22)
    xi. *USB4 Sideband Channel* field is 1b (4.1.1.3.3#23)
    xii. *TBT3-compatible Speeds Supported* bit is 0b if PUT does not support TBT3-compatible speeds (USB4_TBT3_Compatibility_Supported field in VIF is NO) (4.1.1.3.3#24)
    xiii. Bits 2 through 7 in byte 2 are 0 (reserved) (4.1.1.3.3#6)
f. For Register 13 (TXFFE):
    i. *Clock Switch Done (Lane 0)* bit is 1 (4.1.1.3.3#26, 4.1.2.5#5, 4.1.2.5#9rt)
    ii. Bits 4 and 5 in byte 2 are 0 (reserved) (4.1.1.3.3#6)
    iii. Bits 4 and 5 in byte 3 are 0 (reserved) (4.1.1.3.3#6)
    iv. If x1 Link, the *Clock Switch Done (Lane 1)* bit is 0 (4.1.1.3.3#27, 4.1.2.5#5, 4.1.2.5#9rt)
    v. If x2 Link, the *Clock Switch Done (Lane 1)* bit is 1 (4.1.1.3.3#27, 4.1.2.5#5, 4.1.2.5#9rt)
g. For Register 18:
    i. All bits are 0 (default value) (4.1.1.3.3#6)

Part 6 – Bonding

27. Wait for a Hot Plug Event Packet with UPG=0b from the PUT
28. Enumerate the UUT Router
29. Set the *Lane Bonding* bit to 1b in the Adapter Configuration Space of Lane 0
30. Verify that the PUT puts 001b in the *Lane Bonding Target* field of all TS1 and TS2 Ordered Sets (4.2.2.2#1)
31. Verify that the *Adapter State* field in the USB4 Adapter Configuration Capability of the Lane 0 Adapter is set to CL0 (4.2.2.2#3)
32. Verify that the PUT sends a Hot Unplug Event Packet for the Lane 1 Adapter (4.2.2.2#5)

Part 7 – Configuration Space Verification

33. Read the *Adapter State* field of the Lane 0 Adapter
34. Verify that the Lane 0 Adapter is in CL0 state (4.2.1.4.1#1)
35. Read the *Adapter State* field of the Lane 1 Adapter:
    a. If Link is x2, verify that state is CL0 (4.2.1.4.1#1)
    b. If Link is x1, verify that state is CLd (4.1.2.3#5)
36. Read the USB4 Adapter Configuration Capability of the Lane 0 Adapter and verify:
    a. *Current Link Speed* field is set to Gen 3 if Link is Gen 3 speed (4.1.2.3#11)
    b. *Current Link Speed* field is set to Gen 2 if Link is Gen 2 speed (4.1.2.3#11)
    c. *Negotiated Link Width* field in Lane 0 Adapter is x2 if Link is x2 (4.2.2.2#4)
    d. *Negotiated Link Width* field in Lane 0 Adapter is x1 if Link is x1
37. Read the USB4 Port Capability of the PUT and verify:
    a. *Bonding Enabled* is 1b for a x2 Link (4.1.2.3#7)
    b. *Bonding Enabled* is 0b for a x1 Link (4.1.2.3#8)
    c. *TBT3-Compatible Speed Used* bit is set to 0b
    d. If speed is Gen 2 and RS-FEC is on, *RS-FEC Enabled (Gen 2)* bit is 1b (4.1.2.3#14)
    e. If speed is Gen 2 and RS-FEC is off, *RS-FEC Enabled (Gen 2)* bit is 0b (4.1.2.3#14)
    f. If speed is Gen 3 and RS-FEC is on, *RS-FEC Enabled (Gen 3)* bit is 1b (4.1.2.3#17)
    g. If speed is Gen 3 and RS-FEC is off, *RS-FEC Enabled (Gen 3)* bit is 0b (4.1.2.3#17)
38. Stop Analyzer

Adapter State Tests

Unless noted otherwise, the tests in this section are performed at Gen 2 speed and repeated at Gen 3 speed (if Gen 3 speed is supported).

Note: The tests in this section are performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.

TD 4.6 DFP Lane Disable/Enable Test (DFP Only)

Note: This test is only performed on DFP

A. Purpose:
- Verify that DFP transitions into Disabled state correctly after being disabled
- Verify that DFP exits Disabled state correctly after being enabled

B. Asserts:
- 4.2.1.1.1#1, 4.2.1.1.1#2
- 4.2.1.2.2#2
- 4.2.1.3.3#5
- 4.2.2.4#1
- 4.4.6.2.1#1, 4.4.6.2.1#2

C. Test Setups
- H1 (Host)
- D5 (Hub)

D. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Start Analyzer
2. Reset UUT
3. Enumerate UUT Router
4. Set the following fields in the Adapter Configuration Space of both Lane Adapters:
   a. *Link Credits Allocated* = 2
   b. *Inter-Domain Slave* = 1b
   c. *Target Link Width* = 0000 11b
   d. *CL0s Enable* = 1b
   e. *CL1 Enable* = 1b
   f. *CL2 Enable* = 1b
   g. *Lane Bonding* = 1b

Part 1 – Lane 1 Adapter Disabled then Enabled

5. Set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 1b
6. Verify that the PUT sent an LT_Fall Transaction for Lane 1 (4.4.6.2.1#1)
7. Verify that the PUT sends a Hot Plug Event packet with UPG = 1b for the Lane 1 Adapter (4.4.6.2.1#2)
8. Read the *Plugged* bit in Adapter Configuration Space of the Lane 1 Adapter
9. Verify that the *Plugged* bit is 0b for the Lane 1 Adapter (4.2.1.1.1#2)
10. Read the Adapter State of Lane 1 and Lane 0
11. Verify that the Lane 1 Adapter is in the Disabled state (4.2.1.1.1#1)
12. Verify that the Lane 0 Adapter is in CL0 state (4.2.2.4#1)

13. Set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 0b
14. Reset the PUT
15. Verify that the PUT sends a Hot Plug Event Packet for the Lane 1 Adapter (4.2.1.3.3#5)
16. Verify that the Lane 0 Adapter and the Lane 1 Adapter are both in the CL0 state

Part 2 – Both Lanes Disabled, then Enabled

17. Set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 1b
18. Wait for a Hot Plug Event packet with UPG = 1b for the Lane 1 Adapter
19. Set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 0 Adapter to 1b
20. Verify that the PUT sent an LT_Fall Transaction (4.4.6.2.1#1)
21. Verify that the PUT sends a Hot Plug Event Packet with UPG = 1b for the Lane 1 Adapter (4.4.6.2.1#2)
22. Read the *Plugged* bit in Adapter Configuration Space of the Lane 0 Adapter
23. Verify that the *Plugged* bit is 0b for the Lane 0 Adapter (4.2.1.1.1#2)
24. Read the Adapter State of Lane 1 and Lane 0
25. Verify that the Lane 1 Adapter is in the Disabled state (4.2.1.1.1#1, 4.4.6.2.1#3)
26. Verify that the Lane 0 Adapter is in the Disabled state (4.2.1.1.1#1, 4.4.6.2.1#3)
27. Set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 0 Adapter to 0b
28. Reset the PUT
29. Verify that the PUT sends a Hot Plug Event Packet for the Lane 0 Adapter (4.2.1.3.3#5)
30. Verify that the Lane 0 Adapter is in the CL0 state
31. Set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 0b
32. Reset the PUT
33. Verify that the PUT sends a Hot Plug Event Packet for the Lane 1 Adapter (4.2.1.3.3#5)
34. Verify that the Lane 0 Adapter and the Lane 1 Adapter are both in the CL0 state

Part 3 – Configuration Space Validation

35. Read the Adapter Configuration space of each Adapter and verify that the following fields have default values (4.4.6.2.1#3)
    a. *Link Credits Allocated* = 0
    b. *Inter-Domain Slave* = 0b
    c. *Target Link Width* = 000 01b
    d. *CL0s Enable* = 0b
    e. *CL1 Enable* = 0b
    f. *CL2 Enable* = 0b
    g. *Lane Bonding* = 0b
36. Stop Analyzer

TD 4.7 UFP Lane Disable/Enable Test (UFP Only)

Note: This test is only performed on the UFP.

A. Purpose:
- Verify that UFP Adapters transition into Disabled state correctly when Link Partner is disabled
- Verify that UFP Adapters exit Disabled state correctly when Link Partner is enabled

B. Asserts:
- 4.2.1.2.2#5, 4.2.1.2.2#7
- 4.4.6.2.1.1#1-3
- 4.4.6.2.1.2#1, 4.4.6.2.1.2#2, 4.4.6.2.1.2#4

C. Test Setups
- D1 (Device)
- D3 (Hub)

D. Procedure:

USB4 Does the following:

Part 0 – Setup

1. Start Analyzer
2. Reset UUT
3. Enumerate UUT Router
4. Initiate Lane Bonding
5. Set the following fields:
   a. *Link Credits Allocated* = 2
   b. *Inter-Domain Slave* = 1b
   c. *Target Link Width* = 0000 11b
   d. *CL0s Enable* = 1b
   e. *CL1 Enable* = 1b
   f. *CL2 Enable* = 1b
   g. *Lane Bonding* = 1b

Part 1 – Lane 1 is Disabled, then Enabled

6. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 1b
7. Wait 1 second
8. Verify that the PUT is in the CLd state (4.4.6.2.1.1#3)
9. Wait 1 second
10. Verify that the PUT does not start Lane Initialization (4.2.1.2.2#7)
11. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 0b
12. Verify that the PUT does not start Lane Initialization on Lane 1 until it receives a Broadcast RT Transaction with the *Lane1Enabled* bit set to 1b (4.2.1.2.2#7)
13. Verify that:
    a. PUT starts Lane Initialization on Lane 1 (4.2.1.2.2#5)
    b. Lane Initialization starts from Phase 4 (4.2.1.2.2#5)
    c. PUT retained state from Phase 1-3 of previous Link Initialization (4.2.1.2.2#5)

Part 2 – Both Lanes are Disabled, then Enabled

14. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 1b
15. Wait 1 second
16. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 0 Adapter to 1b
17. Verify that the PUT Drives SBTX to logical low for a minimum of tDisconnectTx (4.4.6.2.1.2#1)

    Note: Lane 0 is enabled as part of disconnect flow

18. Verify that the PUT does not start Lane Initialization on Lane 0 until it receives a Broadcast RT Transaction with the *Lane0Enabled* bit set to 1b (4.2.1.2.2#6)
19. Verify that the PUT does not start Lane Initialization on Lane 1 until it receives a Broadcast RT Transaction with the *Lane1Enabled* bit set to 1b (4.2.1.2.2#7)
20. Verify that the PUT starts Lane Initialization from Phase 1 (4.4.6.2.1.2#4)
21. Wait for Lane Initialization to finish

Part 3 – Configuration Space Verification

22. Verify that the PUT sent at least one Hot Plug Event Packet with UPG=1 for Lane 1 (4.4.6.2.1.1#1)

    Note: PUT can either send one Hot Plug Event Packet (UPG=1) or three Hot Plug Event Packets (UPG=1; UPG=0; UPG=1)

23. Verify that the PUT sent a Hot Plug Event Packet with UPG=1 for Lane 0 (4.4.6.2.1.1#1)
24. Verify that the PUT sent a Hot Plug Event Packet with UPG=0 for Lane 0
25. Verify that the PUT sent a Hot Plug Event Packet with UPG=0 for Lane 1
26. Read the Adapter Configuration space of the Lane 0 Adapter and Lane 1 Adapter and verify that the following fields have default values (4.4.6.2.1.2#2)
    a. *Link Credits Allocated* = 0
    b. *Inter-Domain Slave* = 0b
    c. *Target Link Width* = 000 01b
    d. *CL0s Enable* = 0b
    e. *CL1 Enable* = 0b
    f. *CL2 Enable* = 0b
    g. *Lane Bonding* = 0b
27. Stop Analyzer

TD 4.8 Inter-Domain Disable/Enable

Note: This test is only performed on DFP.

A. Purpose:
- Verify that DFP Adapters transition into Disabled state correctly when Link Partner (DFP) is disabled
- Verify that DFP Adapters exit Disabled state correctly when Link Partner is enabled

B. Asserts:
- 4.2.1.2.1#5
- 4.2.1.4.3#4

C. Test Setups
- H1 (Host)
- D5 (Hub)

D. Procedure:

USB4 does the following:

Part 0 – Setup

1. Start Analyzer
2. Reset UUT
3. Enumerate UUT Router
4. Set the following fields:
   a. *Link Credits Allocated* = 2
   b. *Inter-Domain Slave* = 1b
   c. *Target Link Width* = 0000 11b
   d. *CL0s Enable* = 1b
   e. *CL1 Enable* = 1b
   f. *CL2 Enable* = 1b
   g. *Lane Bonding* = 1b

Part 1 – Lane 1 is Disabled, then Enabled

5. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 1b
6. Wait 1 second
7. Verify that Lane 1 transitions to CLd state (4.2.1.2.1#5, 4.2.1.4.3#4)
8. Wait 1 second
9. Verify that the PUT does not start Lane Initialization (4.2.1.2.2#7)
10. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 0b
11. Verify that the PUT does not start Lane Initialization until it receives a Broadcast RT Transaction with the *Lane1Enabled* bit set to 1b (4.2.1.2.2#7)
12. Verify that:
    a. The PUT starts Lane Initialization on Lane 1 (4.2.1.2.2#5)
    b. Lane Initialization starts from Phase 4 (4.2.1.2.2#5)
    c. The PUT retained state from Phase 1-3 of previous Link Initialization (4.2.1.2.2#5)

Part 2 – Both Lanes are Disabled, then Enabled

13. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 1b
14. Wait 1 second

15. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 0 Adapter to 1b
16. Wait 1 second
17. Verify that the PUT does not start Lane Initialization (4.2.1.2.2#6, 4.2.1.2.2#7)
18. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 0 Adapter to 0b
19. Reset the Link Partner
20. Verify that the PUT doesn't start Lane Initialization on Lane 0 until after it receives a Broadcast RT Transaction with the *Lane0Enabled* bit set to 1b (4.2.1.2.2#6)
21. Verify that Lane Initialization starts from Phase 4 (4.2.1.2.2#5)
22. Verify that the PUT retained state from Phase 1-3 of previous Link Initialization (4.2.1.2.2#5)
23. In the Link Partner of the PUT, set the *Lane Disable* bit in the Adapter Configuration Space of the Lane 1 Adapter to 0b
24. Reset the Link Partner
25. Verify that the PUT doesn't start Lane Initialization on Lane 1 until after it receives a Broadcast RT Transaction with the *Lane1Enabled* bit set to 1b (4.2.1.2.2#7)
26. Verify that Lane Initialization starts from Phase 4 (4.2.1.2.2#5)
27. Verify that the PUT retained state from Phase 1-3 of previous Link Initialization (4.2.1.2.2#5)
28. Stop Analyzer

TD 4.9 Lane Initialization Adapter State Test

A. Purpose:

- Verify that the PUT transitions between states correctly during Lane Initialization

B. Asserts:

- 4.2.1.2.3#2
- 4.2.1.3.2#1, 4.2.1.3.2#2
- 4.2.1.3.3#1, 4.2.1.3.3#6
- 4.2.1.3.4#4-7
- 4.2.1.3.5#3-5 4.2.1.3.5#8 4.2.1.3.5#11
- 4.2.1.4.1#1
- 4.2.1.4.3#8, 4.2.1.4.3#9
- 4.2.1.5.1#1, 4.2.1.5.1#2
- 4.2.1.5.2#1
- 4.2.1.5.3#1
- 4.2.1.5.3#3 4.2.1.5.3#2
- 4.2.1.4.1#2
- 4.2.2.2#2
- 4.2.2.2.1#3
- 4.4.4#3-8

C. Test Setups

- H1 (Host)
- D1 (Device)
- D3 (Hub UFP)
- D5 (Hub DFP)

D. Repetitions:

- Repeat with bonding initiated as follows:
  - Send TS1 OS to PUT
  - Set Lane Bonding bit to 1b in the Lane 0 Adapter
  - Set Lane Bonding bit to 1b in the Lane 1 Adapter

E. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Start Analyzer
2. Reset PUT
3. Start Lane Initialization

Part 1 – Training State

4. Verify that:
   a. PUT starts sending back-to-back SLOS1, which indicates entry to Training.LOCK1 sub-state (4.2.1.2.3#2)
   b. SLOS1 are not scrambled (4.2.1.3.4#4)
   c. PUT does not send any partial SLOS1 (4.2.1.3.4#5, 4.2.1.3.4#6, 4.2.1.3.4#7)

5. Verify that the PUT sends back-to-back SLOS1 until all of the following are true: (4.2.1.3.2#1)
    a. KG Host/Device sent at least 2 SLOS1 symbols to PUT
    b. KG Host/Device received at least 2 complete SLOS1 (if Gen 2 speed) or at least 4 complete SLOS1 (if Gen 3 speed) from PUT
    c. The Rx Locked bit in PUT is 1b (TxFFE negotiation is complete)
6. Verify that:
    a. PUT starts sending back-to-back SLOS2, which indicates entry to Training.LOCK2 sub-state (4.2.1.3.2#1)
    a. SLOS2 are not scrambled (4.2.1.3.4#4)
    b. PUT does not send any partial SLOS2 (4.2.1.3.4#7)
    c. Transition to Training.LOCK2 substate occurs within tTrainingTransmission after receiving the last bit of the last SLOS1 (4.2.1.3.2#2)
7. Verify that the PUT sends back-to-back SLOS2 until all of the following are true: (4.2.1.3.2#1)
    a. KG Host/Device sent at least 2 SLOS symbols
    b. KG Host/Device received at least 2 complete SLOS2 (if Gen 2 speed) or at least 4 complete SLOS2 (if Gen 3 speed) from PUT
8. Verify that the PUT starts sending back-to-back TS1, which indicates entry to Training.TS1 sub-state (4.2.1.3.2#1)
9. Transition to Training.TS1 substate occurs within tTrainingTransmission after receiving the last bit of the last SLOS2 (4.2.1.3.2#2)
10. Parse each TS1 Ordered set and verify that:
    a. Bits 58:56 are 000b if bit 4 in the Target Link Width field in USB4 Adapter Configuration Capability is 1b (two single-lane Links) (4.2.1.3.5#3)
    b. Bits 58:56 are 001b if bit 4 in the Target Link Width field in USB4 Adapter Configuration Capability is 1b (dual-lane Link) (4.2.1.3.5#3)
    c. Bits 55:48 are 00h if Ordered Set is on the Lane 0 (4.2.1.3.5#4)
    d. Bits 55:48 are 01h if Ordered Set is on the Lane 1 (4.2.1.3.5#4)
    e. Bits 31:29 are 000b (4.2.1.3.5#5)
    f. Bits 28:26 match the Lane Bonding Target field (4.2.1.3.5#8)
    g. Bits 9:0 are 00 1111 0010b (4.2.1.3.5#11)
11. Verify that the PUT sends back-to-back TS1 until all of the following are true: (4.2.1.3.2#1)
    a. KG Host/Device sent at least 2 TS1
    b. If Gen 2, PUT sent at least 32 TS1
    c. If Gen 3, PUT sent at least 16 TS1
12. Verify that the PUT transitions starts sending back-to-back TS2, which indicates entry to Training.TS2 sub-state (4.2.1.3.2#1)
13. Transition to Training.TS2 substate occurs within tTrainingTransmission after receiving the last bit of the last TS1 (4.2.1.3.2#2)
14. Parse each TS2 Ordered set and verify that:
    a. Bits 58:56 are 000b if bit 4 in the Target Link Width field in USB4 Adapter Configuration Capability is 1b (two single-lane Links) (4.2.1.3.5#3)
    b. Bits 58:56 are 001b if bit 4 in the Target Link Width field in USB4 Adapter Configuration Capability is 1b (dual-lane Link) (4.2.1.3.5#3)
    c. Bits 55:48 are 00h if Ordered Set is on the Lane 0 (4.2.1.3.5#4)
    d. Bits 55:48 are 01h if Ordered Set is on the Lane 1 (4.2.1.3.5#4)
    e. Bits 31:29 are 000b (4.2.1.3.5#5)
    f. Bits 28:26 match the Lane Bonding Target field (4.2.1.3.5#8)
    g. Bits 9:0 are 00 1111 0010b (4.2.1.3.5#11)
15. Verify that the PUT sends back-to-back TS2 until all of the following are true: (4.2.1.3.2#1)
    a. KG Host/Device sent at least 2 TS2
    b. If Gen 2, PUT sent at least 16 TS2

c. If Gen 3, PUT sent at least 8 TS2

16. Verify that the PUT transitions to CL0 state (i.e. stops sending TS2) within tTrainingAbort2 after it send the first SLOS1 symbol (4.2.1.3.3#1, 4.2.1.4.1#1)

Part 2 – Bonding State

17. Initiate bonding (see repetitions)
18. Verify that the PUT starts sending back-to-back TS1 (which indicates entry to Bonding.TS1 state) after receiving 3 TS1 (4.2.1.4.3#8, 4.2.1.4.3#9, 4.2.1.5.1#1, 4.2.1.5.1#2)
19. Send back-to-back TS1 to the PUT
20. Verify that the PUT starts sending back-to-back TS2 (which indicates entry to Bonding.TS2 state) after all of the following are true: (4.2.1.5.2#1)
    a. KG Host/Device sent at least 2 TS1
    b. If Gen 2, PUT sent at least 32 TS1
    c. If Gen 3, PUT sent at least 16 TS1
21. Send back-to-back TS2 to the PUT
22. Verify that the PUT doesn't stop sending back-to-back TS2 until all of the following are true: (4.2.1.5.2#1, 4.2.1.5.3#1)
    a. KG Host/Device sent at least 2 TS2
    b. If Gen 2, PUT sent at least 16 TS2
    c. If Gen 3, PUT sent at least 8 TS2
23. Verify that first PUT to transition to CL0 state sends TS2 until other PUT transitions to CL0 state (4.2.2.2.1#3, 4.2.1.5.3#3)
24. Verify that the PUT is in CL0 state (4.2.1.5.3#2, 4.2.1.4.1#2)
    a. Verify that the PUT transitioned back to CL0 state within tBonding time (4.2.2.2#2)
    b. Verify that both Lanes transitioned from the Training state to the CL0 state within tTrainingAbort2 time. (4.2.2.2.1#2)

Part 3 – CL0 State

25. Verify that:
    a. PUT sends a de-skew Ordered Set on each lane after Adapter transitions to CL0 state (4.4.4#3)
    b. De-Skew Ordered Set is only sent in direction exiting electrical idle (4.4.4#4)
    c. De-skew OS are sent simultaneously (within permitted skew) (4.4.4#6)
    d. Each de-skew Ordered Set is sent on both Lanes in the same locations within the Symbol (4.4.4#6)
    e. PUT sends a de-skew Ordered Set immediately after sending the last TS2 ordered set (4.4.4#8)
26. After transitioning to CL0 state, verify that the PUT sends only TS2 Ordered Sets before it sends a de-skew ordered set (4.4.4#9)
27. Read the *Plugged* bit and verify that it is 1b (4.2.1.3.3#6)
28. Stop Analyzer

TD 4.10 CL2 Test (No Re-timers)

Note: This test is not performed if PUT contains On-Board Re-timers. This test is only performed with a Passive Cable.

A. Purpose:
- Verify that the PUT enters CL2 state correctly when there are no Re-timers on the Link
- Verify that the PUT exits CL2 state correctly when there are no Re-timers on the Link

B. Asserts:
- 4.2.1.6.1#3, 4.2.1.6.1#6
- 4.2.1.6.2#1, 4.2.1.6.2#7, 4.2.1.6.2#10, 4.2.1.6.2#13, 4.2.1.6.2#14, 4.2.1.6.2#30, 4.2.1.6.2#33
- 4.2.1.6.3#1
- 4.2.1.6.4#1, 4.2.1.6.4#4
- 4.2.1.6.5.2#8-32

C. Test Setups
- H1 (Host)
- D1 (Device)
- D3 (Hub UFP)
- D5 (Hub DFP)

D. Repetitions:
- Repeat with:
  - PUT as PM Secondary
  - Link Partner as PM Secondary
- Repeat with:
  - EXIT_TIME = tEnterLFPS1
  - EXIT_TIME = 5 minutes

E. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Read the *CL2 Support* bit in the PUT
5. Do not enable Bi-Directional Time Sync Handshakes
6. Configure the PM Secondary (see repetitions)
7. Enable CLx states in the PUT and in the Link Partner:
   a. *CL2 Enable* = 1b
   b. *CL1 Enable* = 1b
   c. *CL0s Enable* = 1b
8. If both the PUT and Link Partner send CL2_REQ at the same time:
   a. If PUT is the PM Secondary, perform Part 1
   b. Else, perform Part 2
9. If the Link Partner sends CL2_REQ before the PUT:
   a. If PUT does not support CL2:
      i. Verify that the PUT sends CL_NACK (4.2.1.6.3#1)
      ii. Perform Part 1
   b. If PUT sends CL_NACK, perform Part 1
   c. If PUT sends CL2_ACK, perform Part 2

10. If the PUT sends CL2_REQ before the Link Partner:
    a. If Link Partner sends CL_NACK, perform Part 3
    b. If Link Partner sends CL2_ACK, perform Part 4
11. If neither send CL2_REQ, retry test (stop after 5 attempts)

Part 1 – PUT Sends CL_NACK

12. If PUT sent CL2_REQ and PM Secondary bit in PUT is 0b, verify that the PUT continues to send CL_NACK until last CL2_REQ is sent (4.2.1.6.2#7)
13. Else, verify that the PUT sends 16 CL_NACK (4.2.1.6.2#13)
14. Parse each CL_NACK and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#6)
15. Verify that the PUT is in CL0 state (4.2.1.6.2#14)

Part 2 – PUT Sends CL2_ACK

16. Verify that the PUT sends the CL2_ACK 375 times (4.2.1.6.2#10)
17. Parse each CL2_ACK and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#3)
18. Verify that the PUT shuts down its receivers after receiving a CL_OFF Ordered Set (4.2.1.6.2#30)
19. Verify that the PUT does the following after the equivalent of 375 symbol times passed since sending the first CL2_ACK:
    a. Shut down its transmitter (4.2.1.6.2#33)
    b. Transitions to CL2 state (4.2.1.6.2#33)
20. Verify that transmitter is in electrical idle (4.2.1.6.4#1)
21. Verify that Lane common mode voltages are maintained (4.2.1.6.4#1)
22. Verify that receiver termination is maintained (4.2.1.6.4#4)
23. Perform Part 5

Part 3 – Link Partner Sends CL_NACK

24. PUT sent back-to-back CL2_REQ until it received CL_NACK (4.2.1.6.2#1)
25. PUT does not send another CL2_REQ or CL1_REQ for at least tCLxRetry (4.2.1.6.2#20)
26. PUT Adapters are in CL0 state (4.2.1.6.2#21)

Part 4 – Link Partner Sends CL2_ACK

27. PUT sent back-to-back CL2_REQ until it receives CL2_ACK (4.2.1.6.2#1)
28. PUT sends 375 CL_OFF Ordered Sets (4.2.1.6.2#17)
29. The first CL_OFF Ordered Set is sent within tCLxResponse after getting the CL2_ACK (4.2.1.6.2#18)
30. The PUT shuts off its receivers (4.2.1.6.2#19)
31. The PUT shuts off its transmitters within tTxOff time after sending the last CL_OFF Ordered Set (4.2.1.6.2#24)
32. The PUT Adapters are in the CL2 state (4.2.1.6.2#25)
33. Perform Part 5

Part 5 – CL2 Exit

34. Wait EXIT_TIME time after detecting that the PUT transitioned to CL2 state (see repetitions)
35. Send the PUT a Read Request to cause the PUT Adapters to exit the CL2 state

36. Verify that the PUT does the following:
    a. Sends an LFPS burst on the Lane for at least 3 LFPS cycles (4.2.1.6.5.2#8)
    b. Returns to Electrical Idle for tPreData (4.2.1.6.5.2#9)
    c. Starts transmitting SLOS1 on the Lane (4.2.1.6.5.2#10)
    d. Enables the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received (4.2.1.6.5.2#11)
    e. Completes Symbol lock within tRxLock time (4.2.1.6.5.2#11)
    f. Transitions to Training.LOCK1 sub-state (4.2.1.3.1#3, 4.2.1.6.5.2#12)
    g. Enables SSC if SSC is disabled (4.2.1.6.5.2#13)
37. Verify that the PUT transitions to CL0 state (4.2.1.4.1#1)

TD 4.11 CL2 Test (Re-timers)

Note: This test is only performed with an Active Cable.

A. Purpose:
- Verify that the PUT enters CL2 state correctly when there are Re-timers on the Link
- Verify that the PUT exits CL2 state correctly when there are Re-timers on the Link

B. Asserts:
- 4.2.1.3.1#3
- 4.2.1.6.1#3, 4.2.1.6.1#6
- 4.2.1.6.1.2#9, 4.2.1.6.1.2#10
- 4.2.1.6.2#1, 4.2.1.6.2#7, 4.2.1.6.2#10, 4.2.1.6.2#13, 4.2.1.6.2#14, 4.2.1.6.2#33
- 4.2.1.6.3#1
- 4.2.1.6.4#1, 4.2.1.6.4#4
- 4.2.1.6.5.3#9-45, 4.2.1.6.5#48
- 4.2.4.2#1rt
- 4.2.4.3.2.1#1rt, 4.2.4.3.2.1#4rt, 4.2.4.3.2.1#5rt
- 4.2.4.3.2.3#4rt
- 4.2.4.3.3#2rt

C. Test Setups
- H1 (Host)
- D1 (Device)
- D3 (Hub UFP)
- D5 (Hub DFP)

D. Repetitions:
- Repeat with:
  - PUT as PM Secondary
  - Link Partner as PM Secondary
- Repeat with:
  - EXIT_TIME = tEnterLFPS1
  - EXIT_TIME = 5 minutes

E. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Read the *CL2 Support* bit in the PUT
5. Do not enable Bi-Directional Time Sync Handshakes
6. Configure the PM Secondary (see repetitions)
7. Enable CLx states in the PUT and in the Link Partner:
   a. *CL2 Enable* = 1b
   b. *CL1 Enable* = 1b
   c. *CL0s Enable* = 1b
8. If both the PUT and Link Partner send CL2_REQ at the same time:
   a. If PUT is the PM Secondary, perform Part 1
   b. Else, perform Part 2
9. If the Link Partner sends CL2_REQ before the PUT:
   a. If PUT does not support CL2:
      i. Verify that the PUT sends CL_NACK (4.2.1.6.3#1)
      ii. Perform Part 1

b. If PUT sends NACK, perform Part 1
c. If PUT sends ACK, perform Part 2

10. If the PUT sends CL2_REQ before the Link Partner:
    a. If Link Partner sends NACK, perform Part 3
    b. If Link Partner sends ACK, perform Part 4
11. If neither send CL2_REQ, retry test (stop after 5 attempts)

Part 1 – PUT Sends CL_NACK

12. If PUT sent CL2_REQ and PM Secondary bit in PUT is 0b, verify that the PUT continues to send CL_NACK until last CL2 REQ is sent (4.2.1.6.2#7)
13. Else, verify that the PUT sends 16 CL_NACK (4.2.1.6.2#13)
14. Parse each CL_NACK and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#6)
15. Verify that the PUT is in CL0 state (4.2.1.6.2#14)

Part 2 – PUT Sends CL2_ACK

16. Verify that the PUT sends the CL2_ACK 375 times (4.2.1.6.2#10)
17. Parse each CL2_ACK and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#3)
18. Verify that the PUT shuts down its receivers after receiving a CL_OFF (4.2.1.6.2#30)
19. Verify that the PUT does the following after the equivalent of 375 symbol times passed since sending the first CL2_ACK:
    a. Shut down its transmitter (4.2.1.6.2#33)
    b. Transitions to CL2 state (4.2.1.6.2#33)
20. Verify that transmitter is in electrical idle (4.2.1.6.4#1, 4.2.4.2#1rt)
21. Verify that Lane common mode voltages are maintained (4.2.1.6.4#1, 4.2.4.2#1rt)
22. Verify that receiver termination is maintained (4.2.1.6.4#4)
23. Perform Part 5

Part 3 – Link Partner Sends CL_NACK

24. PUT sent back-to-back CL2_REQ until it received CL_NACK (4.2.1.6.2#1)
25. PUT does not send another CL2_REQ or CL1_REQ for at least tCLxRetry (4.2.1.6.2#20)
26. PUT Adapters are in CL0 state (4.2.1.6.2#21)

Part 4 – Link Partner Sends CL2_ACK

27. PUT sent back-to-back CL2_REQ until it received CL2_ACK (4.2.1.6.2#1)
28. PUT sends 375 CL_OFF Ordered Sets (4.2.1.6.2#17)
29. The first CL_OFF Ordered Set is sent within tCLxResponse after getting the CL2_ACK (4.2.1.6.2#18)
30. The PUT shuts off its receivers (4.2.1.6.2#19)
31. The PUT shuts off its transmitters within tTxOff time after sending the last CL_OFF Ordered Set (4.2.1.6.2#24)
32. The PUT Adapters are in the CL2 state (4.2.1.6.2#25)
33. Perform Part 5

Part 5 – CL2 Exit

34. Wait EXIT_TIME time after detecting that the PUT transitioned to CL2 state (see repetitions)
35. Send the PUT a Read Request to cause the PUT Adapters to exit the CL2 state
36. Verify that the PUT does the following:
    a. Sends a LFPS burst on the Lane for at least 3 LFPS cycles (4.2.1.6.5.3#9)
        i. If PUT contains On-Board Re-timers, LFPS is sent for at least 5 LFPS cycles (4.2.4.3.2.1#1rt)
    b. Returns to Electrical Idle for tPreData (4.2.1.6.5.3#10, 4.2.4.3.2.1#5rt)
    c. Transmits Ordered Sets as follows:
        i. If PUT does not contain On-Board Re-timers, it starts transmitting SLOS1 on the Lane (4.2.1.6.5.3#11)
        ii. If PUT contains On-Board Re-timers, it starts transmitting CL_WAKE1.X Ordered Set Symbols (4.2.4.3.2.1#5rt)
    d. Enables the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received (4.2.1.6.5.3#12, 4.2.4.3.2.1#4rt)
    e. Completes Symbol lock as follows:
        i. If no On-Board Re-timers, complete within tRxLock time (4.2.1.6.5.3#12)
        ii. If On-Board Re-timers, complete within tCLxLock time (4.2.4.3.3#2rt)
    f. Upon reception of 3 consecutive and identical CL_WAKE1.X Ordered Sets, starts transmitting CL_WAKE2.X Ordered Sets on the Lane (4.2.1.6.5#48, 4.2.1.6.5.3#13)
        i. CL_WAKE2.X from PUT are not scrambled (4.2.1.6.1.2#9)
        ii. PUT does not send any partial CL_WAKE2.X (4.2.1.6.1.2#10)
    g. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Sets, transition to Training.LOCK1 substate (4.2.1.3.1#3, 4.2.1.6.5.3#14)
    h. Upon reception of 7 back-to-back SLOS Symbols, transitions to Training.LOCK1 substate (4.2.1.3.1#3, 4.2.1.6.5.3#14)
    i. Enable SSC if SSC is disabled (4.2.1.6.5.3#15)
    j. If PUT contains On-Board Re-timers, verify that it stops sending CL_WAKE1.X Ordered Set Symbols (4.2.4.3.2.3#4rt)
37. Verify that the PUT transitions to CL0 state

TD 4.12 CL1 Test (No Re-timers)

Note: This test is not performed if PUT contains On-Board Re-timers. This test is only performed with a Passive Cable.

A. Purpose:
- Verify that the PUT enters CL1 state correctly when there are no Re-timers on the Link
- Verify that the PUT exits CL1 state correctly when there are no Re-timers on the Link

B. Asserts:
- 4.2.1.6.1#4, 4.2.1.6.1#6
- 4.2.1.6.2#1, 4.2.1.6.2#7, 4.2.1.6.2#11, 4.2.1.6.2#13, 4.2.1.6.2#14, 4.2.1.6.2#30, 4.2.1.6.2#34
- 4.2.1.6.3#16
- 4.2.1.6.4#2, 4.2.1.6.4#4
- 4.2.1.6.5.2#8-32

C. Test Setups
- H1 (Host)
- D1 (Device)
- D3 (Hub UFP)
- D5 (Hub DFP)

D. Repetitions:
- Repeat with:
  - PUT as PM Secondary
  - Link Partner as PM Secondary
- Repeat with:
  - EXIT_TIME = tEnterLFPS1
  - EXIT_TIME = 5 minutes

E. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Read the *CL1 Support* bit in the PUT
5. Do not enable Bi-Directional Time Sync Handshakes
6. Configure the PM Secondary (see repetitions)
7. Enable CLx states in the PUT and in the Link Partner:
   a. *CL2 Enable* = 0b
   b. *CL1 Enable* = 1b
   c. *CL0s Enable* = 1b
8. If both the PUT and Link Partner send CL1_REQ at the same time:
   a. If PUT is the PM Secondary, perform Part 1
   b. Else, perform Part 2
9. If the Link Partner sends CL1_REQ before the PUT:
   a. If PUT does not support CL1:
      i. Verify that the PUT sends CL_NACK (4.2.1.6.3#16)
      ii. Perform Part 1
   b. If PUT sends CL_NACK, perform Part 1
   c. If PUT sends CL1_ACK, perform Part 2

10. If the PUT sends CL1_REQ before the Link Partner:
    a. If Link Partner sends CL_NACK, perform Part 3
    b. If Link Partner sends CL1_ACK, perform Part 4
11. If neither send CL1_REQ, retry test (stop after 5 attempts)

Part 1 – PUT Sends CL_NACK

12. If PUT sent CL1_REQ and PM Secondary bit in PUT is 0b, verify that the PUT continues to send CL_NACK until last CL1_REQ is sent (4.2.1.6.2#7)
13. Else, verify that the PUT sends 16 CL_NACK (4.2.1.6.2#13)
14. Parse each CL_NACK and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#6)
15. Verify that the PUT is in CL0 state (4.2.1.6.2#14)

Part 2 – PUT Sends CL1_ACK

16. Verify that the PUT sends the CL1_ACK 375 times (4.2.1.6.2#11)
17. Parse each CL1_ACK and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#4)
18. Verify that the PUT shuts down its receivers after receiving a CL_OFF (4.2.1.6.2#30)
19. Verify that the PUT does the following after the equivalent of 375 symbol times passed since sending the first CL1_ACK:
    a. Shut down its transmitter (4.2.1.6.2#34)
    b. Transitions to CL1 state (4.2.1.6.2#34)
20. Verify that transmitter is in electrical idle (4.2.1.6.4#2)
21. Verify that Lane common mode voltages are maintained (4.2.1.6.4#2)
22. Verify that receiver termination is maintained (4.2.1.6.4#4)
23. Perform Part 5

Part 3 – Link Partner Sends CL_NACK

24. PUT sent back-to-back CL2_REQ until it received CL_NACK (4.2.1.6.2#1)
25. PUT does not send another CL2_REQ or CL1_REQ for at least tCLxRetry (4.2.1.6.2#20)
26. PUT Adapters are in CL0 state (4.2.1.6.2#21)

Part 4 – Link Partner Sends CL1_ACK

27. PUT sent back-to-back CL1_REQ until it received CL1_ACK (4.2.1.6.2#1)
28. PUT sends 375 CL_OFF Ordered Sets (4.2.1.6.2#17)
29. The first CL_OFF Ordered Set is sent within tCLxResponse after getting the CL1_ACK (4.2.1.6.2#18)
30. The PUT shuts off its receivers (4.2.1.6.2#19)
31. The PUT shuts off its transmitters within tTxOff time after sending the last CL_OFF Ordered Set (4.2.1.6.2#24)
32. The PUT Adapters are in the CL1 state (4.2.1.6.2#26)
33. Perform Part 5

Part 5 – CL1 Exit

34. Wait EXIT_TIME time after detecting that the PUT transitioned to CL1 state (see repetitions)
35. Send the PUT a Read Request to cause the PUT Adapters to exit the CL1 state

36. Verify that the PUT does the following:
    a. Sends an LFPS burst on the Lane for at least 3 LFPS cycles (4.2.1.6.5.2#8)
    b. Returns to Electrical Idle for tPreData (4.2.1.6.5.2#9)
    c. Starts transmitting SLOS1 on the Lane (4.2.1.6.5.2#10)
    d. Enables the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received (4.2.1.6.5.2#11)
    e. Completes Symbol lock within tRxLock time (4.2.1.6.5.2#11)
    f. Transitions to Training.LOCK1 sub-state (4.2.1.3.1#3, 4.2.1.6.5.2#12)
    g. Enables SSC if SSC is disabled (4.2.1.6.5.2#13)
37. Verify that the PUT transitions to CL0 state

TD 4.13 CL1 Test (Re-timers)

Note: This test is only performed with an Active Cable.

A. Purpose:
- Verify that the PUT enters CL1 state correctly when there are Re-timers on the Link
- Verify that the PUT exits CL1 state correctly when there are Re-timers on the Link

B. Asserts:
- 4.2.1.3.1#3
- 4.2.1.6.1#4, 4.2.1.6.1#6
- 4.2.1.6.1.2#9, 4.2.1.6.1.2#10
- 4.2.1.6.2#7, 4.2.1.6.2#11, 4.2.1.6.2#13, 4.2.1.6.2#14, 4.2.1.6.2#34
- 4.2.1.6.3#16
- 4.2.1.6.4#2, 4.2.1.6.4#4
- 4.2.1.6.5.3#9-45, 4.2.1.6.5#48
- 4.2.4.2#2rt
- 4.2.4.3.2.1#1rt, 4.2.4.3.2.1#4rt, 4.2.4.3.2.1#5rt
- 4.2.4.3.2.3#4rt
- 4.2.4.3.3#2r

C. Test Setups
- H1 (Host)
- D1 (Device)
- D3 (Hub UFP)
- D5 (Hub DFP)

D. Repetitions:
- Repeat with:
  - PUT as PM Secondary
  - Link Partner as PM Secondary
- Repeat with:
  - EXIT_TIME = tEnterLFPS1
  - EXIT_TIME = 5 minutes

E. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Read the *CL1 Support* bit in the PUT
5. Do not enable Bi-Directional Time Sync Handshakes
6. Configure the PM Secondary (see repetitions)
7. Enable CLx states in the PUT and in the Link Partner:
   a. *CL2 Enable* = 0b
   b. *CL1 Enable* = 1b
   c. *CL0s Enable* = 1b
8. If both the PUT and Link Partner send CL1_REQ at the same time:
   a. If PUT is the PM Secondary, perform Part 1
   b. Else, perform Part 2
9. If the Link Partner sends CL1_REQ before the PUT:
   a. If PUT does not support CL1:
      i. Verify that the PUT sends CL_NACK (4.2.1.6.3#16)
      ii. Perform Part 1
   b. If PUT sends NACK, perform Part 1

    c. If PUT sends ACK, perform Part 2
10. If the PUT sends CL1_REQ before the Link Partner:
    a. If Link Partner sends NACK, perform Part 3
    b. If Link Partner sends ACK, perform Part 4
11. If neither send CL1_REQ, retry test (stop after 5 attempts)

Part 1 – PUT Sends CL_NACK

12. If PUT sent CL2_REQ and PM Secondary bit in PUT is 0b, verify that the PUT continues to send CL_NACK until last CL1_REQ is sent (4.2.1.6.2#7)
13. Else, verify that the PUT sends 16 CL_NACK (4.2.1.6.2#13)
14. Parse each CL_NACK and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#6)
15. Verify that the PUT is in CL0 state (4.2.1.6.2#14)

Part 2 – PUT Sends CL1_ACK

16. Verify that the PUT sends the CL1_ACK 375 times (4.2.1.6.2#11)
17. Parse each CL1_ACK and verify that bits 9:0 (SCR) in the payload are 00 1111 0010b (4.2.1.6.1#4)
18. Verify that the PUT shuts down its receivers after receiving a CL_OFF (4.2.1.6.2#30)
19. Verify that the PUT does the following after the equivalent of 375 symbol times passed since sending the first CL1_ACK:
    a. Shut down its transmitter (4.2.1.6.2#33)
    b. Transitions to CL1 state (4.2.1.6.2#33)
20. Verify that transmitter is in electrical idle (4.2.1.6.4#2, 4.2.4.2#2rt)
21. Verify that Lane common mode voltages are maintained (4.2.1.6.4#2, 4.2.4.2#2rt)
22. Verify that receiver termination is maintained (4.2.1.6.4#4)
23. Perform Part 5

Part 3 – Link Partner Sends CL_NACK

24. PUT sent back-to-back CL1_REQ until it received CL_NACK (4.2.1.6.2#1)
25. PUT does not send another CL2_REQ or CL1_REQ for at least tCLxRetry (4.2.1.6.2#20)
26. PUT Adapters are in CL0 state (4.2.1.6.2#21)

Part 4 – Link Partner Sends CL1_ACK

27. PUT sent back-to-back CL1_REQ until it received CL1_ACK (4.2.1.6.2#1)
28. PUT sends 375 CL_OFF Ordered Sets (4.2.1.6.2#17)
29. The first CL_OFF Ordered Set is sent within tCLxResponse after getting the CL1_ACK (4.2.1.6.2#18)
30. The PUT shuts off its receivers (4.2.1.6.2#19)
31. The PUT shuts off its transmitters within tTxOff time after sending the last CL_OFF Ordered Set (4.2.1.6.2#24)
32. The PUT Adapters are in the CL1 state (4.2.1.6.2#26)
33. Perform Part 5

Part 5 – CL1 Exit

34. Wait EXIT_TIME time after detecting that the PUT transitioned to CL1 state (see repetitions)
35. Send the PUT a Read Request to cause the PUT Adapters to exit the CL1 state
36. Verify that the PUT does the following:
    a. Sends an LFPS burst on the Lane for at least 3 LFPS cycles (4.2.1.6.5.3#9)
        i. If PUT contains On-Board Re-timers, LFPS is sent for at least 5 LFPS cycles (4.2.4.3.2.1#1rt)
    b. Returns to Electrical Idle for tPreData (4.2.1.6.5.3#10, 4.2.4.3.2.1#5rt)
    c. If PUT does not contain On-Board Re-timers, it starts transmitting SLOS1 on the Lane (4.2.1.6.5.3#11)
    d. If PUT contains On-Board Re-timers, it starts transmitting CL_WAKE1.X Ordered Set Symbols (4.2.4.3.2.1#5rt)
    e. Enables the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received (4.2.1.6.5.3#12, 4.2.4.3.2.1#4rt)
    f. Complete Symbol lock
        i. If no On-Board Re-timers, complete within tRxLock time (4.2.1.6.5.3#12)
        ii. If On-Board Re-timers, complete within tCLxLock time (4.2.4.3.3#2rt)
    g. Upon reception of 3 consecutive and identical CL_WAKE1.X Ordered Sets, starts transmitting CL_WAKE2.X Ordered Sets on the Lane (4.2.1.6.5#48, 4.2.1.6.5.3#13)
    h. CL_WAKE2.X from PUT are not scrambled (4.2.1.6.1.2#9)
    i. PUT does not send any partial CL_WAKE2.X (4.2.1.6.1.2#10)
    j. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Sets, transitions to Training.LOCK1 substate (4.2.1.3.1#3, 4.2.1.6.5.3#14)
    k. Upon reception of 7 back-to-back SLOS Symbols, transitions to Training.LOCK1 substate (4.2.1.3.1#3, 4.2.1.6.5.3#14)
    l. Enable SSC if SSC is disabled (4.2.1.6.5.3#15)
    m. If PUT contains On-Board Re-timers, verify that it stops sending CL_WAKE1.X Ordered Set Symbols (4.2.4.3.2.3#4rt)
37. Verify that the PUT transitions to CL0 state

TD 4.14 CL0s Test (No Re-timers)

Note: This test is not performed if PUT contains On-Board Re-timers. This test is only performed with a Passive Cable.

Note: This test is not performed if the Router does not support CL0s state.

Note: This test is only performed on DFP

A. Purpose:
   - Verify that the PUT enters CL0s state correctly when there are no Re-timers on the Link
   - Verify that the PUTs exit CL0s state correctly when there are no Re-timers on the Link

B. Asserts:
   - 4.2.1.4.1#3
   - 4.2.1.6.1#5
   - 4.2.1.6.2#12, 4.2.1.6.2#30
   - 4.2.1.6.4#3, 4.2.1.6.4#4
   - 4.2.1.6.5.1#11, 4.2.1.6.5.1#12, 4.2.1.6.5.1#15, 4.2.1.6.5.1#16

C. Test Setups
   - H1 (Host)
   - D5 (Hub)

D. Repetitions:
   - Repeat with:
     - EXIT_TIME = (375 Symbol Times + 100ns)
     - EXIT_TIME = 5 minutes

E. Procedure:

USB4 CV performs the following steps:

Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Read the *CL0s Support* bit in PUT
5. Enable CLx states in the PUT and the PUT Link Partner:
   a. *CL2 Enable* = 1b
   b. *CL1 Enable* = 1b
   c. *CL0s Enable* = 1b
6. Configure/enable unidirectional timestamps (HiFi mode) for objection to CL2/CL1 in the PUT

Part 1 – Initiate CL0s Entry

7. Wait for the Link Partner to send CL2_REQ Ordered Sets
8. Verify that the PUT responds with CL0s_ACK (4.2.1.6.2#12)
9. Parse each CL0s_ACK and verify that bits 9:0 (SCR) in the payload are 00 1111 0010 (4.2.1.6.1#5)
10. Verify that the PUT sends CL0s_ACK for 16 symbol times (4.2.1.6.2#12)
11. Send CL_OFF to PUT for 375 symbol times
12. Verify that the PUT transitions to CL0s state after receiving CL_OFF (4.2.1.6.2#30)

13. Verify that transmitter is in electrical idle (4.2.1.6.4#3)
14. Verify that Lane common mode voltages are maintained (4.2.1.6.4#3)
15. Verify that receiver termination is maintained (4.2.1.6.4#4)

Part 2 – Initiate CL0s Exit

16. Send the PUT a Read Request to cause the PUT Adapters to exit the CL0s state
17. Verify that the PUT does the following after detecting LFPS:
    a. Enables the receiver not earlier than tCLxIdleRx after the last LFPS cycle received (4.2.1.6.5.1#11)
    b. Completes Symbol lock within tRxLock time (4.2.1.6.5.1#11)
    c. On reception of 3 consecutive CL_WAKE1.X Ordered Sets, transmits 16 CL_WAKE2.X Ordered Sets. (4.2.1.6.5.1#12)
    d. On detection of 3 consecutive SLOS Symbols, transmits 16 TS2 Ordered Sets (4.2.1.6.5.1#15)
    e. On detection of 2 consecutive TS2 Ordered Sets, transitions to CL0 state (4.2.1.6.5.1#16, 4.2.1.4.1#3)

TD 4.15 CL0s Test (Re-timers)

Note: This test is only performed with an Active Cable.

Note: This test is not performed if the Router does not support CL0s state.

A. Purpose:
- Verify that the PUT enters CL0s state correctly when there are Re-timers on the Link
- Verify that the PUTs exit CL0s state correctly when there are Re-timers on the Link

B. Asserts:
- 4.2.1.4.1#3
- 4.2.1.6.1#5
- 4.2.1.6.2#12, 4.2.1.6.2#30, 4.2.1.6.2#35
- 4.2.1.6.4#3, 4.2.1.6.4#4
- 4.2.1.6.5.1#11, 4.2.1.6.5.1#12, 4.2.1.6.5.1#15, 4.2.1.6.5.1#16
- 4.2.4.2#3rt
- 4.2.4.3.1#3rt, 4.2.4.3.1#4rt, 4.2.4.3.1#7rt
- 4.2.4.3.3#2rt

C. Test Setups
- H1 (Host)
- D1 (Device)
- D3 (Hub UFP)
- D5 (Hub DFP)

D. Repetitions:
- Repeat with:
  - EXIT_TIME = (375 Symbol Times + 100ns)
  - EXIT_TIME = 5 minutes

E. Procedure:

USB4 CV performs the following steps:

Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Read the *CL0s Support* bit in PUT
5. Enable CLx states in the PUT and the PUT Link Partner:
   a. *CL2 Enable* = 1b
   b. *CL1 Enable* = 1b
   c. *CL0s Enable* = 1b
6. Configure/enable unidirectional timestamps (HiFi mode) for objection to CL2/CL1 in the PUT

Part 1 – Initiate CL0s Entry

7. Wait for the Link Partner to send CL2_REQ Ordered Sets
8. Verify that the PUT responds with CL0s_ACK (4.2.1.6.2#12)
9. Parse each CL0s_ACK and verify that bits 9:0 (SCR) in the payload are 00 1111 0010 (4.2.1.6.1#5)
10. Verify that the PUT sends CL0s_ACK for 16 symbol times (4.2.1.6.2#12)
11. Send CL_OFF to PUT for 375 symbol times

12. Verify that the PUT transitions to CL0s state after receiving CL_OFF (4.2.1.6.2#30)
13. Wait the equivalent of 375 Symbol Times after the PUT sends the first response Ordered Set
14. Verify that the PUT:
    a. Shuts down its receiver (4.2.1.6.2#35)
    b. Transitions to CL0s state (4.2.1.6.2#35)
15. Verify that transmitter is in electrical idle (4.2.1.6.4#3, 4.2.4.2#3rt)
16. Verify that Lane common mode voltages are maintained (4.2.1.6.4#3, 4.2.4.2#3rt)
17. Verify that receiver termination is maintained (4.2.1.6.4#4)

Part 2 – Initiate CL0s Exit

18. Send the PUT a Read Request to cause the PUT Adapters to exit the CL0s state
19. Verify that the PUT does the following after detecting LFPS:
    a. Enables the receiver not earlier than tCLxIdleRx after the last LFPS cycle received (4.2.1.6.5.1#11, 4.2.4.3.1#3rt)
    b. If PUT contains On-Board Re-timers, PUT sends CL_WAKE1.X Ordered Set Symbols (4.2.4.3.1#4rt)
    c. Complete Symbol lock
        i. If no On-Board Re-timers, complete within tRxLock time ((4.2.1.6.5.1#11)
        ii. If On-Board Re-timers, complete within tCLxLock time (4.2.4.3.3#2rt)
    d. On reception of 3 consecutive CL_WAKE1.X Ordered Sets, transmits 16 CL_WAKE2.X Ordered Sets. (4.2.1.6.5.1#12)
    e. On detection of 3 consecutive SLOS Symbols, transmits 16 TS2 Ordered Sets (4.2.1.6.5.1#15)
    f. On detection of 2 consecutive TS2 Ordered Sets, transitions to CL0 state (4.2.1.6.5.1#16, 4.2.1.4.1#3)
    g. If PUT contains On-Board Re-timers, PUT stop sending CL_WAKE1.X Ordered Set Symbols (4.2.4.3.1#7rt)
20. If PUT contains On-Board Re-timers, verify that the PUT sends CL_WAKE1.X Ordered Set Symbols

TD 4.16 CLx Exit Initiation Test

Note: This test is not performed if the Router does not support CLx states.

A. Purpose:
- Verify that the PUT initiates exit from CLx states correctly

B. Asserts:
- 4.2.1.6.5#1, 4.2.1.6.5.1#1-4, 4.2.1.6.5.1#8-9, 4.2.1.6.5.2#1-5, 4.2.1.6.5.3#1-5

C. Test Setups
- H1 (Host)
- D1 (Device)
- D3 (Hub UFP)
- D5 (Hub DFP)

D. Repetitions:
- Repeat for all supported CLx states

E. Procedure:

USB4 CV performs the following steps:

Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Transition the PUT Adapters to CLx state (see repetitions)
5. If testing CL0s exit, perform Part 1
6. If testing CL1 or CL2 exit and there are no Re-timers on the Link, perform Part 2
7. If testing CL1 or CL2 exit and there are one or more Re-timers in the Link, perform Part 3

Part 1 – CL0s exit

8. Send the PUT a Read Request to cause the PUT Adapters to exit the CL0s state
9. Verify that the PUT transitions out of CL0s state as follows: (4.2.1.6.5#1)
    a. PUT sends an LFPS burst on all Lanes for the duration of at least 16 LFPS cycles (4.2.1.6.5.1#1)
    b. PUT returns to Electrical Idle for tPreData (4.2.1.6.5.1#2)
    c. PUT starts transmitting SLOS1 on each Lane of the USB4 Port (4.2.1.6.5.1#3)
    d. On detection of 2 back-to-back TS2 Ordered Sets, PUT stops sending SLOS1 and sends at least 16 TS2 Ordered Sets (4.2.1.6.5.1#4)
    e. PUT Adapters transition to CL0 state (4.2.1.6.5.1#8)
10. Verify that PUT resumes operation as a Dual-Lane Link (4.2.1.6.5.1#9)
11. Verify that PUT sends a de-skew Ordered Set (4.2.1.6.5.1#9)

Part 2 – CL1/CL2 Exit (no Re-timers)

9. Send the PUT a Read Request to cause the PUT Adapters to exit the CL1/CL2 state
10. Verify that the PUT transitions out of CL1/CL2 state as follows:
    a. PUT sends a Low Frequency Periodic Signaling (LFPS) burst on each Lane until the receiver detects LFPS (4.2.1.6.5.2#1)
    b. PUT Returns to Electrical Idle for tPreData time (4.2.1.6.5.2#3)

c. PUT starts transmitting SLOS1 (4.2.1.6.5.2#4)
d. PUT Adapters complete Symbol lock within tRxLock time (4.2.1.6.5.2#5)
e. PUT Adapters transition to Training.LOCK1 sub-state (4.2.1.6.5.2#6)

Part 3 – CL1/CL2 Exit (Re-timers)

9. Send the PUT a Read Request to cause the PUT Adapters to exit the CL1/CL2 state
10. Verify that the PUT transitions out of CL1/CL2 state as follows:
    a. PUT sends a Low Frequency Periodic Signaling (LFPS) burst on each Lane until its receiver detects LFPS (4.2.1.6.5.3#1)
    b. PUT returns to Electrical Idle for tPreData (4.2.1.6.5.3#3)
    c. PUT starts transmitting SLOS1 (4.2.1.6.5.3#4)
    d. PUT Adapters complete Symbol lock within tRxLock time. (4.2.1.6.5.3#5)
    e. Upon reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols, PUT starts transmitting CL_WAKE2.X Ordered Set Symbols (4.2.1.6.5.3#6)
    f. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, PUT Adapters transition to Training.LOCK1 sub-state (4.2.1.6.5.3#7)

Lane 0/Lane 1 Tests

Unless specified otherwise, the tests in this section are performed on all Ports of a UUT. The tests are performed at the highest speed that the UUT supports. Lanes are bonded and RS-FEC is enabled.

Background Check

This test is performed by the Analyzer in conjunction with all of the Lane 0/Lane 1 Tests.

1. Parse each TSI and TS2 Ordered Set and verify that bits 31:29 (Rsvd) are 0. (4.2.1.3.5#6)
2. When an Adapter transitions to the CL0 state and Lanes are not bonded, verify that the first bytes transmitted after the last TS2 Ordered Set are either a Transport Layer Packet header or an Ordered Set that is not SLOS, TS1, or TS2. (4.4.1#1)
3. When an Adapter transitions to the CL0 state and Lanes are bonded, verify that the first bytes transmitted after the last TS2 Ordered Set are a de-skew Ordered Set followed by either a Transport Layer Packet header, an Idle Packet or any Ordered Set other than SLOS, TS1 or TS2. (4.4.1#2)
4. When operating with a Dual-lane Link, verify that if one Lane transitions to Training State, other Lane also transitions to training state (4.2.2.2#8)

Link Tests

Unless noted otherwise, the tests in this section are performed at Gen 2 speed and repeated at Gen 3 speed (if Gen 3 speed is supported).

TD 4.17 UFP SBRX Disconnect Test (UFP Only)

Note: This test is only performed on the UFP.

A. Purpose:

- Verify that the PUT handles SBRX-initiated Disconnect on UFP correctly

B. Asserts:

- 4.4.5.1.1#1-5

C. Repeat with the following Disconnect Events:

- Router Hot Unplug (4.4.5.1.1#3) – disable/enable to generate
- DFP Reset (4.4.5.1.1#4)
- The Domain enters Sleep state and the *USB4 Port is Configured* bit in a USB4 Port is set to 0b (4.4.5.1.1#5)

D. Test Setups

- D1 (Device)
- D3 (Hub)

E. Procedure:

USB4 CV performs the following steps:

1. Start Analyzer
2. Reset UUT
3. Perform Lane Initialization
4. Wait for PUT Adapters to reach CL0 state
5. Set the following fields:
   a. *Link Credits Allocated* = 2
   b. *Inter-Domain Slave* = 1b
   c. *CL0s Enable* = 1b
   d. *CL1 Enable* = 1b
   e. *CL2 Enable* = 1b
   f. *Lane Bonding* = 1b
6. Initiate Disconnect Event (see repetitions)
7. Verify that the PUT drives SBTX low for at least tDisconnectTx (4.4.5.1.1#1)
8. Read the following fields and verify default values: (4.4.5.1.1#2)
   a. *Link Credits Allocated* = 0
   b. *Inter-Domain Slave* = 0b
   c. *CL0s Enable* = 0b
   d. *CL1 Enable* = 0b
   e. *CL2 Enable* = 0b
   f. *Lane Bonding* = 0b
9. Stop Analyzer

TD 4.18 DFP SBRX Disconnect Test (DFP Only)

Note: This test is only performed on DFP

A. Purpose:

- Verify that the PUT handles SBRX-initiated Disconnect on DFP correctly

B. Asserts:

- 4.4.5.2.1#1-3, 4.4.5.2.1#6, 4.4.5.2.1#7

C. Test Setups

- H1 (Host)
- D5 (Hub)

D. Procedure:

USB4 CV performs the following steps:

1. Start Analyzer
2. Reset UUT
3. Wait for a Hot Plug Event Packet with UPG=0b from the PUT
4. Enumerate UUT Router
5. Set the following fields:
    a. *Link Credits Allocated* = 2
    b. *Inter-Domain Slave* = 1b
    c. *CL0s Enable* = 1b
    d. *CL1 Enable* = 1b
    e. *CL2 Enable* = 1b
    f. *Lane Bonding* = 1b
6. Configure a Loopback Path
7. Continuously send traffic on Loopback Path
8. Initiate a disconnect so that the Link Partner drives SBTX to logical low for tDisconnectRx
9. Verify that the PUT does the following:
    a. Sends an LT_LRoff Transaction (4.4.5.2.1#1)
    b. Stops sending Transport Layer Packets (4.4.5.2.1#2)
10. Verify that both PUT Adapters are in CLd state (4.4.5.2.1#3)
11. Verify that the PUT sends a Hot Unplug Event Packet with UPG = 1b for each enabled Adapter (4.4.5.2.1#6)
12. Read the following fields from the Adapter Configuration space of each PUT and verify that the following fields have default values
    a. *Link Credits Allocated* = 0
    b. *Inter-Domain Slave* = 0b
    c. *CL0s Enable* = 0b
    d. *CL1 Enable* = 0b
    e. *CL2 Enable* = 0b
    f. *Lane Bonding* = 0b
13. Stop Analyzer

TD 4.19 LT_LRoff Disconnect Test (DFP Only)

Note: This test is only performed on DFP.

A. Purpose:

- Verify that the PUT handles Disconnect on DFP correctly

B. Asserts:

- 4.4.5.2.2#1, 4.4.5.2.2#3, 4.4.5.2.2#6, 4.4.5.2.2#7, 4.4.5.2.2#9

C. Test Setups

- H2 (Host)
- D5 (Hub)

D. Procedure:

USB4 CV performs the following steps:

1. Reset UUT
2. Wait for a Hot Plug Event Packet with UPG=0b from the PUT
3. Enumerate UUT Router
4. Set the following fields:
    a. *Link Credits Allocated* = 2
    b. *Inter-Domain Slave* = 1b
    c. *CL0s Enable* = 1b
    d. *CL1 Enable* = 1b
    e. *CL2 Enable* = 1b
    f. *Lane Bonding* = 1b
5. Set the Enter Sleep bit to 0b
6. Enable inter-Domain Wake
7. Transition Domain to sleep state
8. Tell the Link Partner to send an LT_LRoff Transaction to the PUT
9. Verify that the PUT does the following:
    a. Send an LT_LRoff Transaction (4.4.5.2.2#1)
    b. Adapters transition to the CLd state (4.4.5.2.2#3)
10. Verify that the PUT starts Lane Initialization (4.4.5.2.2#9)
11. Verify that the PUT sends a Hot Unplug Event Packet with UPG = 1b for each enabled Adapter (4.4.5.2.2#6)
12. Read the following fields from the Adapter Configuration space of each PUT and verify that the following fields have default values (4.4.5.2.2#7)
    a. *Link Credits Allocated* = 0
    b. *Inter-Domain Slave* = 0b
    c. *CL0s Enable* = 0b
    d. *CL1 Enable* = 0b
    e. *CL2 Enable* = 0b
    f. *Lane Bonding* = 0b

TD 4.20 Tx Skew Test

A. Purpose:
   - Verify that the PUT transmitter does not exceed the maximum allowed skew

B. Asserts:
   - 4.2.2.2#7

C. Test Setups
   - H1 (Host)
   - D1 (Device)
   - D3 (Hub UFP)
   - D5 (Hub DFP)

D. Repetitions:
   - Repeat test 10 times

E. Procedure:

USB4 CV performs the following steps:

1. Start Analyzer
2. Reset UUT
3. Enumerate RUT
4. Enable bi-directional Time Sync Handshakes
   a. TSPacketInterval = 16 (HiFi)
   b. EnableUniDIrectionalMode = 0
5. Wait 1 minute
6. Stop Analyzer
7. Parse analyzer trace and verify that skew between Lane 0 and Lane 1 does not exceed LANE_TO_LANE_SKEW (26ns)

Sleep/Wake Tests

TD 4.21 UFP Router Sleep Test (UFP Only)

Note: This test is only performed on the UFP.

A. Purpose:

- Verify that a Router enters sleep state correctly

B. Asserts:

- 4.4.5.1.3#1, 4.4.5.1.3#2
- 4.5.1#6, 4.5.1#9-10, 4.5.1#14
- 4.5.2#1, 4.5.2#3

C. Repetitions:

- *USB4 Port is Inter Domain* bit = 0b; *USB4 Port is Configured* bit =1b; *Enable Wake on Connect* bit = 0b
- *USB4 Port is Inter Domain* bit = 1b; *Enable Wake on Inter-Domain* bit = 1b; *Enable Wake on Connect* bit = 1b
- *USB4 Port is Inter Domain* bit = 0b; *USB4 Port is Configured bit* = 0b
- *USB4 Port is Inter Domain* bit = 1b; *Enable Wake on Inter-Domain bit* = 0b

D. Test Setups

- D1 (Device)
- D3 (Hub)

E. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Reset UUT
2. Perform Lane Initialization
3. Initiate Lane Bonding

Part 1 – Sleep not Enabled

4. Set the *Enter Sleep* bit to 0b
5. Set the *Enable Wake on Connect* bit to 1b
6. Send an LT_LRoff Transaction

   Note: this disconnects the Port

7. Verify that the UUT sends an LT_LRoff Transaction (4.4.5.1.3#1)
8. Verify that the UUT drives SBTX low for at least tDisconnectTx (4.4.5.1.3#2)

Part 2 – Sleep Enabled

9. Configure the *USB4 Port is Inter Domain* bit, *USB4 Port is Configured* bit, *Enable Wake on Connect* bit, and *Enable Wake on Inter-Domain* bit (see repetitions)
10. Set the *Enter Sleep* bit to 1b
11. Poll the *Sleep Ready* bit
12. Verify that the UUT sets the *Sleep Ready* bit to 1b (4.5.1#8)

13. Transition system to sleep
14. If either of the following are true, verify that the UUT drives SBTX low for at least tDisconnectTx (initiates disconnect):
    a. The *USB4 Port is Inter-Domain* bit is 0b, the *USB4 Port is Configured* bit is 0b, and the *Enable Wake on Connect* bit is 0b (4.5.1#9)
    b. The *USB4 Port is Inter-Domain* bit is 1b and the *Enable Wake on Inter-Domain* bit is set to 0b (4.5.1#10)
15. If neither of the above are true, verify that:
    a. UUT sends an LT_LRoff Transaction (4.5.1#12)
    a. UUT Adapters are in the CLd state (4.5.1#14)
    b. UUT is in sleep state (4.5.1#1, 4.5.1#5)
    c. If the *USB4 Port is Inter-Domain* bit is 1b:
        i. Send the UUT an AT Transaction with a Read Command
        ii. Verify that the UUT does not send a response (4.5.2#3)

Part 3 – Configuration Space Verification

16. Wake the host system
17. Read the Path Configuration Space of the PUT and verify all non-zero Paths are 0 (4.5.2#1)

TD 4.22 DFP Router Sleep Test (DFP Only)

Note: This test is only performed on the DFP.

A. Purpose:

- Verify that a Router enters sleep state correctly

B. Asserts:

- 4.4.5.1.3#1, 4.4.5.1.3#2
- 4.5.1#6, 4.5.1#9-10, 4.5.1#14
- 4.5.2#1, 4.5.2#3

C. Repetitions:

- *USB4 Port is Inter-Domain* bit = 0b; *USB4 Port is Configured* bit =1b; *Enable Wake on Connect* bit = 0b
- U*SB4 Port is Inter-Domain* bit = 0b; *USB4 Port is Configured* bit =1b; *Enable Wake on Connect* bit = 1b
- *USB4 Port is Inter-Domain* bit = 0b; USB4 Port is Configured bit = 0b
- *USB4 Port is Inter-Domain* bit = 1b; *Enable Wake on Inter-Domain* bit = 1b
- *USB4 Port is Inter-Domain* bit = 1b; *Enable Wake on Inter-Domain* bit = 0b

D. Test Setups

- H1 (Host)
- D5 (Hub)

E. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Reset UUT
2. Perform Lane Initialization
3. Initiate Lane Bonding

Part 1 – Sleep not Enabled

4. Set the *Enter Sleep* bit to 0b
5. Attempt to transition the UUT to sleep
6. Verify that the UUT does not go into sleep state (4.5.1#6)

Part 2 – Sleep Enabled

7. Configure *USB4 Port is Inter-Domain* bit, *USB4 Port is Configured* bit, *Enable Wake on Connect* bit, and *Enable Wake on Inter-Domain* bit (see repetitions)
8. Set the *Enter Sleep* bit to 1b
9. Poll the *Sleep Ready* bit
10. Verify that the UUT sets the *Sleep Ready* bit to 1b (4.5.1#8)
11. Transition the host system to sleep

12. If either of the following are true, verify that the UUT drives SBTX low for at least tDisconnectTx (initiates disconnect):
    a. The *USB4 Port is Inter-Domain* bit is 0b, the *USB4 Port is Configured* bit is 0b, and the *Enable Wake on Connect* bit is 0b (4.5.1#9)
    b. The *USB4 Port is Inter-Domain* bit is 1b and the *Enable Wake on Inter-Domain* bit is set to 0b (4.5.1#10)
13. If neither of the above are true, verify that:
    a. UUT sends an LT_LRoff Transaction (4.5.1#12)
    b. UUT Adapters are in the CLd state (4.5.1#14)
    c. UUT is in sleep state (4.5.1#1, 4.5.1#5)
    d. If *USB4 Port is Inter-Domain* bit is 1b:
        iii. Send UUT an AT Transaction with a Read Command
        iv. Verify that the UUT does not send a response (4.5.2#3)

Part 3 – Configuration Space Verification

14. Wake the host system
15. Read the Path Configuration Space of the PUT and verify all non-zero Paths are 0 (4.5.2#1)

TD 4.23 Wake on Connect Test (DFP Only)

Note: This test is only performed on the DFP.

A. Purpose:

- Verify that the UUT handles Wake on Connect Events correctly

B. Asserts:

- 4.1.2.2#2
- 4.2.1.2.2#3
- 4.5.3#1, 4.5.3#2
- 4.5.4#3, 4.5.4#5
- 8.2.2.4#21, 8.2.2.4#23-25
- 4.1.2.2#1rt

C. Test Setups

- H1 (Host)
- D5 (Hub)

D. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Reset the UUT
2. Perform Lane Initialization
3. Wait for UUT Adapters to reach CL0 state
4. In the PUT:
    a. Set *Port is Configured* bit to 0b
    b. Set the *Enable Wake on Connect* bit to 1b

Part 1 – Wake on Connect Enabled

5. Tell the tester to connect a USB4 device to the PUT 30 seconds after the host system goes to sleep
6. Transition the host system to sleep:
    a. Set the *Enter Sleep* bit to 1b in the UUT
    b. Wait for the UUT to transition to Sleep state
7. After the USB4 device is connected, verify that:
    a. SBRX goes to logical high for tConnectRX time (4.1.2.2#2, 4.1.2.2#1rt)
    b. Lane Initialization starts on all Lanes (4.5.4#3)
    c. Lane Initialization starts from Phase 2
8. Wait for the UUT Adapters to reach CL0 state.
9. Verify that UUT sends a Hot Plug Event packet with UPG=0b (4.5.4#5)
10. Read the following fields from the Adapter Configuration Space of the DFP and verify:
    a. *Router Detected* is 1 (8.2.2.4#21)
    b. *Wake on Connect Status* bit is 1b (8.2.2.4#23)
11. Tell the tester to disconnect the USB4 device

Part 2 – Wake on Connect Disabled

12. Tell the tester to connect a USB4 device to the PUT 30 seconds after the host system goes to sleep
13. Set the *Enable Wake on Connect* bit to 0b in the DFP
14. Transition the host system to sleep:
    a. Set the *Enter Sleep* bit to 1b in the UUT
    b. Wait for the UUT to transition to Sleep state
15. Wait 1 minute and verify that system does not wake
16. Wake the host system
17. Read the *Wake on Connect Status* bit from the Adapter Configuration Space of the DFP
18. Verify that the *Wake on Connect Status* bit is 0b (8.2.2.4#24, 8.2.2.4#25)

TD 4.24 Wake on Disconnect Test (DFP Only)

Note: This test is only performed on the DFP.

A. Purpose:

- Verify that the UUT handles Wake on Disconnect Events correctly

B. Asserts:

- 4.1.2.2#2
- 4.2.1.2.2#3
- 4.5.3#3, 4.5.3#4
- 4.5.4#1, 4.5.4#3, 4.5.4#5
- 8.2.2.4#22, 8.2.2.4#26-28
- 4.1.2.2#1rt

C. Test Setups

- H1 (Host)
- D5 (Hub)

D. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Reset the UUT
2. Perform Lane Initialization
3. Wait for UUT Adapters to reach CL0 state
4. In the PUT:
    a. Set *Port is Configured* bit to 1b
    b. Set *USB4 Port is Inter-Domain* bit to 0b
    c. Set the *Enable Wake on Disconnect* bit to 1b
5. Tell tester to connect a USB4 Device to the PUT

Part 1 – Wake on Disconnect Enabled

6. Tell the tester to disconnect the USB4 device from the PUT 30 seconds after the host system goes to sleep
7. Transition the host system to sleep:
    a. Set the *Enter Sleep* bit to 1b in UUT
    b. Wait for the UUT to transition to Sleep state
8. After the USB4 device is disconnected, verify that:
    a. SBRX goes to logical high for tConnectRX time (4.1.2.2#2, 4.1.2.2#1rt)
    b. Lane Initialization starts on all Lanes (4.5.4#3)
    c. Lane Initialization starts from Phase 2
9. Wait for the UUT Adapters to reach CL0 state.
10. Verify that UUT sends a Hot Plug Event packet with UPG=0b (4.5.4#5)
11. Read the following fields from PUT Adapter Configuration Space and verify:
    a. *Router Detected* is 0 (8.2.2.4#22)
    b. *Wake on Disconnect Status* bit is 1b (8.2.2.4#26)
12. Tell the tester to re-connect the USB4 device to the PUT

Part 2 – Wake on Disconnect Disabled

13. Set the *Enable Wake on Disconnect* bit to 0b in the PUT
14. Tell the tester to disconnect the USB4 device from the PUT 30 seconds after the host system goes to sleep
15. Transition the host system to sleep:
    a. Set the *Enter Sleep* bit to 1b in the UUT
    b. Wait for the UUT to transition to Sleep state
16. Wait 1 minute and verify that system does not wake
17. Wake system
18. Read the *Wake on Disconnect Status* bit from the Adapter Configuration Space of the PUT
19. Verify that the *Wake on Disconnect Status* bit is 0b (8.2.2.4#27, 8.2.2.4#28)

TD 4.25 Wake on Inter-Domain Event (DFP Only)

Note: This test is only performed on the DFP.

A. Purpose:

- Verify that the UUT handles Wake on Inter-Domain Events correctly

B. Asserts:

- 4.2.1.2.2#3
- 4.5.3#5, 4.5.3#6
- 4.5.4#1, 4.5.4#3, 4.5.4#5
- 8.2.2.4#32-34

C. Test Setups

- H1 (Host)
- D5 (Hub DFP)

D. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Reset the UUT
2. Perform Lane Initialization
3. Wait for the UUT Adapters to reach CL0 state
4. In the PUT:
    a. Set *Port is Inter-Domain* bit to 1b
    b. Set the *Enable Wake on Inter-Domain* bit to 1b
5. Connect a USB4 Host to the PUT

Part 1 – Wake on Inter-Domain Enabled

6. Tell the tester to connect a USB4 host to the PUT 30 seconds after the host system goes to sleep
7. Transition the host system to sleep:
    a. Set the *Enter Sleep* bit to 1b in the UUT
    b. Wait for the UUT to transition to Sleep state
8. After the USB4 host is disconnected, verify that:
    a. SBRX goes to logical low for tWake time (4.5.4#1)
    b. Lane Initialization starts on all Lanes (4.5.4#3)
    c. Lane Initialization starts from Phase 5 (4.2.1.2.2#3)
    d. UUT sends a Hot Plug Event packet with UPG=0b (4.5.4#5)
9. Wait for the UUT Adapters to reach CL0 state.
10. Verify that UUT sends a Hot Plug Event packet with UPG=0b (4.5.4#5)
11. Read the *Wake on Inter-Domain Status* bit from the Adapter Configuration Space of the PUT
12. Verify that the *Wake on Inter-Domain Status* bit is 1b (8.2.2.4#32)
13. Tell the tester to re-connect the USB4 Host to the PUT

Part 2 – Wake on Inter-Domain Disabled

14. Set the *Enable Wake on Inter-Domain* bit to 0b in the PUT
15. Tell the tester to connect a USB4 host to the PUT 30 seconds after the host system goes to sleep

16. Transition the host system to sleep:
    a. Set the *Enter Sleep* bit to 1b in the UUT
    b. Wait for the UUT to transition to Sleep state
17. Wait 1 minute and verify that system does not wake
18. Wake the host system
19. Read the *Wake on Inter-Domain Status* bit from the Adapter Configuration Space of the DFP
20. Verify that the *Wake on Inter-Domain Status* bit is 0b (8.2.2.4#33, 8.2.2.4#34)

TD 4.26 Wake on USB4 Event (DFP Only)

Note: This test is only performed on the DFP.

A. Purpose:

- Verify that the UUT handles Wake on USB4 Events correctly

B. Asserts:

- 4.1.2.2#2
- 4.2.1.2.2#3
- 4.5.3#9
- 4.5.4#1, 4.5.4#3, 4.5.4#5
- 8.2.2.4#29-31
- 4.1.2.2#1rt

C. Test Setups

- H1 (Host)
- D5 (Hub)

D. Procedure:

USB4 CV performs the following steps:

Part 0 – Setup

1. Reset the UUT
2. Perform Lane Initialization
3. Wait for the UUT Adapters to reach CL0 state
4. In the PUT:
    a. Set *Port is Configured* bit to 1b
    b. Set *Port is Inter-Domain* bit to 0b
    c. Set the *Enable Wake on USB4* bit to 1b

Part 1 – Wake on USB4 Enabled

5. Tell the tester to connect a USB4 hub to the PUT
6. Enable wake on connect on the DFPs of the USB4 hub
7. Tell the tester to connect a USB4 device to the DFP of the USB4 hub 30 seconds after the host system goes to sleep
8. Transition the host system to sleep:
    a. Set the *Enter Sleep* bit to 1b in UUT
    b. Wait for the UUT to transition to Sleep state
9. After the USB4 device is connected to the USB4 hub, verify that:
    a. SBRX goes to logical high for tConnectRX time (4.1.2.2#2, 4.1.2.2#1rt)
    b. Lane Initialization starts on all Lanes (4.5.4#3)
    c. Lane Initialization starts from Phase 2
10. Wait for the UUT Adapters to reach CL0 state
11. Verify that UUT sends a Hot Plug Event packet with UPG=0b (4.5.4#5)
12. Read the *Wake on USB4 Wake Status* bit from the Adapter Configuration Space of the DFP
13. Verify that the *Wake on USB4 Wake Status* bit is 1b (8.2.2.4#29)
14. Tell the tester to disconnect the USB4 device from the USB4 Hub (leave the USB4 hub connected to the PUT)

Part 2 – Wake on USB4 Disabled

15. Set the *Enable Wake on USB4* bit to 0b in the PUT
16. Tell the tester to connect a USB4 device to the DFP of the USB4 hub 30 seconds after the host system goes to sleep
17. Transition the host system to sleep:
    a. Set the *Enter Sleep* bit to 1b in the UUT
    b. Wait for the UUT to transition to Sleep state
18. Wait 1 minute and verify that system does not wake
19. Wake the host system
20. Read the *Wake on USB4 Wake Status* bit from the Adapter Configuration Space of the PUT
21. Verify that the *Wake on USB4 Wake Status* bit is 0b (8.2.2.4#30, 8.2.2.4#31)

USB4 Mode Tests – Exerciser Required

The tests in this section are performed in USB4 mode where all connected Ports negotiate and enter USB4 operation as described in the USB Type-C Specification and the USB PD Specification. The Sideband Channel operates as a USB4 Sideband Channel.

Unless specified otherwise, the tests in this section are performed on all Ports of a UUT. The tests are performed at the highest speed that the UUT supports. Lanes are bonded and RS-FEC is enabled.

Unless otherwise noted, a test will timeout if it takes more than 500ms to go from one step to the next step. It is a test failure if a test times out.

Sideband Channel Tests

This section defines the tests that verify that the Sideband Channel of the PUT is compliant with the USB4 Specification.

Background Check

This test is performed by the Exerciser in conjunction with all of the Sideband Channel Tests.

1. Parse each LT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.1#1)
    a. A DLE symbol (FEh)
    b. A LSE symbol
    c. A CLSE symbol
2. Parse the LSE Symbol in each LT Transaction and verify that:
    a. Bits [7:6] (*StartLT*) are set to 10b (4.1.1.2.1#4)
    b. Bit 5 (*LSELane*) is 0 for an LT_LRoff Transaction (4.1.1.2.1#3)
    c. Bit 4 is reserved (0b) (1.7#5)
    d. Bits [3:0] (*LSESymbol*) do not contain reserved values (1.7#1)

    Note: Defined LSESymbol values are 0000b (LT_Fall), 0010b (LT_Resume), and 0011b (LT_LRoff)

3. Parse each AT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.2#1)
    a. A DLE symbol (FEh)
    b. A STX symbol
    c. A DLE symbol (FEh)
    d. No more than 66 Data Symbols (4.1.1.2.2#2)
    e. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5,4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
    f. An ETX symbol (40h)
4. For each AT Command:
    a. Parse the STX Symbol and verify that:
        i. Bits [7:6] (*StartAT*) are 00b (4.1.1.2.2#8)
        ii. Bit 5 is reserved (0b) (1.7#5)
        iii. Bit 4 (*Responder*) is 0b (4.1.1.2.2#7)
        iv. Bit 3 (*Bounce*) is set to 0b (4.1.1.2.2#6)
        v. Bit 2 (*Recipient*) is 1b (4.1.1.2.2#5)
        vi. Bit 1 (*ReturnBounce*) is set to 0b (4.1.1.2.2#4)

b. Parse the Data Symbols and verify that: (4.1.1.3.1#1)
    i. The REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 127 to 255
    ii. The LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
    iii. If WnR=0, there is no COMMAND_DATA
    iv. If WnR=1b, the COMMAND_DATA is the same length as in the LEN field

5. For each AT Response:
    a. Parse the STX Symbol and verify that:
        i. Bits [7:6] (*StartAT*) are 00b (4.1.1.2.2#8)
        ii. Bit 5 is reserved (0b) (1.7#5)
        iii. Bit 4 (*Responder*) is 0b (4.1.1.2.2#7)
        iv. Bit 3 (*Bounce*) is set to 0b (4.1.1.2.2#6)
        v. Bit 2 (*Recipient*) is 1b (4.1.1.2.2#5)
        vi. Bit 1 (*ReturnBounce*) is set to 0b (4.1.1.2.2#4)
    b. Parse the Data Symbols and verify that they consist of the following symbols in the following order: (4.1.1.3.1#2)
        i. A REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 127 to 255
        ii. A LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
        iii. If WnR=0b, RESPONSE_DATA is the same length as in the LEN field (unless test specifies otherwise)
        iv. If WnR=1n, RESPONSE_DATA is 00h (unless test specified otherwise)
    c. Verify that the value in the LEN field is not greater than 64 (4.1.1.3.1#2)

6. When the PUT receives an AT Command with the Recipient bit set to 1b, verify that the PUT responds with an AT Response (unless the test specifies otherwise). (4.1.1.2.2#9)
7. Parse each Broadcast RT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.3.1#1)
    a. A DLE symbol (FEh)
    b. A STX symbol
    c. Two Link Parameters symbols
    d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5,4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
    e. A DLE symbol (FEh)
    f. An ETX symbol (40h)

8. Parse the STX Symbol for a Broadcast RT Transaction and verify that:
    a. *Index* = 0 (4.1.1.2.3.1#4)
    b. *CmdNotResp*=1b (4.1.1.2.3.1#5)

9. Parse Byte 2 of a Broadcast RT Transaction and verify that:
    a. Bits [7:5] are 0 (reserved) (1.7#5)
    b. Bit 4 (*TBTCompatibleSpeed*) is 0b (4.1.1.2.3.1#6)
    c. Bit 1 (reserved) is 0b (1.7#5)
    d. Bit 0 (*USB4*) is 1b (4.1.1.2.3.1#7)

10. Parse each Addressed RT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.3.2#1)
    a. A DLE symbol (FEh)
    b. A STX symbol
    c. No more than 66 Data Symbols (4.1.1.2.3.2#2)
    d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5-#9)
    e. A DLE symbol (FEh)
    f. An ETX symbol (40h)

11. Parse each RT Command and verify that: (4.1.1.3.1#1)
    a. The REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 127 to 255
    b. The LEN symbol does not contain a value greater than 64
    c. If WnR=0, there is no COMMAND_DATA
    d. If WnR=1b, the COMMAND_DATA is the same length as in the LEN field
12. Parse each RT Response and verify that it consists of the following symbols in the following order: (4.1.1.3.1#2)
    a. The REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 127 to 255
    b. The LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
    c. If WnR=0b, RESPONSE_DATA is the same length as in the LEN field (unless test specifies otherwise)
    d. If WnR=1n, RESPONSE_DATA is 00h (unless test specified otherwise)
13. Verify that the PUT sends an AT Response within tCmdResponse (50ms) of receiving an AT Command. (4.1.1.2.5.1#1)
14. Verify that the PUT sends an Addressed RT Response within tCmdResponse (50ms) of receiving an Addressed RT Command. (4.1.1.2.5.2#1)

Transaction Tests

TD 4.27 Invalid CLSE Test

A. Purpose:

- Verify that the PUT checks CLSE symbols
- Verify that the PUT drops a Transaction with an invalid CLSE

B. Asserts:

- 4.1.1.2.1#5, 4.1.1.2.1#6

C. Test Setups
- H3 (Host)
- D2 (Device)
- D4 (Hub UFP)
- D6 (Hub DFP)

D. Procedure:

Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined "Upstream of the UUT" and the test steps that are defined "On the PUT". When this test is performed on a DFP, USB4 CV performs the tests steps that are defined "Upstream of the UUT" and the Exerciser performs the test steps that are defined "On the PUT".

Upstream of the UUT:

Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding

On the PUT:

Part 1 – Lane 1 Adapter

4. Send an LT_Fall Transaction to the PUT
    a. Transaction targets the Lane 1 Adapter
    b. Transaction has an invalid CLSE
5. Verify that the Lane 1 Adapter stays in the CL0 state (4.1.1.2.1#5, 4.1.1.2.1#6)

Part 2 – Lane 0 Adapter

6. Send an LT_Fall Transaction to the PUT
    a. Transaction targets the Lane 0 Adapter
    b. Transaction has an invalid CLSE
7. Verify that SBTX in the PUT stays high (4.1.1.2.1#5, 4.1.1.2.1#6)
8. Verify that the Lane 0 Adapter stays in the CL0 state (4.1.1.2.1#5, 4.1.1.2.1#6)

TD 4.28 Multiple DLE Test

A. Purpose:

- Verify that the PUT correctly handles AT and RT Transactions with multiple preceding DLE symbols

B. Asserts:

- 4.1.1.2.4#2

C. Test Setups

- H3 (Host)
- D2 (Device)
- D4 (Hub UFP)
- D6 (Hub DFP)

D. Repetitions:

- Repeat with AT Transactions
- Repeat with Addressed RT Transactions with the following:
  - *Index* = 0
  - *Index* = First On-Board Re-timer (if present)
  - *Index* = Second On-Board Re-timer (if present)
- Repeat both Transaction types with 2 DLE symbols and 10 DLE symbols

E. Procedure:

Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined "Upstream of the UUT" and the test steps that are defined "On the PUT". When this test is performed on a DFP, USB4 CV performs the tests steps that are defined "Upstream of the UUT" and the Exerciser performs the test steps that are defined "On the PUT".

Upstream of the UUT:

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding

On the PUT:

4. Send the DLE symbols to the PUT (see repetitions)
5. Immediately after sending the DLE symbols, send the PUT a Write Command with the following:
   a. *Target* = Register 9 (Metadata)
   b. *Length* = 4
   c. *Command Data* = FFFF FFFFh
6. Wait for a Write Response from the PUT
7. Send the PUT a Read Command with the following:
   d. *Target* = Register 9 (Metadata)
   e. *Length* = 4
8. Verify that the contents of Register 9 are FFFF FFFFh (4.1.1.2.4#2)

TD 4.29 Transaction Error Test

A. Purpose:

- Verify that the PUT ignores AT Transactions and Addressed RT Transactions that don't have data and CRC fields.
- Verify that the PUT ignores symbols that are not part of a Transaction
- Verify that the PUT ignores AT Transactions and Addressed RT Transactions with an invalid CRC

B. Asserts:

- 4.1.1.2.6#1-4

B. Test Setups

- H3 (Host)
- D2 (Device)
- D4 (Hub UFP)
- D6 (Hub DFP)

C. Repetitions:

- Repeat with AT Transactions
- Repeat with Addressed RT Transactions with the following:
  - Index = 0
  - Index = First On-Board Re-timer (if present)
  - Index = Second On-Board Re-timer (if present)

D. Procedure:

Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined "Upstream of the UUT" and the test steps that are defined "On the PUT". When this test is performed on a DFP, USB4 CV performs the tests steps that are defined "Upstream of the UUT" and the Exerciser performs the test steps that are defined "On the PUT".

Upstream of the UUT:

Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding

On the PUT:

Part 1 – Malformed Command

4. Send the PUT a Write Command with No data symbols and no CRC
5. Verify that the PUT does not send a response (4.1.1.2.6#2)
6. Send the PUT a Read Command with no data symbols and no CRC
7. Verify that the PUT does not sent a response (4.1.1.2.6#2)

Part 2 – Extra Preceding Symbols

8. Send the PUT a series of 10 extra symbols followed by a Write Command

a. *Target* = Register 18 (Data)
b. COMMAND_DATA = FF … FFh
c. Extra symbols are random data (excluding FEh symbol)

9. Verify that the PUT sends a Write Response for the Write Command (4.1.1.2.6#3)
10. Verify that the PUT does not send any other responses (4.1.1.2.6#4)
11. Send the PUT a series of 10 extra symbols followed by a Read Command
    a. *Target* = Register 18 (Data)
    b. Extra symbols are random data (excluding FEh symbol)
12. Verify that the PUT sends a Read Response with RESPONSE_DATA = FF … FFh (4.1.1.2.6#3)
13. Verify that the PUT does not send any other responses (4.1.1.2.6#4)

Part 3 – Bad CRC

14. Send the PUT a Write Command
    a. *Target* = Register 18 (Data)
    b. CRC is invalid
    c. COMMAND_DATA = 00 … 00h
15. Verify that the PUT does not send a Write Response (4.1.1.2.6#1)
16. Send the PUT a Read Command
    a. *Target* = Register 18 (Data)
    b. CRC is valid
17. Wait for the PUT to send a Read Response
18. Verify that the value of the RESPONSE_DATA in the Read Response is the same as what was written in Part 2 (FF … FFh) (4.1.1.2.6#1)

TD 4.30 SB Register Read Error Test

A. Purpose:

- Verify that the PUT correctly handles Read Request error cases

B. Asserts:

- 4.1.1.3.1#6-10

C. Test Setups

- H3 (Host)
- D2 (Device)
- D4 (Hub UFP)
- D6 (Hub DFP)

D. Repetitions:

- Repeat with AT Transactions
- Repeat with Addressed RT Transactions with the following:
  - *Index* = 0
  - *Index* = First On-Board Re-timer (if present)
  - *Index* = Second On-Board Re-timer (if present)

E. Procedure:

Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined "Upstream of the UUT" and the test steps that are defined "On the PUT". When this test is performed on a DFP, USB4 CV performs the tests steps that are defined "Upstream of the UUT" and the Exerciser performs the test steps that are defined "On the PUT".

Upstream of the UUT:

Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding

On the PUT:

Part 1 – Malformed Command (Too Short)

4. Send the PUT a Read Command with a Single Data Symbol
5. Verify that the PUT responds with a Read Response with:
   a. No RESPONSE_DATA (4.1.1.3.1#6)
   b. LEN = 0 (4.1.1.3.1#6)

Part 2 – Invalid Target

6. Send the PUT a Read Command that targets an undefined register
7. Verify that the PUT responds with a Read Response with:
   a. No RESPONSE_DATA (4.1.1.3.1#7)
   b. LEN = 0 (4.1.1.3.1#7)

Part 3 – Malformed Command (Too Long)

8. Send the PUT a Read Command
    a. COMMAND_DATA = FFh
    b. LEN = 3
9. Verify that the PUT responds with a Read Response with:
    a. No RESPONSE_DATA (4.1.1.3.1#8)
    b. LEN = 0 (4.1.1.3.1#8)

Part 4 – Long Read (Read > Register Length)

10. Send the PUT a Read Command
    a. *Target* = register 1 (Device ID)
    b. LEN = 4
11. Record the RESPONSE_DATA returned in the Read Response
12. Send the PUT a Read Command
    a. *Target* = Register 1
    b. LEN = 5
13. Verify that the PUT responds with a Read Response with:
    a. RESPONSE_DATA = same a recorded in Step 10 (4.1.1.3.1#9)
    b. LEN = 4 (4.1.1.3.1#9)

Part 5 – Short Read (Read < Register Length)

14. Send the PUT a Read Command
    a. *Target* = Register 1 (Device ID)
    b. LEN = 4
15. Record the RESPONSE_DATA returned in the Read Response
16. Send the PUT a Read Command
    a. *Target* = Register 1 (Device ID)
    b. LEN = 3
17. Verify that the PUT sends a Read Response with:
    a. RESPONSE_DATA = the first 3 bytes of Register 1 as recorded in Step 16 (4.1.1.3.1#10)
    b. LEN = 4 (4.1.1.3.1#10)

Lane Initialization Tests

Note: The tests in this section are performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.

TD 4.31 Phase 4 Exit Test

A. Purpose:
- Verify that the PUT Transitions out of Phase 4 correctly under all conditions

B. Asserts:
- 4.1.2.4#1, 4.1.2.4#2

C. Test Setups
- H3 (Host)
- D2 (Device)
- D4 (Hub UFP)
- D6 (Hub DFP)

D. Procedure:

The Exerciser performs the following steps:

Part 0 – Setup

1. Drive SBTX to logic low (which will restart Lane Initialization)
2. Perform Lane Initialization through phase 3

Part 1 – Broadcast RT Transaction Last

3. Verify that the PUT sends a Broadcast RT Transaction every tLaneParams (4.1.2.4#1)
4. Wait for both to be true:
    a. At least tLTPhase4 time passed after completing Phase 2
    b. PUT sent at least 2 Broadcast RT Transactions
5. Send a Broadcast RT Transaction
6. Verify that the PUT stops sending Broadcast RT Transactions (4.1.2.4#2)
7. Finish Lane Initialization

Part 2 - Broadcast RT Transaction First

8. Drive SBTX to logic low (which will restart Lane Initialization)
9. Perform Lane initialization through phase 3
10. Send a Broadcast RT Transaction immediately after entering phase 3 (before tLTPhase4 time has passed)
11. Verify that the PUT continues to send a Broadcast RT Transaction every tLaneParams until the following are true: (4.1.2.4#2)
    a. PUT sent at least 2 Broadcast RT Transactions
    b. At least tLTPhase4 time has passed
12. Verify that the PUT stops sending Broadcast RT Transactions (4.1.2.4#2)
13. Finish Lane Initialization

Adapter State Tests

Unless noted otherwise, the tests in this section are performed at Gen 2 speed and repeated at Gen 3 speed (if Gen 3 speed is supported).

Note: The tests in this section are performed simultaneously for both the Lane 0 Adapter and the Lane 1 Adapter of the Port being tested.

TD 4.32 Training Delay Test

A. Purpose:
- Verify that the PUT handles a Link Training delay correctly

B. Asserts:
- 4.2.1.3.2#1
- 4.2.1.4.3#6

C. Test Setups
- H3 (Host)
- D2 (Device)
- D4 (Hub UFP)
- D6 (Hub DFP)

D. Procedure:

The Exerciser performs the following steps:

Part 1 – TS1 delay

1. Drive SBTX to logic low (which will restart Lane Initialization)
2. Start Lane Initialization
3. After receiving the first SLOS1 from the PUT, start a timer that counts up from 0 in increments of 1ms
4. When the PUT starts sending TS1 OS, continue sending SLOS2 until the timer reaches 900ms (tTrainingAbort1 - tTrainingAbort2)
5. Resume Lane Initialization (send TS1 OS)
6. Verify that PUT completes Lane Initialization (4.2.1.3.2#1)

Part 2 – TS2 delay

7. Reset UUT
8. Start Lane Initialization
9. After receiving the first SLOS1 from the PUT, start a timer that counts up from 0 in increments of 1ms. When the PUT starts sending TS2 OS, continue sending TS1 OS until the timer reaches 900ms (tTrainingAbort1 - tTrainingAbort2)
10. Resume Lane Initialization (send TS2 OS to PUT)
11. Verify that the PUT transitions to CL0 state (4.2.1.3.2#1)
12. Finish Lane Initialization

Part 3 – TS1→Lock2

13. Reset UUT
14. Start Lane Initialization
15. Continue sending SLOS2 until PUT starts sending TS1 OS
16. Send PUT one TS1 OS, then send SLOS1

Note: When RS-FEC is on, the first n SLOS1 symbols will be RS-FEC encoded (at Gen 2 speed, 32=<n<=64; at Gen 3 speed, 16=<n<=32). After sending n SLOS symbols, RS-FEC is turned off.

17. Verify that the PUT sends SLOS2 (4.2.1.3.2#1, 4.2.1.4.3#6)
18. Finish Lane Initialization

Part 4 – TS2→Lock2

19. Reset UUT
20. Start Lane Initialization
21. Continue sending TS1 OS until PUT starts sending TS2 OS
22. Send PUT one TS2 OS, then send SLOS1

Note: When RS-FEC is on, the first n SLOS1 symbols will be RS-FEC encoded (at Gen 2 speed, 32=<n<=64; at Gen 3 speed, 16=<n<=32). After sending n SLOS symbols, RS-FEC is turned off.

23. Verify that the PUT sends SLOS2 (4.2.1.3.2#1, 4.2.1.4.3#6)
24. Finish Lane Initialization

TD 4.33 Training Fail Test

A. Purpose:
   - Verify that the PUT handles Link Training failure correctly

B. Asserts:
   - 4.2.1.3.2#1
   - 4.2.1.3.3#4
   - 4.2.1.4.3#6
   - 4.2.1.2.2#4

C. Test Setups
   - H3 (Host)
   - D2 (Device)
   - D4 (Hub UFP)
   - D6 (Hub DFP)

D. Procedure:

The Exerciser performs the following steps:

Part 1 – Lock Failure

1. Drive SBTX to logic low (which will restart Lane Initialization)
2. Perform Lane Initialization
3. When PUT starts sending TS1 OS, continue sending SLOS2
4. Wait tTrainingAbort1 time
5. Verify that the PUT transitions to the CLd state (4.2.1.3.2#1)
6. Verify that the PUT starts Lane Initialization from Phase 1 (4.2.1.2.2#4)

Part 2 – TS2 Failure

7. When PUT starts sending TS2 OS, continue sending TS1
8. Wait tTrainingAbort1 time
9. Verify that the PUT transitions to the CLd state (4.2.1.3.2#1)
10. Verify that the PUT starts Lane Initialization from Phase 1 (4.2.1.2.2#4)

Part 3 – Failure After CL0

11. Complete Lane Initialization (PUT Adapters are in CL0 state)
12. Start sending SLOS1 Symbols
13. Verify that the PUT Adapters transition to Training state (4.2.1.4.3#6)
14. Continue sending back-to-back SLOS1 for tTrainingAbort2 time
15. Verify that the PUT restarts Lane Initialization (4.2.1.3.3#4)
16. Verify that the PUT starts Lane Initialization from Phase 1 (4.2.1.2.2#4)

TD 4.34 Bonding Delay Test

A. Purpose:
- Verify that the PUT handles delay in Bonding State correctly

B. Asserts:
- 4.2.1.5.2#1

C. Test Setups
- H3 (Host)
- D2 (Device)
- D4 (Hub UFP)
- D6 (Hub DFP)

D. Procedure:

Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined "Upstream of the UUT" and the test steps that are defined "On the PUT". When this test is performed on a DFP, USB4 CV performs the tests steps that are defined "Upstream of the UUT" and the Exerciser performs the test steps that are defined "On the PUT".

Upstream of the UUT:

Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding

On the PUT:

Part 1 – TS1 delay

4. When PUT starts sending TS2 OS, continue sending TS1 OS for 80 us (tBonding – 20 us)
5. Resume Lane Bonding (send TS2 OS to PUT)
6. Verify that the PUT starts sending TS2 OS (4.2.1.5.2#1)
7. Finish Lane Initialization

Part 2 – TS1→Lock2

8. Drive SBTX to logic low (which will restart Lane Initialization)
9. Complete Lane Initialization
10. Send TS1 OS to initiate Lane Bonding.
11. When PUT starts sending TS1 OS, send SLOS1
12. Verify that the PUT sends SLOS2 (4.2.1.5.2#1)
13. Finish Lane Initialization

Part 3 – TS2→Lock2

14. Drive SBTX to logic low (which will restart Lane Initialization)
15. Start Lane Initialization
16. Set *Lane Bonding* bit to 1b in PUT to initiate Lane bonding
17. When PUT starts sending TS2 OS, send SLOS1
18. Verify that the PUT sends SLOS2 (4.2.1.5.2#1)
19. Finish Lane Initialization

TD 4.35 Bonding Fail Test

A. Purpose:
   - Verify that the PUT initiates a disconnect when Lane bonding fails

B. Asserts:
   - 4.2.2.2#6

C. Test Setups
   - H3 (Host)
   - D2 (Device)
   - D4 (Hub UFP)
   - D6 (Hub DFP)

D. Procedure:

Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined "Upstream of the UUT" and the test steps that are defined "On the PUT". When this test is performed on a DFP, USB4 CV performs the tests steps that are defined "Upstream of the UUT" and the Exerciser performs the test steps that are defined "On the PUT".

Upstream of the UUT:

Part 0 – Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding

On the PUT:

Part 1 – No TS OS

4. When PUT sends TS1 OS, send SLOS1
5. Continue sending SLOS1 for at least tBonding time so that bonding fails
6. Verify that the PUT drives SBTX to logic Low for at least tDisconnect (4.2.2.2#6)
7. Perform Lane Initialization

Part 2 – Incorrect TS OS

8. Send 3 TS1 OS with Lane Bonding Target = 001b to initiate Lane Bonding.
9. Send TS1 OS with Lane Bonding Target = 000b to both Adapters
10. Continue sending TS1 for at least tBonding time so that bonding fails
11. Verify that the PUT drives SBTX to logic Low for at least tDisconnect (4.2.2.2#6)
12. Perform Lane Initialization

Part 3 – CL0 timeout

13. Send 3 TS1 OS with Lane Bonding Target = 001b to initiate Lane Bonding
14. Send TS1 OS with Lane Bonding Target = 00b to the Lane 1 Adapter:
    a. Send TS1 OS with Lane Bonding Target = 001b to the Lane 0 Adapter
15. Continue sending TS1 OS for at least tBonding time so that Bonding fails
16. Verify that the PUT drives SBTX to logic Low for at least tDisconnect (4.2.2.2#6)

TD 4.36 TS1/TS2 Bits Ignored Test

A. Purpose:
- Verify that the PUT ignores reserved bits in TS1 and TS2 Ordered Sets

B. Asserts:
- 4.2.1.3.5#2, 4.2.1.3.5#5, 4.2.1.3.5#7, 4.2.1.3.5#9-10

C. Repetitions:
- Repeat for the following bits in the TS1 and TS2 Ordered Sets:
  - 47:32 (4.2.1.3.5#5)
  - 31:29 (4.2.1.3.5#7)
  - 28:26 (4.2.1.3.5#9)
  - 25:16 (4.2.1.3.5#10)

B. Test Setups
- H3 (Host)
- D2 (Device)
- D4 (Hub UFP)
- D6 (Hub DFP)

D. Procedure:

The Exerciser performs the following steps:

1. Drive SBTX to logic low (which will restart Lane Initialization)
2. Perform Lane Initialization
3. During Training state, send the PUT TS1 and TS2 Ordered Sets with different values in bits 63:59 (see repetitions)
4. Verify that Lane Initialization completes without error (4.2.1.3.5#2)

TD 4.37 CLx Entry Errors Test

Note: This test is not performed if the Router does not support CLx states.

A. Purpose:
   - Verify that the PUT handles errors while entering low power states

B. Asserts:
   - 4.2.1.6.2#38

C. Test Setups
   - H3 (Host)
   - D2 (Device)
   - D4 (Hub UFP)
   - D6 (Hub DFP)

D. Repetitions:
   - Repeat for all supported CLx states

E. Procedure:

Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined "Upstream of the UUT" and the test steps that are defined "On the PUT". When this test is performed on a DFP, USB4 CV performs the tests steps that are defined "Upstream of the UUT" and the Exerciser performs the test steps that are defined "On the PUT".

Upstream of the UUT:

Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Enable CLx states
   a. If testing CL2 state, enable all CLx states
   b. If testing CL1 state or CL0s state, enable all CLx states except CL2 state
5. Configure objections
   a. If testing CL2 state, configure no objections to CL2
   b. If testing CL1 state, configure no objections to CL1
   c. If testing CL0s state, configure objection to CL1
6. Configure both PUT Adapters with *PM Secondary* = 1b
7. Tell Exerciser to perform the test

On the PUT:

Part 1 – Link Error

8. Send the PUT back-to-back CL2_REQ
9. Wait for the PUT to send Response Ordered Set
   a. If testing CL2, Response Ordered Set = CL2_ACK
   b. If testing CL1, Response Ordered Set = CL1_ACK
   c. If testing CL0s, Response Ordered Set = CL0s_ACK
10. After receiving the first Response Ordered Set from the PUT, send 2 unknown Ordered Sets
11. Verify that the PUT does not enter Training state (4.2.1.6.2#38)
12. Verify that the PUT finishes the transition to the target CLx state

TD 4.38 CL0s Exit Errors Test

Note: This test is not performed if the Router does not support CL0s state.

A. Purpose:
   - Verify that the PUT handles errors while exiting CL0s state

B. Asserts:
   - 4.2.1.6.5.1#13, 4.2.1.6.5.1#17

C. Test Setups
   - H3 (Host)
   - D2 (Device)
   - D4 (Hub UFP)
   - D6 (Hub DFP)

D. Repetitions:
   - Repeat for all supported CLx states

E. Procedure:

The Exerciser performs the following steps:

Part 0 - Setup

1. Drive SBTX to logic low (which will restart Lane Initialization)
2. Perform Lane Initialization
3. Wait for PUTs to reach CL0 state
4. Transition PUTs to CL0s state

Part 1 –tCL0sSwitch Timeout

5. Initiate exit from CL0s state
   a. Send LFPS burst on all Lanes for 16 LFPS cycles
   b. Return to electrical idle for tPreData
   c. Send a CL_WAKE1.X Ordered Set Symbol
   d. Do not send any SLOS or CL_WAKE symbols
6. Wait tCL0sSwitch time
7. Verify that the PUT does not transition to the Training.LOCK1 substate if the time between CL_WAKE1.X and CL_WAKE1.(X+1) is less than 500us (4.2.1.6.5.1#13)

Part 2 – tTS2Timeout Timeout

8. Transition PUT to CL0s state
9. Initiate exit from CL0s state:
   a. Send LFPS burst on all Lanes for 16 LFPS cycles
   b. Return to electrical idle for tPreData
   c. Send 3 back-to-back SLOS symbols
   d. Continue sending SLOS after PUT sends TS2
10. Wait tTS2Timeout time
11. Verify that the PUT transitions to the Training state (4.2.1.6.5.1#17)

Lane 0/Lane 1 Tests

Unless specified otherwise, the tests in this section are performed on all Ports of a UUT. The tests are performed at the highest speed that the UUT supports. Lanes are bonded and RS-FEC is enabled.

Background Check

This test is performed by the Exerciser in conjunction with all of the Lane 0/Lane 1 Tests.

1. Parse each TSI and TS2 Ordered Set and verify that bits 31:29 (Rsvd) are 0. (4.2.1.3.5#6)
2. When an Adapter transitions to the CL0 state and Lanes are not bonded, verify that the first bytes transmitted after the last TS2 Ordered Set are either a Transport Layer Packet header or an Ordered Set that is not SLOS, TS1, or TS2. (4.4.1#1)
3. When an Adapter transitions to the CL0 state and Lanes are bonded, verify that the first bytes transmitted after the last TS2 Ordered Set are a de-skew Ordered Set followed by either a Transport Layer Packet header, an Idle Packet or any Ordered Set other than SLOS, TS1 or TS2. (4.4.1#2)
4. When operating with a Dual-lane Link, verify that, if one Lane transitions to Training State, other Lane also transitions to training state (4.2.2.2#8)

Link Tests

Unless noted otherwise, the tests in this section are performed at Gen 2 speed and repeated at Gen 3 speed (if Gen 3 speed is supported).

TD 4.39 RS-FEC Correctable Error Test (Hubs Only)

Note: This test is only performed on DFP.

A. Purpose:

- Verify that the PUT can correct up to two 1-byte errors in an RS-FEC block

B. Asserts:

- 4.3.6#13

C. Test Setups

- D6 (Hub DFP)

D. Procedure:

USB4 CV performs the following steps:

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Setup a Host Interface Loopback Path
5. Send 10 Host Interface Tunneled Packets on the Loopback Path
6. Verify that the Host Interface Tunneled Packets are received back on the Loopback Path without error and that the data received on the Loopback Path is the same as what was sent out. (4.3.6#13)

The Exerciser does the following while the test is being performed:

- After Lane Bonding is complete, inject randomly spaced errors so that either one or two errors fall within an RS-FEC block
- Perform Loopback function (i.e. return any received Tunneled Packets back to the USB4 Host)

TD 4.40 Unknown Ordered Set Link Error Test

A. Purpose:

- Verify that the PUT detects and reports Link errors correctly

B. Asserts:

- 4.2.1.3.1#2
- 4.2.1.4.3#5
- 4.2.2.2.1#1
- 4.4.2#1-4, 4.4.2#9-12

C. Test Setups

- H3 (Host)
- D2 (Device)
- D4 (Hub UFP)
- D6 (Hub DFP)

D. Repetitions:

- Repeat with Adapters in all states (4.4.2#4)
- Repeat for Lane 1 Adapter and Lane 0 Adapter

E. Procedure:

Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined "Upstream of the UUT" and the test steps that are defined "On the PUT". When this test is performed on a DFP, USB4 CV performs the tests steps that are defined "Upstream of the UUT" and the Exerciser performs the test steps that are defined "On the PUT".

Upstream of the UUT:

Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Write 1b to each bit in the *Logical Layer Errors Enable* field in Adapter Configuration Space
5. Read the value of the *Logical Layer Errors Enable* field in Adapter Configuration Space
    a. If a bit is 1b, then PUT supports that error
    b. If a bit is 0b, the PUT does not support that error
6. Verify that the PUT supports Ordered Set Errors (4.4.2#1)
7. Verify that each PUT reports the same supported errors (4.4.2#3)

Part 1 – Ordered Set Errors – Unknown OS

8. Configure PUT with the OSE bit in the *Logical Layer Errors Enable* field set to 0b
9. Read the *Logical Layer Errors* field to clear and previous errors

On the PUT:

10. Send the PUT 2 back-to-back Ordered Sets with unknown contents
11. Verify that:
    a. Both Adapters entered Training.LOCK1 sub-state (i.e. sent SLOS1) (4.2.2.2.1#1, 4.2.1.3.1#2, 4.2.1.4.3#5, 4.4.2#9)
    b. PUT transitioned to CL0 state within tTrainingAbort2 after entering the Training.LOCK1 sub-state (4.2.1.3.3#3)

Upstream of the UUT:

12. Verify that the PUT:
    a. Sets the OSE bit in *Logical Layer Errors* field to 1b (4.4.2#10)
    b. Does not send a Notification Packet (4.4.2#12)
13. Configure PUT with the OSE bit in the *Logical Layer Errors Enable* field set to 1b
14. Read the *Logical Layer Errors* field to clear and previous errors

On the PUT:

15. Send the PUT 2 back-to-back Ordered Sets with unknown contents
16. Verify that:
    a. The PUT Adapters go to Training.LOCK1 sub-state (i.e. sent SLOS1) (4.2.1.3.1#2, 4.2.1.4.3#5, 4.4.2#9)
    b. PUT transitioned to CL0 state within tTrainingAbort2 after entering the Training.LOCK1 sub-state (4.2.1.3.3#3)

Upstream of the UUT:

17. Verify that the PUT:
    a. Sets the OSE bit in *Logical Layer Errors* field to 1b (4.4.2#10)
    b. Sends a Notification Packet with Event Code = ERR_LINK (4.4.2#11)

TD 4.41 Uncorrectable SCR Link Error Test

A. Purpose:

- Verify that the PUT detects and reports Link errors correctly

B. Asserts:

- 4.2.1.3.1#2
- 4.2.1.4.3#5
- 4.2.2.2.1#1
- 4.4.2#4, 4.4.2#9-12

C. Test Setups

- H3 (Host)
- D2 (Device)
- D4 (Hub UFP)
- D6 (Hub DFP)

D. Repetitions:

- Repeat with Adapters in all states (4.4.2#4)
- Repeat for Lane 1 Adapter and Lane 0 Adapter

E. Procedure:

Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined "Upstream of the UUT" and the test steps that are defined "On the PUT". When this test is performed on a DFP, USB4 CV performs the tests steps that are defined "Upstream of the UUT" and the Exerciser performs the test steps that are defined "On the PUT".

Upstream of the UUT:

Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Write 1b to the OSE bit in the *Logical Layer Errors Enable* field in Adapter Configuration Space

Part 1 – Ordered Set Errors – Uncorrectable SCR

5. Reset UUT
6. Wait for PUTs to reach CL0 state
7. Configure PUT with the OSE bit in the *Logical Layer Errors Enable* field set to 0b
8. Read the *Logical Layer Errors* field to clear and previous errors

On the PUT:

9. Send the PUT 2 back-to-back Ordered Sets with an uncorrectable error in the SCR field
10. Verify that :
    a. The PUT Adapters go to Training.LOCK1 sub-state (i.e. sent SLOS1) (4.2.1.3.1#2, 4.2.1.4.3#5, 4.4.2#9)
    b. Both Adapters entered Training state (4.2.2.2.1#1)
    c. PUT transitioned to CL0 state within tTrainingAbort2 after entering the Training.LOCK1 sub-state (4.2.1.3.3#3)

Upstream of the UUT:

11. Verify that the PUT:
    a. Sets the OSE bit in *Logical Layer Errors* field to 1b (4.4.2#10)
    b. Does not send a Notification Packet (4.4.2#12)
12. Configure PUT with the OSE bit in the *Logical Layer Errors Enable* field set to 1b
13. Read the *Logical Layer Errors* field to clear and previous errors

On the PUT:

14. Send the PUT 2 back-to-back Ordered Sets with unknown contents
15. Verify that:
    a. The PUT Adapters go to Training.LOCK1 sub-state (i.e. sent SLOS1) (4.2.1.3.1#2, 4.2.1.4.3#5, 4.4.2#9)
    b. PUT transitioned to CL0 state within tTrainingAbort2 after entering the Training.LOCK1 sub-state (4.2.1.3.3#3)

Upstream of the UUT:

16. Verify that the PUT:
    a. Sets the OSE bit in *Logical Layer Errors* field to 1b (4.4.2#10)
    b. Sends a Notification Packet with Event Code = ERR_LINK (4.4.2#11)

TD 4.42 Timeout Link Error Test

A. Purpose:

- Verify that the PUT detects and reports Link errors correctly

B. Asserts:

- 4.4.2#4, 4.4.2#14-16

C. Test Setups

- H3 (Host)
- D2 (Device)
- D4 (Hub UFP)
- D6 (Hub DFP)

D. Repetitions:

- Repeat with Adapters in all states (4.4.2#4)
- Repeat for Lane 1 Adapter and Lane 0 Adapter

E. Procedure:

Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined "Upstream of the UUT" and the test steps that are defined "On the PUT". When this test is performed on a DFP, USB4 CV performs the tests steps that are defined "Upstream of the UUT" and the Exerciser performs the test steps that are defined "On the PUT".

Upstream of the UUT:

Part 0 - Setup

1. Reset UUT
2. Enumerate UUT Router
3. Initiate Lane Bonding
4. Write 1b to the TE bit in the *Logical Layer Errors Enable* field in Adapter Configuration Space
5. Read the value of the *Logical Layer Errors Enable* field in Adapter Configuration Space
    a. If the TE bit is 1b (PUT supports TE errors), continue to Part 1
    b. If the TE bit is 0b (PUT does not support TE errors), end test here

Part 1 – Timeout Errors

6. Reset UUT
7. Wait for PUTs to reach CL0 state
8. Configure PUT with the TE bit in the *Logical Layer Errors Enable* field set to 0b
9. Read the *Logical Layer Errors* field to clear and previous errors

On the PUT:

10. Transition the PUT to Training state and only send TS1 to the PUT (to prevent transition to CL0 state)

Upstream of the UUT:

11. Wait for PUT to disconnect, then reconnect and complete Link Initialization.

12. Verify that the PUT:
    a. Sets the TE bit in the *Logical Layer Errors* field to 1b (4.4.2#14)
    b. Does not send a Notification Packet (4.4.2#16)
13. Configure PUT with the TE bit in the *Logical Layer Errors Enable* field set to 1b
14. Read the *Logical Layer Errors* field to clear and previous errors

On the PUT:

15. Transition the PUT to Training state and only send TS1 to the PUT (to prevent transition to CL0 state)

Upstream of the UUT:

16. Wait for PUT to disconnect, then reconnect and complete Link Initialization.
17. Verify that the PUT:
    a. Sets the TE bit in the *Logical Layer Errors* field to 1b (4.4.2#14)
    b. Sends a Notification Packet with Event Code = ERR_LINK (4.4.2#15)

TD 4.43 Rx De-Skew Test

A. Purpose:

- Verify that the PUT receiver can operate with maximum skew

B. Asserts:

- 4.4.4#1

C. Test Setups

- H3 (Host)
- D2 (Device)
- D4 (Hub UFP)
- D6 (Hub DFP)

D. Repetitions:

- Repeat test 5 times with Lane 0 skewed ahead of Lane 1
- Repeat test 5 times with Lane 1 skewed ahead of Lane 0

E. Procedure:

Note: Throughout this test, the Exerciser inserts a static skew between Lane 0 and Lane 1 of up to 44ns on the Link with the UUT.

Note: When performing this test on an UFP, the exerciser performs both the test steps that are defined "Upstream of the UUT". When this test is performed on a DFP, USB4 CV performs the tests steps that are defined "Upstream of the UUT".

Upstream of the UUT:

1. Reset UUT to start Lane Initialization
2. Set bit 4 in the *Logical Layer Errors Enable* field to 1b to enable De-Skew Buffer Error reporting.
3. Initiate Lane Bonding
4. Wait 5 seconds
5. Read bit 4 in the *Logical Layer Errors* field
6. Verify that bit 4 in the *Logical Layer Errors* field is 0b (i.e. there are no De-Skew Buffer errors) (4.4.4#1)
7. Verify that Lane Initialization completes successfully for both Lane 0 and Lane 1 (4.4.4#1)

TBT3-Compatibility Tests – No Exerciser

The tests in this section are performed in TBT3-Compatible mode where all connected Ports negotiate and enter TBT3-Compatible operation as described in the USB Type-C Specification and the USB PD Specification.

Unless specified otherwise, the tests in this section are performed on all Ports of a UUT. The tests are performed at the highest speed that the UUT supports. Lanes are bonded and RS-FEC is enabled.

Unless otherwise noted, a test will timeout if it takes more than 500ms to go from one step to the next step. It is a test failure if a test times out.

Sideband Channel Tests

This section defines the tests that verify that the Sideband Channel of the PUT is compliant with the USB4 Specification.

Background Check

This test is performed by the Analyzer in conjunction with all of the Sideband Channel Tests.

1. Parse each LT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.1#1)
    a. A DLE symbol (FEh)
    b. A LSE symbol
    c. A CLSE symbol
2. Parse the LSE Symbol in each LT Transaction and verify that:
    a. Bits [7:6] (*StartLT*) are set to 10b (4.1.1.2.1#4)
    b. Bit 5 (*LSELane*) is 0 for an LT_LRoff Transaction (4.1.1.2.1#3)
    c. Bit 4 is reserved (0b) (1.7#5)
    d. Bits [3:0] (*LSESymbol*) do not contain reserved values (1.7#1)

    Note: Defined LSESymbol values are 0000b (LT_Fall), 0001b (LT_Gen_2), 0010b (LT_Resume), 0011b (LT_LRoff), 0101b (LT_Gen_3), 0110b (LT_Resume2)

3. Parse each AT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.2#1)
    a. A DLE symbol (FEh)
    b. A STX symbol
    c. No more than 66 Data Symbols (4.1.1.2.2#2)
    d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5,4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
    e. A DLE symbol (FEh)
    f. An ETX symbol (40h)
4. For each AT Command:
    a. Parse the STX Symbol and verify that: (13.2.1.2.2#1)
        i. Bits [7:6] (*StartAT*) are 00b
        ii. Bit 5 is reserved (0b) (1.7#5)
        iii. Bit 4 (*Responder*) is 0b (13.2.1.2.2#3)
    b. Parse the Data Symbols and verify that: (4.1.1.3.1#1)
        i. The REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 127 to 255
        ii. The LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
        iii. If WnR=0, there is no COMMAND_DATA
        iv. If WnR=1b, the COMMAND_DATA is the same length as in the LEN field

5. For each AT Response:
    a. Parse the STX Symbol and verify that: (13.2.1.2.2#1)
        i. Bits [7:6] (*StartAT*) are 00b
        ii. Bit 5 is reserved (0b) (1.7#5)
        iii. Bit 4 (*Responder*) is 0b (13.2.1.2.2#3)
        iv. Bit 2 (*Recipient*) is 1b (13.2.1.2.2#5)
    b. Parse the Data Symbols and verify that they consist of the following symbols in the following order: (4.1.1.3.1#2)
        i. A REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 127 to 255
        ii. A LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
        iii. If WnR=0b, RESPONSE_DATA is the same length as in the LEN field (unless test specifies otherwise)
        iv. If WnR=1n, RESPONSE_DATA is 00h (unless test specified otherwise)
    c. Verify that the value in the LEN field is not greater than 64 (4.1.1.3.1#2)
6. When the PUT receives an AT Command with the Recipient bit set to 1b, verify that the PUT responds with an AT Response (unless the test specifies otherwise). (4.1.1.2.2#9)
7. Parse each Broadcast RT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.3.1#1)
    a. A DLE symbol (FEh)
    b. A STX symbol
    c. Two Link Parameters symbols
    d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5,4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
    e. A DLE symbol (FEh)
    f. An ETX symbol (40h)
8. Parse the STX Symbol for a Broadcast RT Transaction and verify that:
    a. *Index* = 0 (4.1.1.2.3.1#4)
    b. *CmdNotResp*=1b (4.1.1.2.3.1#5)
9. Parse Byte 2 of a Broadcast RT Transaction and verify that:
    a. Bits [7:5] are 0 (reserved) (1.7#5)
    b. Bit 4 (*TBTCompatibleSpeed*) is 1b (13.2.1.2.3#1)
    c. Bit 1 (reserved) is 0b (1.7#5)
    d. Bit 0 (*USB4*) is 0b (13.2.1.2.3#1)
10. Parse each Addressed RT Transaction and verify that it consists of the following symbols in the following order: (4.1.1.2.3.2#1)
    a. A DLE symbol (FEh)
    b. A STX symbol
    c. No more than 66 Data Symbols (4.1.1.2.3.2#2)
    d. 2 CRC Symbols (Low and High) with correct CRC (4.1.1.2.4#5,4.1.1.2.4#6, 4.1.1.2.4#7, 4.1.1.2.4#8, 4.1.1.2.4#9)
    e. A DLE symbol (FEh)
    f. An ETX symbol (40h)
11. Parse the Data Symbols of each RT Command and verify that it consists of the following symbols in the following order: (4.1.1.3.1#1)
    a. The REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 127 to 255
    b. The LEN symbol does not contain a value greater than 64
    c. If WnR=0, there is no COMMAND_DATA
    d. If WnR=1b, the COMMAND_DATA is the same length as in the LEN field

12. Parse the Data Symbols of each RT Response and verify that it consists of the following symbols in the following order: (4.1.1.3.1#2)
    a. The REG symbol does not contain the values 2 to 7, 10 to 11, 14, or 127 to 255
    b. The LEN symbol does not contain a value greater than 64 (4.1.1.3.1#2)
    c. If WnR=0b, RESPONSE_DATA is the same length as in the LEN field (unless test specifies otherwise)
    d. If WnR=1n, RESPONSE_DATA is 00h (unless test specified otherwise)
13. Verify that the PUT sends an AT Response within tCmdResponse (50ms) of receiving an AT Command. (4.1.1.2.5.1#1)
14. Verify that the PUT sends an Addressed RT Response within tCmdResponse (50ms) of receiving an Addressed RT Command. (4.1.1.2.5.2#1)

Transaction Tests

TD 4.44 Bounce Mechanism Test

A. Purpose:

- Verify that the Bounce Mechanism is performed correctly

B. Asserts:

- 13.2.1.2.2.1#1-4

C. Test Setups

- H4 (Host)
- D7 (Device)
- D8 (Hub UFP)
- D9 (Hub DFP)

D. Procedure:

USB4 performs the following steps:

Part 0 – Setup

1. Reset UUT
2. Perform Lane Initialization
3. Initiate Lane Bonding

Part 1 – Link Partner

4. Tell the UUT to send a Write Command to the Re-timer that is adjacent to the Link Partner
5. Verify that a Write Response is received
6. Tell the UUT to send a Read Command to the Re-timer that is adjacent to the Link Partner
7. Verify that a Read Response is received
8. Verify that the data in the Read Response is the same as what was written

Part 2 – Adjacent Re-Timer

9. Tell the Link Partner to send a Write Command to the Re-timer that is adjacent to the UUT
10. Verify that a Write Response is received
11. Tell the Link Partner to send a Read Command to the Re-timer that is adjacent to the UUT
12. Verify that a Read Response is received
13. Verify that the data in the Read Response is the same as what was written

TD 4.45 SB Register Space Test

A. Purpose:

- Verify that SB Register space is formatted correctly

B. Asserts:

- 13.2.1.3#1

C. Test Setups

- H4 (Host)
- D7 (Device)
- D8 (Hub UFP)
- D9 (Hub DFP)

D. Procedure:

USB4 performs the following steps:

Part 0 – Setup

1. Reset UUT
2. Perform Lane Initialization
3. Initiate Lane Bonding
4. Read SB Registers, 3, 4, and 10
5. In SB Register 3, verify the following values:
    a. Byte 0 = 41h
    b. Byte 1 = 50h
    c. Byte 2 = 50h
    d. Byte 3 = 20h
6. In SB Register 4, verify the following values:
    a. Byte 0 = 45h
    b. Byte 1 = 4Dh
    c. Byte 2 = 20h
    d. Byte 3 = 20h
7. In SB Register 10, verify that Byte 0 is 00h

Lane Initialization Tests

TD 4.46 Lane Initialization Test

A. Purpose:

- Verify that Lane Initialization is performed correctly in TBT3-Compatibility mode

B. Asserts:

- 13.2.1.4.4#1-8, 13.2.1.4.4.1#1-14, 13.2.1.4.4.2#1-13

C. Repetitions:

- Repeat with a TBT3 device that uses a:
  - TBT3 Sideband Channel
  - USB4 Sideband Channel
- Repeat at Gen 2 and Gen 3 speeds
- Repeat with RS-FEC enabled and disabled
- Repeat with Passive Cable, Uni-Directional Active Cable, and Bi-Directional Active Cable

D. Test Setups

- H4 (Host)
- D7 (Device)
- D8 (Hub UFP)
- D9 (Hub DFP)

E. Procedure:

USB4 performs the following steps:

Part 0 – Setup

1. Reset PUT
2. Start Lane Initialization
3. In Phase 3, when the UUT sends a Broadcast RT Transaction, verify that:
   a. If USB4 device uses a USB4 Sideband Channel, USB4 bit is 1b (13.2.1.4.2#5, 13.2.1.4.2#7)
   b. If USB4 device uses a TBT3 Sideband Channel, USB4 bit is 0b (13.2.1.4.2#6, 13.2.1.4.2#8)
4. In phase 4, verify the following:
   a. If the UUT does not include any On-Board Re-timers and is operating at Gen 2 speed, verify that:
      i. UUT sends an LT_Gen_2 Transaction for each enabled Lane every tLaneParams (13.2.1.4.3#2)
      ii. UUT continues sending LT_Gen_2 Transactions until all of the following are true: At least tLTPhase4 time has passed from completion of Phase 2; UUT sent LT_Gen_2 Transactions at least twice; UUT received an LT_Gen_2 Transaction (13.2.1.4.3#3)
   b. If the UUT does not include any On-Board Re-timers and is operating at Gen 3 speed, verify that:
      i. UUT sends an LT_Gen_3 Transaction for each enabled Lane every tLaneParams (13.2.1.4.3#4)
      ii. UUT continues sending LT_Gen_3 Transactions until all of the following are true: At least tLTPhase4 time has passed from completion of Phase 2; UUT sent LT_Gen_3 Transactions at least twice; UUT received an LT_Gen_3 Transaction (13.2.1.4.3#5)

c. If the UUT includes one or more On-Board Re-timers and is operating at Gen 2 speed, verify that:
    i. UUT sends a Broadcast RT Transaction every tLaneParams (13.2.1.4.3#6)
    ii. UUT sends an LT_Gen_2 Transaction for each enabled Lane (13.2.1.4.3#8)
    iii. UUT continues sending the Broadcast RT and LT_Gen_2 Transactions until all of the following conditions are true: At least tLTPhase4 time has passed from completion of Phase 2; UUT sent LT_Gen_2 Transactions at least twice; UUT received an LT_Gen_2 Transaction (13.2.1.4.3#9)
d. If the UUT includes one or more On-Board Re-timers and is operating at Gen 3 speed, verify that:
    i. UUT sends a Broadcast RT Transaction every tLaneParams (13.2.1.4.3#10)
    ii. UUT sends an LT_Gen_3 Transaction for each enabled Lane (13.2.1.4.3#12)
    iii. UUT continues sending the Transactions until all of the following conditions are true: At least tLTPhase4 time has passed from completion of Phase 2; UUT sent LT_Gen_3 Transactions at least twice; UUT received an LT_Gen_3 Transaction (13.2.1.4.3#13)

5. If the UUT Router is connected directly to a Cable Re-timer (i.e. UUT is connected by an Active Cable and does not contain any On-Board Re-Timers), perform Asymmetric TxFFE Parameter Negotiation
6. Else perform Symmetric TxFFE Parameter Negotiation
7. In phase 5, verify the following:
    a. If Asymmetric TxFFE Parameter Negotiation is performed:
        i. UUT Transmitter sends an LT_Resume2 Transaction for Lane 1 (LSELane field = 1b) (13.2.1.4.4#3)
        ii. UUT Transmitter sends an LT_Resume2 Transaction for Lane 0 (LSELane field = 0b) (13.2.1.4.4#3)
    b. UUT sets the Clock Switch Done bit to 1b for Lane 1 (13.2.1.4.4#6)
    c. UUT sets the Clock Switch Done bit to 1b for Lane 0 (13.2.1.4.4#6)

Adapter State Tests

TD 4.47 CLd Test (DFP Only)

Note: This test is only performed on the DFP.

A. Purpose:

- Verify that CLd state is entered and exited correctly

B. Asserts:

- 13.2.2.1.1#1-6

C. Repetitions:

- Repeat at Gen 2 and Gen 3 speeds

D. Test Setups

- H4 (Host)
- D9 (Hub)

E. Procedure:

USB4 performs the following steps:

Part 0 – Setup

1. Reset UUT
2. Perform Lane Initialization
3. Initiate Lane Bonding
4. Transition the PUT Adapters to CLd state
5. Transition the PUT Adapters out of CLd state
6. Verify that the Lane 0 Adapter does not start Lane Initialization until it receives one of the following: (13.2.2.1.1#3)
    a. A Broadcast RT Transaction with Lane0Eanbled set to 1b
    b. An LT_Gen_2 Transaction with the *LSELane* bit set to 0b
    c. An LT_Gen_3 Transaction with the *LSELane* bit set to 0b
7. Verify that the Lane 1 Adapter does not start Lane Initialization until it receives one of the following: (13.2.2.1.1#4)
    a. A Broadcast RT Transaction with Lane1Eanbled set to 1b
    b. An LT_Gen_2 Transaction with the *LSELane* bit set to 1b
    c. An LT_Gen_3 Transaction with the *LSELane* bit set to 1b
8. Verify that the Lane Adapters start Lane Initialization from phase 4 (13.2.2.1.1#5)
9. Verify that the Lane Adapters maintain state from phases 1 through 3 before Adapters were put in CLd state (13.2.2.1.1#6)

Lane 0/Lane 1 Tests

Background Check

This test is performed by the or Exerciser in conjunction with all of the Lane 0/Lane 1 Tests.

1. Parse each TSI and TS2 Ordered Set and verify that bits 31:29 (Rsvd) are 0. (4.2.1.3.5#6)
2. When an Adapter transitions to the CL0 state and Lanes are not bonded, verify that the first bytes transmitted after the last TS2 Ordered Set are either a Transport Layer Packet header or an Ordered Set that is not SLOS, TS1, or TS2. (4.4.1#1)
3. When an Adapter transitions to the CL0 state and Lanes are bonded, verify that the first bytes transmitted after the last TS2 Ordered Set are a de-skew Ordered Set followed by either a Transport Layer Packet header, an Idle Packet or any Ordered Set other than SLOS, TS1 or TS2. (4.4.1#2)
4. When operating with a Dual-lane Link, verify that, if one Lane transitions to Training State, other Lane also transitions to training state (4.2.2.2#8)

Link Tests

TD 4.48 Single Lane Link Test (DFP Only)

A. Purpose:

- Verify that the Single Lane Link configuration is supported

B. Asserts:

- 13.2.3.1#1-3

C. Test Setups

- H4 (Host)
- D9 (Hub)

D. Procedure:

USB4 performs the following steps:

Part 0 – Setup

1. Reset UUT
2. Perform Lane Initialization
3. Do not initiate Lane Bonding
4. Set up a loopback Path over Lane 0
5. Set up a loopback Path over Lane 1
6. Perform loopback transfer on each Path simultaneously
7. Verify that both loopback transfers complete without error (13.2.3.1#2)
8. Disable Lane 0
9. Perform loopback transfer on Path 1
10. Verify that loopback transfer completes without error (13.2.3.1#3)

TD 4.49 Sleep Disconnect Test (UFP Only)

Note: This test is only performed on the UFP.

A. Purpose:
- Verify that Device Router performs disconnect after sleep entry when required

B. Asserts:
- 13.2.4#1
- 13.2.4.1#1-3

C. Test Setups
- D7 (Device)
- D8 (Hub)

D. Repetitions:
- Repeat for Lane 1 and Lane 0

E. Procedure:

USB4 performs the following steps:

Part 0 – Setup

1. Reset UUT
2. Perform Lane Initialization
3. Initiate Lane Bonding

Part 1 – Not Inter-Domain

4. Set *Lane is Inter-Domain* bit to 0b
5. Set *Lane Configured* bit to 0b
6. Transition to sleep
7. Verify disconnect (13.2.4.1#2, 13.2.4.1#3)

Part 2 – Inter-Domain

8. Set *Lane is Inter-Domain* bit to 1b
9. Set *Inter-Domain Disconnect on Sleep* to 1b
10. Transition to sleep
11. Verify disconnect (13.2.4.1#2, 13.2.4.1#3)

TD 4.50 VSEC 6 Wake Test (DFP Only)

Note: This test is only performed on the DFP.

A. Purpose:

- Verify that Router initiates Wake correctly

B. Asserts:

- 13.2.4.3#1

C. Test Setups
- H4 (Host)
- D9 (Hub)

D. Repetitions:
- Repeat for the following wake events:
  - Connect USB4 device (bit 1)
  - Disconnect USB4 device (bit 2)
  - Connect DisplayPort Device (bit 3)
  - Disconnect DisplayPort Device (bit 4)
  - USB4 Wake (bit 5)
  - PCIe wake (bit 6)
  - Connect USB 3 device (bit 9)
  - Disconnect USB 3 device (bit 10)

E. Procedure:

USB4 performs the following steps:

1. Reset UUT
2. Perform Lane Initialization
3. Initiate Lane Bonding
4. Set appropriate bit in the *Enable Wake Events* field in VSEC6 (see repetitions)
5. Transition the host system to sleep
6. Initiate wake event (see repetitions)
7. Verify that host system comes out of sleep state (13.2.4.3#1)

TD 4.51 Start Link Initialization Bit Test (DFP Only)

Note: This test is only performed on the DFP.

A. Purpose:
   - Verify that Router exits sleep correctly

B. Asserts:
   - 13.2.4.4#1-2

C. Test Setups
   - H4 (Host)
   - D9 (Hub)

D. Repetitions:
   - Repeat for Lane 1 and Lane 0

E. Procedure:

USB4 performs the following steps:

Part 0 – Setup

1. Reset UUT
2. Perform Lane Initialization
3. Initiate Lane Bonding

Part 1 – Not Inter-Domain

4. Set the *Lane is Configured* bit to 0b
5. Set the *Lane is Inter-Domain* bit to 0b
6. Transition the host system to sleep
7. Initiate Wake
8. Verify Adapter does not start Link Initialization (13.2.4.4#1, 13.2.4.4#2)
9. Set the *Start Link Initialization* bit to 1b
10. Verify that Adapter starts Link Initialization (13.2.4.4#1, 13.2.4.4#2)

Part 2 –Inter-Domain

11. Set the *Lane is Configured* bit to 1b
12. Set the *Lane is Inter-Domain* bit to 1b
13. Transition the host system to sleep
14. Initiate Wake
15. Verify Adapter does not start Link Initialization (13.2.4.4#1, 13.2.4.4#2)
16. Set the *Start Link Initialization* bit to 1b
17. Verify that Adapter starts Link Initialization (13.2.4.4#1, 13.2.4.4#2)